MC14175B

Quad Type D Flip-Flop

The MC14175B quad type D flip−flop is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each of the four flip−flops is positive−edge triggered by a common clock input (C). An active−low reset input (R) asynchronously resets all flip−flops. Each flip−flop has independent Data (D) inputs and complementary outputs (Q and Q). These devices may be used as shift register elements or as type T flip−flops for counter and toggle applications.

Features

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Compatible with Two Low−Power TTL Loads or One Low−Power Schottky TTL Load
- Functional Equivalent to TTL 74175
- These Devices are Pb−Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

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MARKING DIAGRAMS

PDIP−16
P SUFFIX
CASE 648

```
16
MC14175BCP
 o  AWLYYWWG
1
```

SOIC−16
D SUFFIX
CASE 751B

```
16
   14175BG
 o  AWLYWW
1
```

SOEIAJ−16
F SUFFIX
CASE 966

```
16
   MC14175B
 o   ALYWG
1
```

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input or Output Current (DC or Transient) per Pin	I_{in}, I_{out}	±10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range		−65 to +150	°C
Lead Temperature (8−Second Soldering)		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic "P and D/DW"
   Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
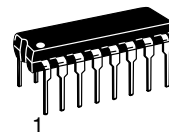
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
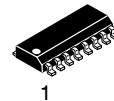
ORDERING INFORMATION
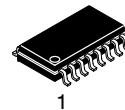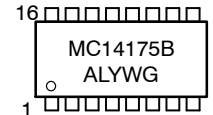
Device	Package	Shipping[†]
MC14175BCPG	PDIP−16 (Pb−Free)	500 Units/Rail
MC14175BDG	SOIC−16 (Pb−Free)	48 Units/Rail
MC14175BDR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel
NLV14175BDR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel
MC14175BFELG	SOEIAJ−16 (Pb−Free)	2000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
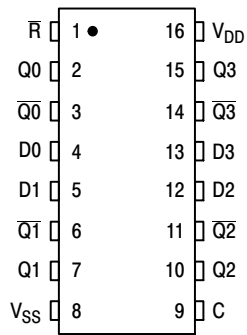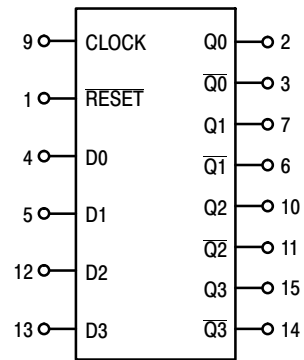
MC14175B

Figure 1. Pin Assignment

$\overline{R}$	1 ●	16	V_{DD}
Q0	2	15	Q3
$\overline{Q0}$	3	14	$\overline{Q3}$
D0	4	13	D3
D1	5	12	D2
$\overline{Q1}$	6	11	$\overline{Q2}$
Q1	7	10	Q2
V_{SS}	8	9	C

Figure 1. Pin Assignment

TRUTH TABLE

Inputs			Outputs	
Clock	Data	$\overline{\text{Reset}}$	Q	$\overline{Q}$
⟋	0	1	0	1
⟋	1	1	1	0
⟍	X	1	Q	$\overline{Q}$	No Change
X	X	0	0	1

X = Don't Care

Figure 2. Block Diagram

9	CLOCK	Q0	2
		$\overline{Q0}$	3
1	$\overline{RESET}$	Q1	7
4	D0	$\overline{Q1}$	6
5	D1	Q2	10
		$\overline{Q2}$	11
12	D2	Q3	15
13	D3	$\overline{Q3}$	14

V_{DD} = PIN 16
V_{SS} = PIN 8
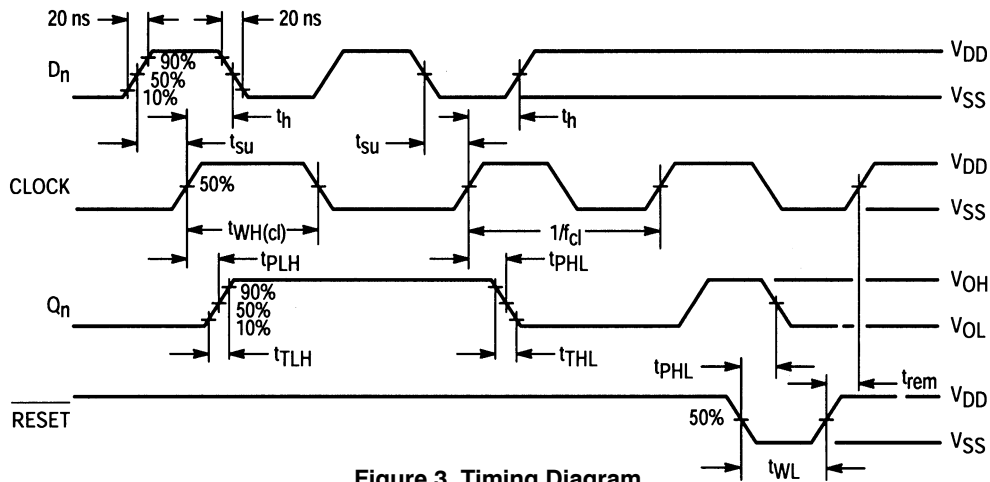
Figure 2. Block Diagram
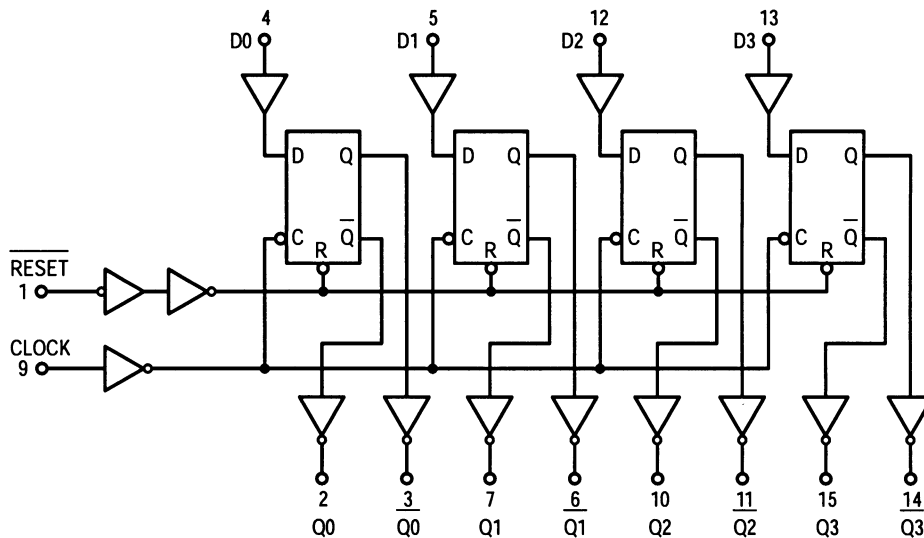

Figure 3. Timing Diagram

Figure 4. Functional Block Diagram

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	– – – –	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	– – – –	– 1.7 – 0.36 – 0.9 – 2.4	– – – –	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current	I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μAdc
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15		I_T = (1.7 μA/kHz) f + I_{DD} I_T = (3.4 μA/kHz) f + I_{DD} I_T = (5.0 μA/kHz) f + I_{DD}						μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50)$ Vfk where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ (Note 6)	Max	
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time — Clock to Q, Q̄ t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 175 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 72 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 57 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	220 90 70	400 160 120	ns
Propagation Delay Time — Reset to Q, Q̄ t_{PHL} = (0.9 ns/pF) C_L + 280 ns t_{PHL} = (0.36 ns/pF) C_L + 112 ns t_{PHL} = (0.26 ns/pF) C_L + 87 ns	t_{PHL}, t_{PLH}	5.0 10 15	– – –	325 130 100	500 200 150	ns
Clock Pulse Width	t_{WH}	5.0 10 15	250 100 75	110 45 35	– – –	ns
Reset Pulse Width	t_{WL}	5.0 10 15	200 80 60	100 40 30	– – –	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	– – –	4.5 11 14	2.0 5.0 6.5	mHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	– – –	– – –	15 5.0 4.0	μs
Data Setup Time	t_{su}	5.0 10 15	120 50 40	60 25 20	– – –	ns
Data Hold Time	t_h	5.0 10 15	80 40 30	40 20 15	– – –	ns
Reset Removal Time	t_{rem}	5.0 10 15	250 100 80	125 50 40	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14175B

PACKAGE DIMENSIONS
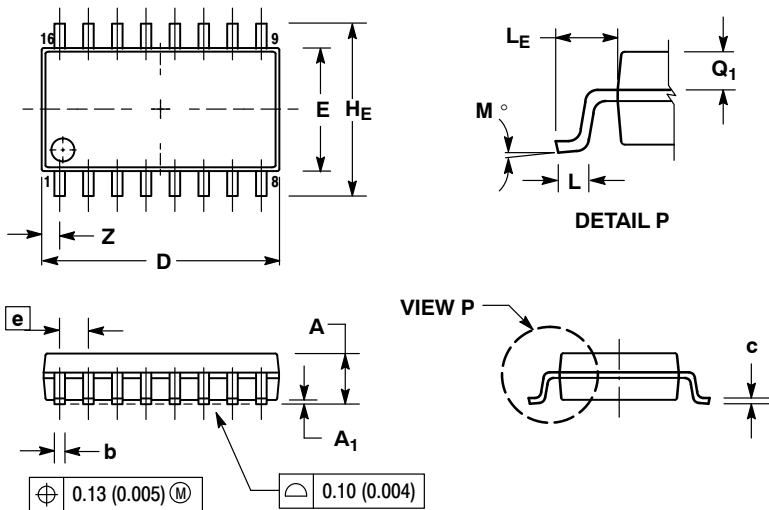
PDIP−16
CASE 648−08
ISSUE T
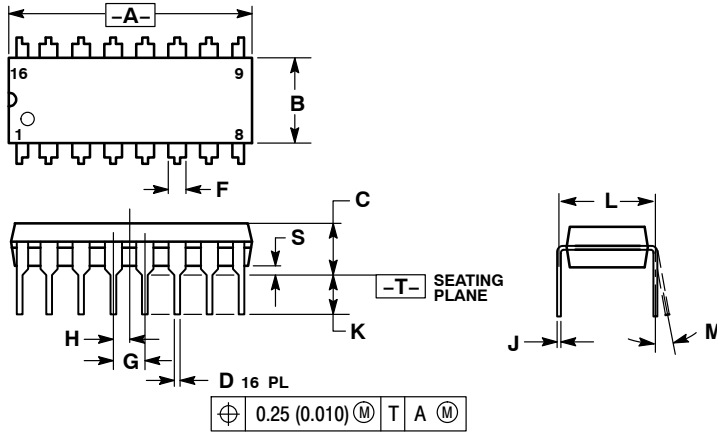
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOEIAJ−16
CASE 966−01
ISSUE A

DETAIL P

VIEW P

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

MC14175B

PACKAGE DIMENSIONS

SOIC−16
CASE 751B−05
ISSUE K
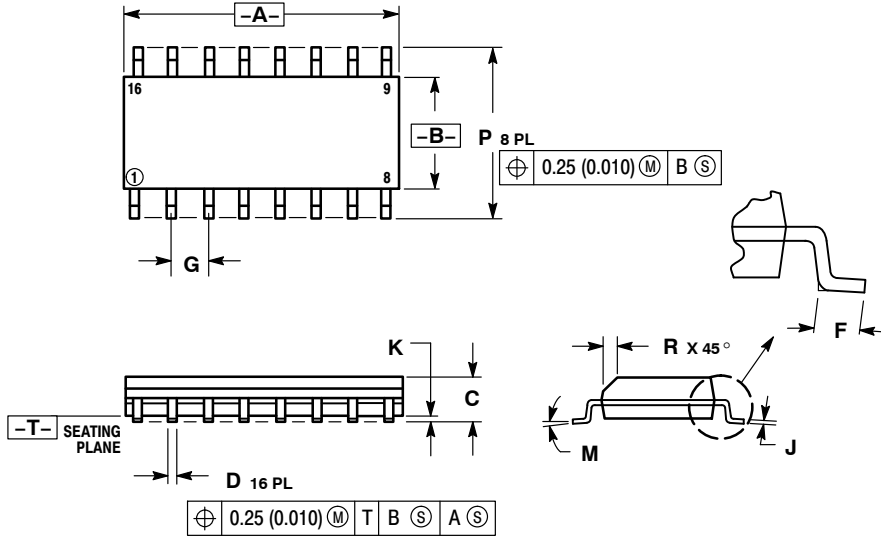
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS