Octal D-Type Latch with 3-State Output

The MC74VHC373 is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

- High Speed: $t_{PD} = 5.0 \text{ ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 4.0 \mu A$ (Max) at $T_A = 25^{\circ}C$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% \ V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.9 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates

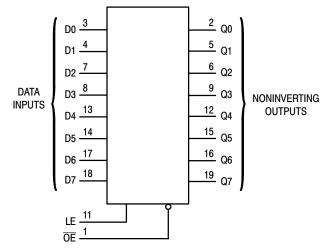


Figure 1. LOGIC DIAGRAM

FUNCTION TABLE

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L L H	H H L X	H L X	H L No Change Z



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MARKING DIAGRAMS



SOIC-20 WIDE DW SUFFIX CASE 751D





TSSOP-20 DT SUFFIX CASE 948E





SOIC EIAJ M SUFFIX CASE 967



A = Assembly Location

WL = Wafer Lot YY = Year

WW = Work Week

PIN ASSIGNMENT

OE [1●	20	v _{cc}
Q0 [2	19] Q7
D0 [3	18	D7
D1 [4	17	D6
Q1 [5	16	Q6
Q2 [6	15] Q5
D2 [7	14] D5
D3 [8	13	D4
Q3 [9	12	Q4
GND [10	11	LE

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC373DW	SOIC-WIDE	38 / Rail
MC74VHC373DWR2	SOIC-WIDE	1000 / Reel
MC74VHC373DT	TSSOP-20	75 / Rail
MC74VHC373DTR2	TSSOP-20	2500 / Reel
MC74VHC373M	SOIC EIAJ	40 / Rail
MC74VHC373MEL	SOIC EIAJ	2000 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	r	Value	Unit
V _{CC}	DC Supply Voltage		- 0.5 to + 7.0	V
V _{in}	DC Input Voltage		- 0.5 to + 7.0	V
V _{out}	DC Output Voltage		-0.5 to $V_{CC} + 0.5$	V
I _{IK}	Input Diode Current	- 20	mA	
I _{OK}	Output Diode Current	± 20	mA	
I _{out}	DC Output Current, per Pin		± 25	mA
Icc	DC Supply Current, V _{CC} and GI	ND Pins	± 75	mA
P _D	Power Dissipation in Still Air,	er Dissipation in Still Air, SOIC Packages† TSSOP Package†		mW
T _{stg}	Storage Temperature	- 65 to + 150	°C	

^{*} Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
V _{CC}	DC Supply Voltage		2.0	5.5	V
V _{in}	DC Input Voltage		0	5.5	V
V _{out}	DC Output Voltage		0	V_{CC}	V
T _A	Operating Temperature		- 40	+ 85	°C
t _r , t _f	Input Rise and Fall Time $V_{CC} = V_{CC} = V_{$	3.3 V 5.0 V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

			V_{CC} $T_A = 25^{\circ}C$ $T_A = -$	$T_A = -40$	0 to 85°C				
Symbol	Parameter	Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V _{CC} x 0.7			1.50 V _{CC} x 0.7		٧
V _{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V _{CC} x 0.3		0.50 V _{CC} x 0.3	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		
V _{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μА

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

[†]Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

DC ELECTRICAL CHARACTERISTICS

			v _{cc}		T _A = 25°C		T _A = - 40	0 to 85°C	
Symbol	Parameter	Test Conditions	v	Min	Тур	Max	Min	Max	Unit
I _{OZ}	Maximum Three–State Leakage Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5			± 0.25		± 2.5	μА
lcc	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			4.0		40.0	μА

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$)

					T _A = 25°C		T _A = -4	0 to 85°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to Q	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		7.3 9.8	11.4 14.9	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		4.9 6.4	7.2 9.2	1.0 1.0	8.5 10.5	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, LE to Q	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		5.0 6.5	7.2 9.2	1.0 1.0	8.5 10.5	
t _{PZL} , t _{PZH}	Output Enable Time, OE to Q	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $R_L = 1 \text{ k}\Omega$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		7.3 9.8	11.4 14.9	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $R_L = 1 \text{ k}\Omega$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		5.5 7.0	8.1 10.1	1.0 1.0	9.5 11.5	
t _{PLZ} , t _{PHZ}	Output Disable Time, OE to Q	$\begin{aligned} &V_{CC} = 3.3 \pm 0.3 \text{ V} \\ &R_L = 1 \text{ k}\Omega \end{aligned}$	C _L = 50 pF		9.5	13.2	1.0	15.0	ns
		$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1 \text{ k}\Omega$	C _L = 50 pF		6.5	9.2	1.0	10.5	
t _{OSLH} , t _{OSHL}	Output to Output Skew	V _{CC} = 3.3 ± 0.3 V (Note 1)	C _L = 50 pF			1.5		1.5	ns
		V _{CC} = 5.5 ± 0.5 V (Note 1)	C _L = 50 pF			1.0		1.0	ns
C _{in}	Maximum Input Capacitance				4	10		10	pF
C _{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				6				pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 2)	27	pF

NOISE CHARACTERISTICS (Input $t_f = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

		T _A =		
Symbol	Parameter	Тур	Max	Unit
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.6	0.9	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	- 0.6	- 0.9	V
V _{IHD}	V _{IHD} Minimum High Level Dynamic Input Voltage		3.5	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.
 C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per latch). C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0 \text{ ns}$)

			T _A =	25°C	T _A = - 40 to 85°C	
Symbol	Parameter	Test Conditions	Тур	Limit	Limit	Unit
t _{w(h)}	Minimum Pulse Width, LE	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$		5.0 5.0	5.0 5.0	ns
t _{su}	Minimum Setup Time, D to LE	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$		4.0 4.0	4.0 4.0	ns
t _h	Minimum Hold Time, D to LE	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$		1.0 1.0	1.0 1.0	ns

SWITCHING WAVEFORMS

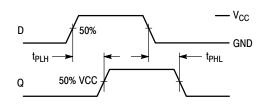


Figure 2.

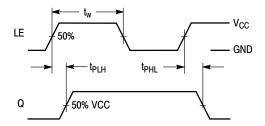


Figure 3.

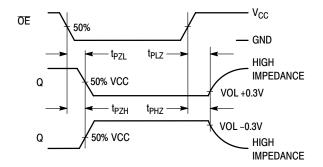


Figure 4.

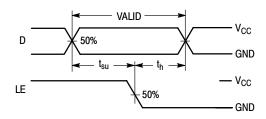
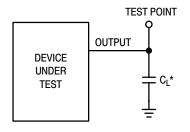
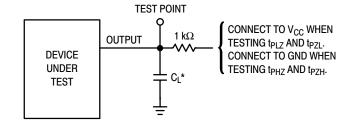


Figure 5.

TEST CIRCUITS





*Includes all probe and jig capacitance

*Includes all probe and jig capacitance

Figure 6.

Figure 7.

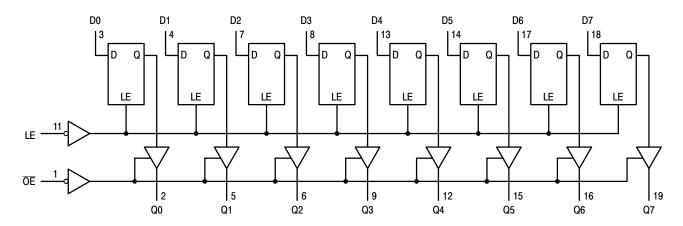


Figure 8. EXPANDED LOGIC DIAGRAM

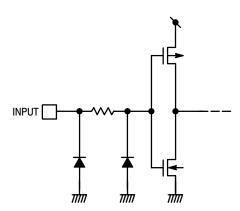
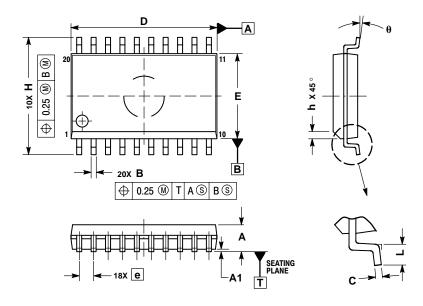


Figure 9. INPUT EQUIVALENT CIRCUIT

OUTLINE DIMENSIONS

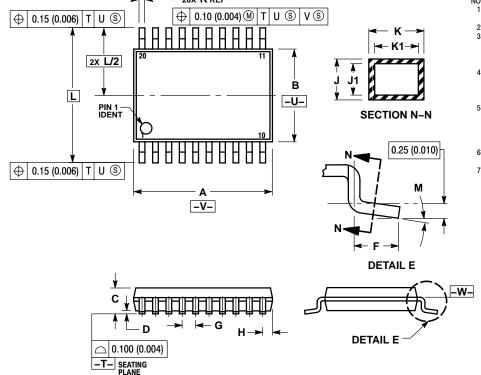
SOIC **DW SUFFIX** CASE 751D-05 ISSUE F



- I. DIMENSIONS ARE IN MILLIMETERS.
 INTERPRET DIMENSIONS AND TOLERANCES
 PER ASME Y14.5M, 1994.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRICION.
- PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS
DIM	MIN	MAX
Α	2.35	2.65
A1	0.10	0.25
В	0.35	0.49
С	0.23	0.32
D	12.65	12.95
Е	7.40	7.60
е	1.27	BSC
Н	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

TSSOP DT SUFFIX CASE 948E-02 ISSUE B



- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- (U.UVO) FER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- PER SIDE.

 DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
 EXCESS OF THE K DIMENSION AT MAXIMUM
 MATERIAL CONDITION.

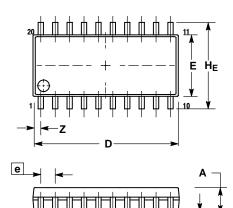
 ETERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

$\overline{}$				
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	6.40	6.60	0.252	0.260
В	4.30	4.50	0.169	0.177
C		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

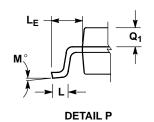
OUTLINE DIMENSIONS

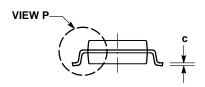
SOIC EIAJ M SUFFIX CASE 967-01 **ISSUE O**



0.10 (0.004)

0.13 (0.005) M





NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) DEED RICE.
- PROTRUSIONS SHALL NUT EXCEED U.13 (U.50U)
 PER SIDE.

 4. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.

 5. THE LEAD WIDTH DIMENSION (b) DOES NOT
 INCLUDE DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
 TOTAL IN EXCESS OF THE LEAD WIDTH
 DIMENSION AT MAXIMUM MATERIAL CONDITION.
 DAMBAR CANNOT BE LOCATED ON THE LOWER DIMENSION AT MAXIMUM MATERIAL CONDITION.
 DAMBAR CANNOT BE LOCATED ON THE LOWER
 RADIUS OR THE FOOT. MINIMUM SPACE
 BETWEEN PROTRUSIONS AND ADJACENT LEAD
 TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
Е	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10°
Q_1	0.70	0.90	0.028	0.035
Z		0.81		0.032

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