MC44608

Few External Components Reliable and Flexible SMPS Controller

The MC44608 is a high performance voltage mode controller designed for off−line converters. This high voltage circuit that integrates the startup current source and the oscillator capacitor, requires few external components while offering a high flexibility and reliability.

The device also features a very high efficiency standby management consisting of an effective Pulsed Mode operation. This technique enables the reduction of the standby power consumption to approximately 1.0 W while delivering 300 mW in a 150 W SMPS.

General Features

- Integrated Startup Current Source
- Lossless Off−Line Startup
- Direct Off−Line Operation
- Fast Startup
- Flexibility
- Duty Cycle Control
- Undervoltage Lockout with Hysteresis
- On Chip Oscillator Switching Frequency 40, 75, or 100 kHz
- Secondary Control with Few External Components
- Pb−Free Packages are Available

Protections

- Maximum Duty Cycle Limitation
- Cycle by Cycle Current Limitation
- Demagnetization (Zero Current Detection) Protection
- “Over V_{CC} Protection” Against Open Loop
- Programmable Low Inertia Over Voltage Protection Against Open Loop
- Internal Thermal Protection

SMPS Controller

- Pulsed Mode Techniques for a Very High Efficiency Low Power Mode
- Lossless Startup
- Low dV/dT for Low EMI Radiations

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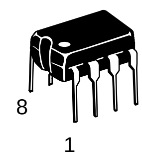
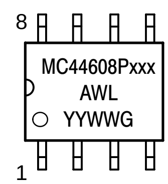


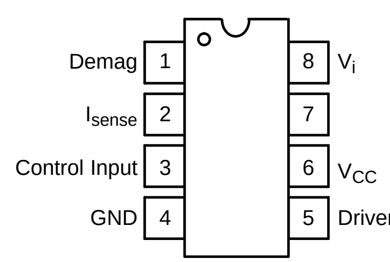
PDIP−8
P SUFFIX
CASE 626

MARKING DIAGRAM



MC44608Pxxx	= Device Code	
	xxx = 40, 75, or 100	
A	= Assembly Location	
WL	= Wafer Lot	
YY	= Year	
WW	= Work Week	
G	= Pb−Free Package	

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

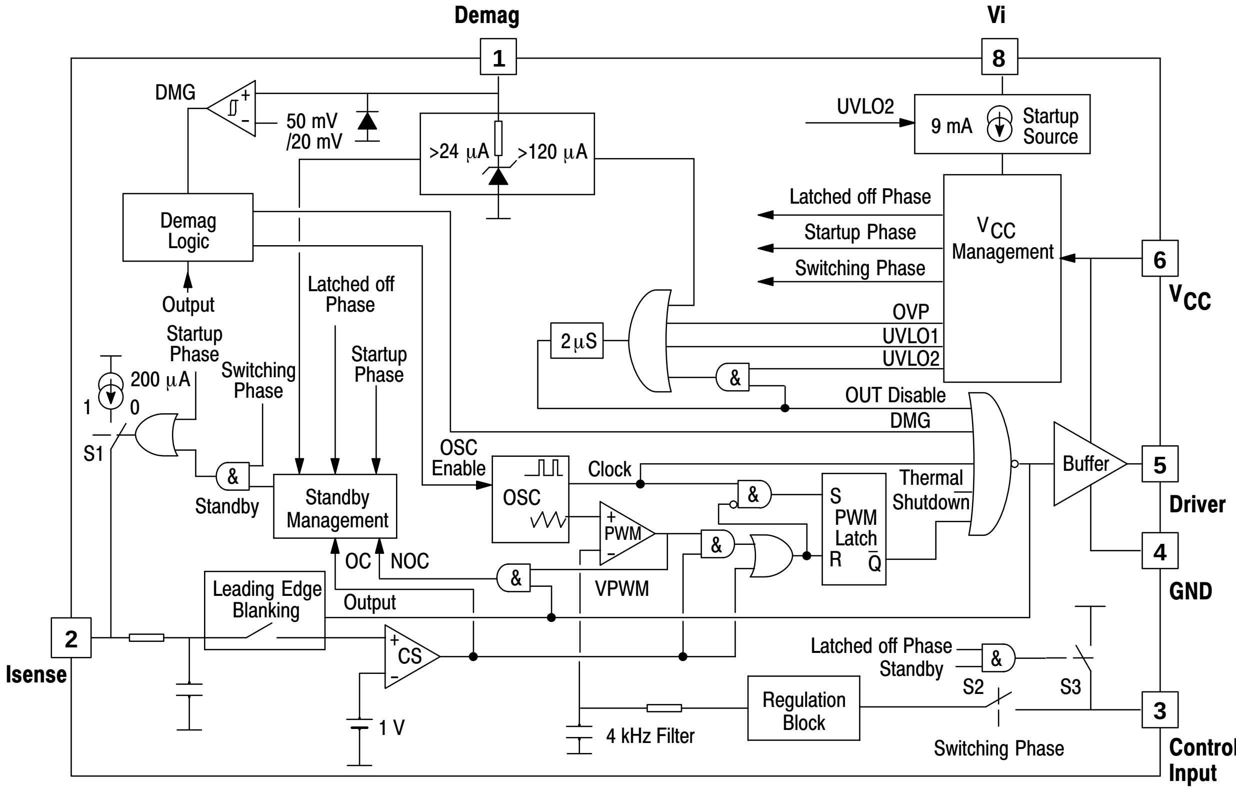


Figure 1. Representative Block Diagram

ORDERING INFORMATION

Device	Switching Frequency	Package	Shipping
MC44608P40	40 kHz	PDIP−8	50 Units / Rail
MC44608P40G		PDIP−8 (Pb−Free)	50 Units / Rail
MC44608P75	75 kHz	PDIP−8	50 Units / Rail
MC44608P75G		PDIP−8 (Pb−Free)	50 Units / Rail
MC44608P100	100 kHz	PDIP−8	50 Units / Rail

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply Current	I_{CC}	30	mA
Output Supply Voltage with Respect to Ground	V_{CC}	16	V
All Inputs except Vi	V_{inputs}	−1.0 to +16	V
Line Voltage Absolute Rating	V_i	500	V
Recommended Line Voltage Operating Condition	V_i	400	V
Power Dissipation and Thermal Characteristics Maximum Power Dissipation at T_A = 85°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$	 600 100	 mW °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	−25 to +85	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Output Resistor					Ω
Sink Resistance	R_{OL}	5.0	8.5	15	
Source Resistance	R_{OH}	–	15	–	
Output Voltage Rise Time (from 3.0 V up to 9.0 V) (Note 1)	t_r	–	50	–	ns
Output Voltage Falling Edge Slew−Rate (from 9.0 V down to 3.0 V) (Note 1)	t_f	–	50	–	ns
CONTROL INPUT SECTION					
Duty Cycle @ I_{pin3} = 2.5 mA	d_{2mA}	–	–	2.0	%
Duty Cycle @ I_{pin3} = 1.0 mA	d_{1mA}	36	43	48	%
Control Input Clamp Voltage (Switching Phase) @ I_{pin3} = −1.0 mA		4.75	5.0	5.25	V
Latched Phase Control Input Voltage (Standby) @ I_{pin3} = +500 μA	$V_{LP-stby}$	3.4	3.9	4.3	V
Latched Phase Control Input Voltage (Standby) @ I_{pin3} = +1.0 mA	$V_{LP-stby}$	2.4	3.0	3.7	V
CURRENT SENSE SECTION					
Maximum Current Sense Input Threshold	V_{CS-th}	0.95	1.0	1.05	V
Input Bias Current	I_{B-cs}	−1.8	–	1.8	μA
Standby Current Sense Input Current	$I_{CS-stby}$	180	200	220	μA
Startup Phase Current Sense Input Current	$I_{CS-stup}$	180	200	220	μA
Propagation Delay (Current Sense Input to Output @ V_{TH} T MOS = 3.0 V)	$T_{PLH(In/Out)}$	–	220	–	ns
Leading Edge Blanking Duration MC44608P40	T_{LEB}	–	480	–	ns
Leading Edge Blanking Duration MC44608P75	T_{LEB}	–	250	–	ns
Leading Edge Blanking Duration MC44608P100	T_{LEB}	–	200	–	ns
Leading Edge Blanking + Propagation Delay MC44608P40	T_{DLY}	500	680	900	ns
Leading Edge Blanking + Propagation Delay MC44608P75	T_{DLY}	370	470	570	ns
Leading Edge Blanking + Propagation Delay MC44608P100	T_{DLY}	300	420	500	ns
OSCILLATOR SECTION					
Normal Operation Frequency MC44608P40	f_{osc}	36	40	44	kHz
Normal Operation Frequency MC44608P75	f_{osc}	68	75	82	kHz
Normal Operation Frequency MC44608P100	f_{osc}	90	100	110	kHz
Maximum Duty Cycle @ f = f_{osc}	d_{max}	78	82	86	%
OVERVOLTAGE SECTION					
Quick OVP Input Filtering (R_{demag} = 100 kΩ)	T_{filt}	–	250	–	ns
Propagation Delay (I_{demag} > I_{ovp} to output low)	$T_{PHL(In/Out)}$	–	2.0	–	μs
Quick OVP Current Threshold	I_{OVP}	105	120	140	μA
Protection Threshold Level on V_{CC}	V_{CC-OVP}	14.8	15.3	15.8	V
Minimum Gap Between V_{CC-OVP} and $V_{stup-th}$	$V_{CC-OVP} - V_{stup}$	1.0	–	–	V

1. This parameter is measured using 1.0 nF connected between the output and the ground.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A = −25°C to +85°C unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Typ	Max	Unit
DEMAGNETIZATION DETECTION SECTION (Note 3)					
Demag Comparator Threshold (V_{pin1} increasing)	V_{dmg-th}	30	50	69	mV
Demag Comparator Hysteresis (Note 4)	H_{dmg}	−	30	−	mV
Propagation Delay (Input to Output, Low to High)	$t_{PHL(In/Out)}$	−	300	−	ns
Input Bias Current (V_{demag} = 50 mV)	I_{dem-Ib}	−0.6	−	−	μA
Negative Clamp Level (I_{demag} = −1.0 mA)	$V_{cl-neg-dem}$	−0.9	−0.7	−0.4	V
Positive Clamp Level @ I_{demag} = 125 μA	$V_{cl-pos-dem-H}$	2.05	2.3	2.8	V
Positive Clamp Level @ I_{demag} = 25 μA	$V_{cl-pos-dem-L}$	1.4	1.7	1.9	V
OVERTEMPERATURE SECTION					
Trip Level Over Temperature	T_{high}	−	160	−	°C
Hysteresis	T_{hyst}	−	30	−	°C
STANDBY MAXIMUM CURRENT REDUCTION SECTION					
Normal Mode Recovery Demag Pin Current Threshold	I_{dem-NM}	20	25	30	μA
K FACTORS SECTION FOR PULSED MODE OPERATION					
I_{CCS} / I_{stup} MC44608P40	10 x K1	2.4	2.9	3.8	−
I_{CCS} / I_{stup} MC44608P75	10 x K1	2.8	3.3	4.2	−
I_{CCS} / I_{stup} MC44608P100	10 x K1	3.1	7.0	4.5	−
I_{CCL} / I_{stup}	10^3 x K2	46	52	63	−
(V_{stup} − UVLO2) / (V_{stup} − UVLO1)	10^2 x K_{sstup}	1.8	2.2	2.6	−
(UVLO1 − UVLO2) / (V_{stup} − UVLO1)	10^2 x K_{sl}	90	120	150	−
I_{CS} / V_{csth}	10^6 x Y_{cstby}	175	198	225	−
Demag ratio I_{ovp} / I_{dem} NM	Dmgr	3.0	4.7	5.5	−
($V3_{1.0\ mA}$ − $V3_{0.5\ mA}$) / (1.0 mA − 0.5 mA)	R3	−	1800	−	Ω
$V_{control}$ Latchoff	V3	−	4.8	−	V
SUPPLY SECTION					
Minimum Startup Voltage	V_{ilow}	−	−	50	V
V_{CC} Startup Voltage	$V_{stup-th}$	12.5	13.1	13.8	V
Output Disabling V_{CC} Voltage After Turn On	V_{uvlo1}	9.5	10	10.5	V
Hysteresis ($V_{stup-th}$ − V_{uvlo1})	$H_{stup-uvlo1}$	−	3.1	−	V
V_{CC} Undervoltage Lockout Voltage	V_{uvlo2}	6.2	6.6	7.0	V
Hysteresis (V_{uvlo1} − V_{uvlo2})	$H_{uvlo1-uvlo2}$	−	3.4	−	V
Absolute Normal Condition V_{CC} Start Current @ (V_i = 100 V) and (V_{CC} = 9.0 V)	−(I_{CC})	7.0	9.5	12.8	mA
Switching Phase Supply Current (no load) MC44608P40 MC44608P75 MC44608P100	I_{CCS}	2.0 2.4 2.6	2.6 3.2 3.4	3.6 4.0 4.5	mA
Latched Off Phase Supply Current	$I_{CC-latch}$	0.3	0.5	0.68	mA
Hiccup Mode Duty Cycle (no load)	δ_{Hiccup}	−	10	−	%

2. Adjust V_{CC} above the startup threshold before setting to 12 V. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. This function can be inhibited by connecting pin 1 to GND.
4. Guaranteed by design (non tested).

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	Demag	The Demag pin offers 3 different functions: Zero voltage crossing detection (50 mV), 24 μA current detection and 120 μA current detection. The 24 μA level is used to detect the secondary reconfiguration status and the 120 μA level to detect an Over Voltage status called Quick OVP.
2	I_{sense}	The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the power MOSFET. When I_{sense} reaches 1.0 V, the Driver output (pin 5) is disabled. This is known as the Over Current Protection function. A 200 μA current source is flowing out of the pin 3 during the startup phase and during the switching phase in case of the Pulsed Mode of operation. A resistor can be inserted between the sense resistor and the pin 2, thus a programmable peak current detection can be performed during the SMPS standby mode.
3	Control Input	A feedback current from the secondary side of the SMPS via the Opto−coupler is injected into this pin. A resistor can be connected between this pin and GND to allow the programming of the Burst duty cycle during the standby mode.
4	Ground	This pin is the ground of the primary side of the SMPS.
5	Driver	The current and slew rate capability of this pin are suited to drive Power MOSFETs.
6	V_{CC}	This pin is the positive supply of the IC. The driver output gets disabled when the voltage becomes higher than 15 V and the operating range is between 6.6 V and 13 V. An intermediate voltage level of 10 V creates a disabling condition called Latched Off phase.
7		This pin is to provide isolation between the V_i pin 8 and the V_{CC} pin 6.
8	V_i	This pin can be directly connected to a 500 V voltage source for startup function of the IC. During the startup phase a 9.0 mA current source is internally delivered to the V_{CC} pin 6 allowing a rapid charge of the V_{CC} capacitor. As soon as the IC starts−up, this current source is disabled.

OPERATING DESCRIPTION

Regulation

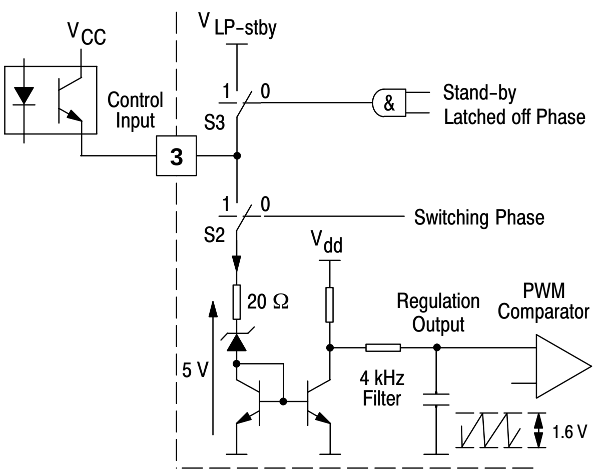


Figure 2. Regulator

The pin 3 senses the feedback current provided by the Opto coupler. During the switching phase the switch S2 is closed and the shunt regulator is accessible by the pin 3. The shunt regulator voltage is typically 5.0 V. The dynamic resistance of the shunt regulator represented by the zener diode is 20 Ω. The gain of the Control input is given on Figure 11 which shows the duty cycle as a function of the current injected into the pin 3.

A 4.0 kHz filter network is inserted between the shunt regulator and the PWM comparator to cancel the high frequency residual noise.

The switch S3 is closed in standby mode during the Latched Off Phase while the switch S2 remains open. (See section PULSED MODE DUTY CYCLE CONTROL).

The resistor Rdpulsed (Rduty cycle burst) has no effect on the regulation process. This resistor is used to determine the burst duty cycle described in the chapter “Pulsed Duty Cycle Control” on page 8.

PWM Latch

The MC44608 works in voltage mode. The on−time is controlled by the PWM comparator that compares the oscillator sawtooth with the regulation block output (refer to the block diagram on page 2).

The PWM latch is initialized by the oscillator and is reset by the PWM comparator or by the current sense comparator in case of an over current. This configuration ensures that only a single pulse appears at the circuit output during an oscillator cycle.

Current Sense

The inductor current is converted to a positive voltage by inserting a ground reference sense resistor R_{Sense} in series with the power switch.

The maximum current sense threshold is fixed at 1.0 V. The peak current is given by the following equation:

$$Ipk_{max} = \frac{1}{R_{sense}(\Omega)}(A)$$

In standby mode, this current can be lowered as due to the activation of a 200 μA current source:

$$Ipk_{max-stby} = \frac{1 - (R_{CS}(k\Omega) \times 0,2)}{R_{sense}(\Omega)} (A)$$

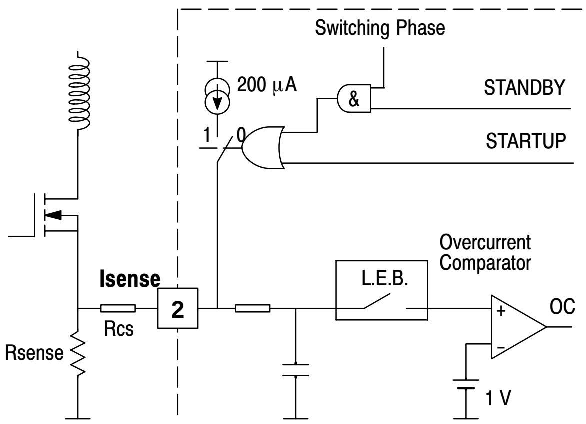


Figure 3. Current Sense

The current sense input consists of a filter (6.0 kΩ, 4.0 pF) and of a leading edge blanking. Thanks to that, this pin is not sensitive to the power switch turn on noise and spikes and practically in most applications, no filtering network is required to sense the current.

Finally, this pin is used:

− as a protection against over currents (Isense > I)

− as a reduction of the peak current during a Pulsed Mode switching phase.

The overcurrent propagation delay is reduced by producing a sharp output turn off (high slew rate). This results in an abrupt output turn off in the event of an over current and in the majority of the pulsed mode switching sequence.

Demagnetization Section

The MC44608 demagnetization detection consists of a comparator designed to compare the V_{CC} winding voltage to a reference that is typically equal to 50 mV.

This reference is chosen low to increase effectiveness of the demagnetization detection even during startup.

A latch is incorporated to turn the demagnetization block output into a low level as soon as a voltage less than 50 mV is detected, and to keep it in this state until a new pulse is generated on the output. This avoids any ringing on the input signal which may alter the demagnetization detection.

For a higher safety, the demagnetization block output is also directly connected to the output, which is disabled during the demagnetization phase.

The demagnetization pin is also used for the quick, programmable OVP. In fact, the demagnetization input current is sensed so that the circuit output is latched off when this current is detected as higher than 120 μA.

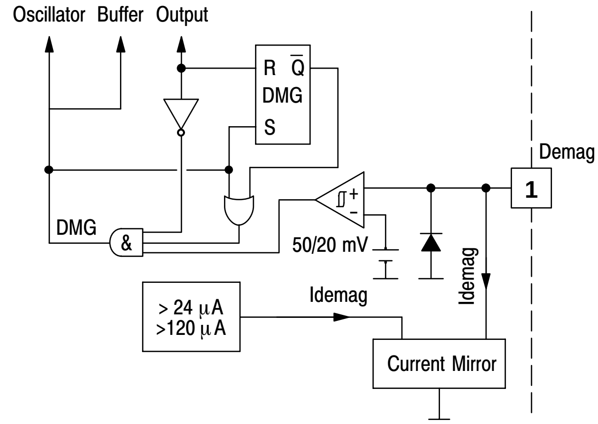


Figure 4. Demagnetization Block

This function can be inhibited by grounding it but in this case, the quick and programmable OVP is also disabled.

Oscillator

The MC44608 contains a fixed frequency oscillator. It is built around a fixed value capacitor CT successively charged and discharged by two distinct current sources ICH and IDCH. The window comparator senses the CT voltage value and activates the sources when the voltage is reaching the 2.4 V/4.0 V levels.

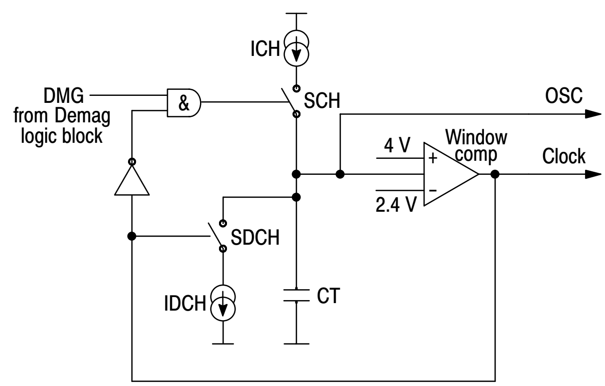


Figure 5. Oscillator Block

The complete demagnetization status DMG is used to inhibit the recharge of the CT capacitor. Thus in case of incomplete transformer demagnetization the next switching cycle is postpone until the DMG signal appears. The oscillator remains at 2.4 V corresponding to the sawtooth valley voltage. In this way the SMPS is working in the so called SOPS mode (Self Oscillating Power Supply). In that case the effective switching frequency is variable and no longer depends on the oscillator timing but on the external working conditions (Refer to DMG signal in the Figure 6).

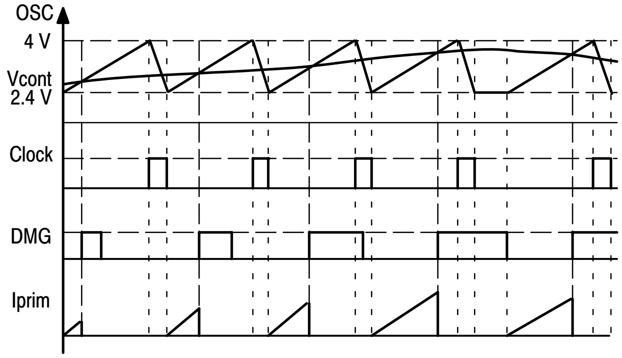


Figure 6.

The OSC and Clock signals are provided according to the Figure 6. The Clock signals correspond to the CT capacitor discharge. The bottom curve represents the current flowing in the sense resistor Rcs. It starts from zero and stops when the sawtooth value is equal to the control voltage Vcont. In this way the SMPS is regulated with a voltage mode control.

Overvoltage Protection

The MC44608 offers two OVP functions:

− a fixed function that detects when V_{CC} is higher than 15.4 V

− a programmable function that uses the demag pin. The current flowing into the demag pin is mirrored and compared to the reference current Iovp (120 μA). Thus this OVP is quicker as it is not impacted by the V_{CC} inertia and is called QOVP.

In both cases, once an OVP condition is detected, the output is latched off until a new circuit startup.

Startup Management

The V_i pin 8 is directly connected to the HV DC rail Vin. This high voltage current source is internally connected to the V_{CC} pin and thus is used to charge the V_{CC} capacitor. The V_{CC} capacitor charge period corresponds to the startup phase. When the V_{CC} voltage reaches 13 V, the high voltage 9.0 mA current source is disabled and the device starts working. The device enters into the switching phase.

It is to be noticed that the maximum rating of the V_i pin 8 is 500 V. ESD protection circuitry is not currently added to this pin due to size limitations and technology constraints. Protection is limited by the drain−substrate junction in avalanche breakdown. To help increase the application safety against high voltage spike on that pin it is possible to insert a small wattage 1.0 kΩ series resistor between the V_{in} rail and pin 8.

The Figure 7 shows the V_{CC} voltage evolution in case of no external current source providing current into the V_{CC} pin during the switching phase. This case can be encountered in SMPS when the self supply through an auxiliary winding is not present (strong overload on the SMPS output for example). The Figure 17 also depicts this working configuration.

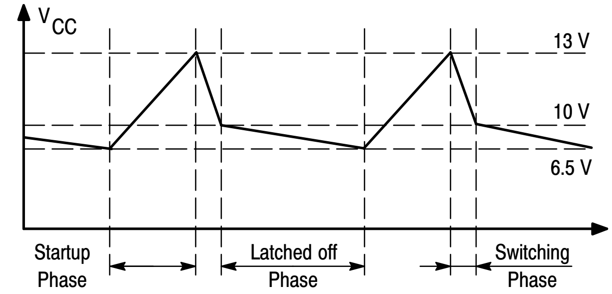


Figure 7. Hiccup Mode

In case of the hiccup mode, the duty cycle of the switching phase is in the range of 10%.

Mode Transition

The LW latch Figure 8 is the memory of the working status at the end of every switching sequence.

Two different cases must be considered for the logic at the termination of the SWITCHING PHASE:

1. No Over Current was observed
2. An Over Current was observed

These 2 cases are corresponding to the signal labelled NOC in case of “No Over Current” and “OC” in case of Over Current. So the effective working status at the end of the ON time memorized in LW corresponds to Q=1 for no over current and Q=0 for over current.

This sequence is repeated during the Switching phase.

Several events can occur:

1. SMPS switch OFF
2. SMPS output overload
3. Transition from Normal to Pulsed Mode
4. Transition from Pulsed Mode to Normal Mode

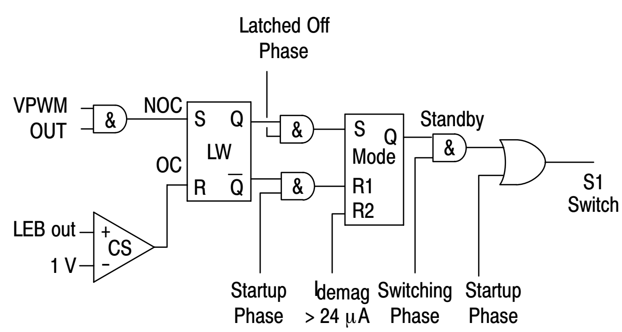


Figure 8. Transition Logic

- **1. SMPS SWITCH OFF**

When the mains is switched OFF, so long as the bulk electrolithic bulk capacitor provides energy to the SMPS, the controller remains in the switching phase. Then the peak current reaches its maximum peak value, the switching frequency decreases and all the secondary voltages are reduced. The V_{CC} voltage is also reduced. When V_{CC} is equal to 10 V, the SMPS stops working.

- **2. Overload**

In the hiccup mode the 3 distinct phases are described as follows (refer to Figure 7):

The SWITCHING PHASE: The SMPS output is low and the regulation block reacts by increasing the ON time (dmax = 80%). The OC is reached at the end of every switching cycle. The LW latch (Figure 8) is reset before the VPWM signal appears. The SMPS output voltage is low. The V_{CC} voltage cannot be maintained at a normal level as the auxiliary winding provides a voltage which is also reduced in a ratio similar to the one on the output (i.e. Vout nominal / Vout short−circuit). Consequently the V_{CC} voltage is reduced at an operating rate given by the combination V_{CC} capacitor value together with the I_{CC} working consumption (3.2 mA) according to the equation 2. When V_{CC} crosses 10V the WORKING PHASE gets terminated. The LW latch remains in the reset status.

The LATCHED−OFF PHASE: The V_{CC} capacitor voltage continues to drop. When it reaches 6.5 V this phase is terminated. Its duration is governed by equation 3.

The startup PHASE is reinitiated. The high voltage startup current source ($-I_{CC1}$ = 9.0 mA) is activated and the MODE latch is reset. The V_{CC} voltage ramps up according to the equation 1. When it reaches 13 V, the IC enters into the SWITCHING PHASE.

The NEXT SWITCHING PHASE: The high voltage current source is inhibited, the MODE latch (Q=0) activates the NORMAL mode of operation. Figure 3 shows that no current is injected out pin 2. The over current sense level corresponds to 1.0 V.

As long as the overload is present, this sequence repeats. The SWITCHING PHASE duty cycle is in the range of 10%.

- **3. Transition from Normal to Pulsed Mode**

In this sequence the secondary side is reconfigured (refer to the typical application schematic on page 13). The high voltage output value becomes lower than the NORMAL mode regulated value. The TL431 shunt regulator is fully OFF. In the SMPS standby mode all the SMPS outputs are lowered except for the low voltage output that supply the wake−up circuit located at the isolated side of the power supply. In that mode the secondary regulation is performed by the zener diode connected in parallel to the TL431.

The secondary reconfiguration status can be detected on the SMPS primary side by measuring the voltage level present on the auxiliary winding Laux. (Refer to the Demagnetization Section). In the reconfigured status, the Laux voltage is also reduced. The V_{CC} self−powering is no longer possible thus the SMPS enters in a hiccup mode similar to the one described under the Overload condition.

In the SMPS standby mode the 3 distinct phases are:

The SWITCHING PHASE: Similar to the Overload mode. The current sense clamping level is reduced according to the equation of the current sense section, page 5. The C.S. clamping level depends on the power to be delivered to the load during the SMPS standby mode. Every switching sequence ON/OFF is terminated by an OC as long as the secondary Zener diode voltage has not been reached. When the Zener voltage is reached the ON cycle is terminated by a true PWM action. The proper SWITCHING PHASE termination must correspond to a NOC condition. The LW latch stores this NOC status.

The LATCHED OFF PHASE: The MODE latch is set.

The startup PHASE is similar to the Overload Mode. The MODE latch remains in its set status (Q=1).

The SWITCHING PHASE: The standby signal is validated and the 200 μA is sourced out of the Current Sense pin 2.

- **4. Transition from Standby to Normal**

The secondary reconfiguration is removed. The regulation on the low voltage secondary rail can no longer be achieved, thus at the end of the SWITCHING PHASE, no PWM condition can be encountered. The LW latch is reset.

At the next WORKING PHASE a NORMAL mode status takes place.

In order to become independent of the recovery time constant on the secondary side of the SMPS an additional reset input R2 is provided on the MODE latch. The condition Idemag<24 μA corresponds to the activation of the secondary reconfiguration status. The R2 reset insures a direct return into the Normal Mode.

Pulsed Mode Duty Cycle Control

During the sleep mode of the SMPS the switch S3 is closed and the control input pin 3 is connected to a 4.6 V voltage source thru a 500 Ω resistor. The discharge rate of the V_{CC} capacitor is given by $I_{CC-latch}$ (device consumption during the LATCHED OFF phase) in addition to the current drawn out of the pin 3. Connecting a resistor between the Pin 3 and GND ($R_{DPULSED}$) a programmable current is drawn from the V_{CC} through pin 3. The duration of the LATCHED OFF phase is impacted by the presence of the resistor $R_{DPULSED}$. The equation 3 shows the relation to the pin 3 current.

Pulsed Mode Phases

Equations 1 through 8 define and predict the effective behavior during the PULSED MODE operation. The equations 6, 7, and 8 contain K, Y, and D factors. These factors are combinations of measured parameters. They appear in the parameter section “Kfactors for pulsed mode operation” page 4. In equations 3 through 8 the pin 3 current is the current defined in the above section “Pulsed Mode Duty Cycle Control”.

EQUATION 1

Startup Phase Duration:

$$t_{start–up} = \frac{C_{Vcc} \times (V_{stup} - UVLO2)}{I_{stup}}$$

where: I_{stup} is the startup current flowing through V_{CC} pin
C_{Vcc} is the V_{CC} capacitor value

EQUATION 2

Switching Phase Duration:

$$t_{switch} = \frac{C_{Vcc} \times (V_{stup} - UVLO1)}{I_{ccS} + I_G}$$

where: I_{ccS} is the no load circuit consumption in switching phase
I_G is the current consumed by the Power Switch

EQUATION 3

Latched−off Phase Duration:

$$t_{latched-off} = \frac{C_{Vcc} \times (UVLO1 - UVLO2)}{I_{ccL} + I_{pin3}}$$

where: I_{ccL} is the latched off phase consumption
I_{pin3} is the current drawn from pin3 adding a resistor

EQUATION 4

Burst Mode Duty Cycle:

$$d_{BM} = \frac{t_{switch}}{t_{start-up} + t_{switch} + t_{latched-off}}$$

EQUATION 5

$$d_{BM} = \frac{\dfrac{C_{Vcc} \times (V_{stup} - UVLO1)}{I_{ccS} + I_G}}{\dfrac{C_{Vcc} \times (V_{stup} - UVLO2)}{I_{stup}} + \dfrac{C_{Vcc} \times (V_{stup} - UVLO1)}{I_{ccS} + I_G} + \dfrac{C_{Vcc} \times (UVLO1 - UVLO2)}{I_{ccL} + I_{pin3}}}$$

EQUATION 6

$$d_{BM} = \frac{1}{1 + \left(k_{S/Stup} \times \dfrac{I_{ccS} + I_G}{I_{stup}}\right) + \left(k_{S/L} \times \dfrac{I_{ccS} + I_G}{I_{ccL} + I_{pin3}}\right)}$$

where: $k_{S/Stup} = (V_{stup} - UVLO2)/(V_{stup} - UVLO1)$
$k_{S/L} = (UVLO1 - UVLO2)/(V_{stup} - UVLO1)$

EQUATION 7

$$d_{BM} = \frac{1}{1 + \left[\frac{I_{ccS} + I_G}{I_{stup}} \times \left(k_{S/Stup} + \left(k_{S/L} \times \frac{I_{stup}}{I_{ccL} + I_{pin3}}\right)\right)\right]}$$

EQUATION 8

$$d_{BM} = \frac{1}{1 + \left\{\left(k1 + \frac{I_G}{I_{stup}}\right) \times \left[k_{S/Stup} + (k_{S/L} \times \frac{1}{k2 + \left(\frac{I_{pin3}}{I_{stup}}\right)})\right]\right\}}$$

where: $k1 = I_{ccs}/I_{stup}$
$k2 = I_{ccL}/I_{stup}$
$k_{S/Stup} = (V_{stup}-UVLO2)/(V_{stup}-UVLO1)$
$k_{S/L} = (UVLO1-UVLO2)/(V_{stup}-UVLO1)$

PULSED MODE CURRENT SENSE CLAMPING LEVEL

Equations 9, 10, 11 and 12 allow the calculation of the Rcs value for the desired maximum current peak value during the SMPS standby mode.

EQUATION 9

$$Ipk_{stby} = \frac{V_{cs-th} - (R_{cs} \times I_{cs})}{R_S}$$

where: V_{cs-th} is the CS comparator threshold
I_{cs} is the CS internal current source
R_S is the sensing resistor
R_{cs} is the resistor connected between pin 2 and R_S

EQUATION 10

$$Ipk_{stby} = V_{cs-th} \times \frac{1 - \left(R_{cs} \times \frac{I_{cs}}{V_{cs-th}}\right)}{R_S}$$

EQUATION 11

$$Ipk_{stby} = V_{cs-th} \times \frac{1 - (R_{cs} \times Y_{cs-stby})}{R_S}$$

where: $Y_{cs-stby} = I_{cs}/V_{cs-th}$
Taking into account the circuit propagation delay (δt_{cs}) and the Power Switch reaction time (δt_{ps}):

EQUATION 12

$$Ipk_{stby} = \left[V_{cs-th} \times \frac{1 - (R_{cs} \times Y_{cs-stby})}{R_S}\right] + \frac{V_{in} \times (\delta t_{cs} + \delta t_{ps})}{L_p}$$

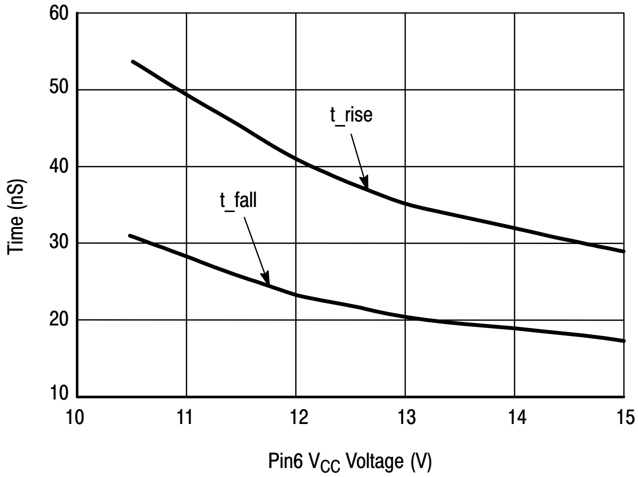


Figure 9. Output Switching Speed

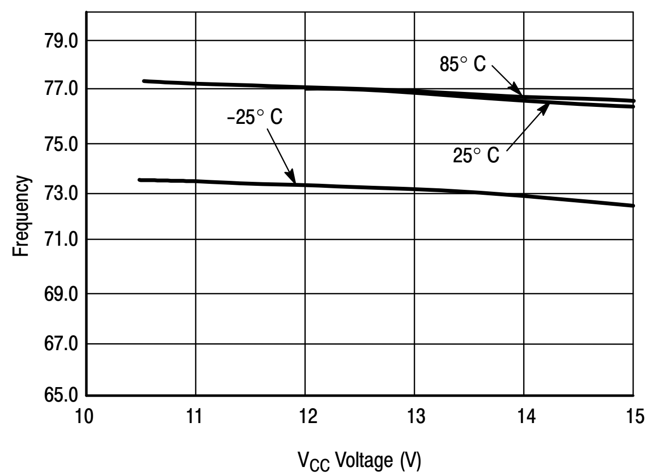


Figure 10. Frequency Stability

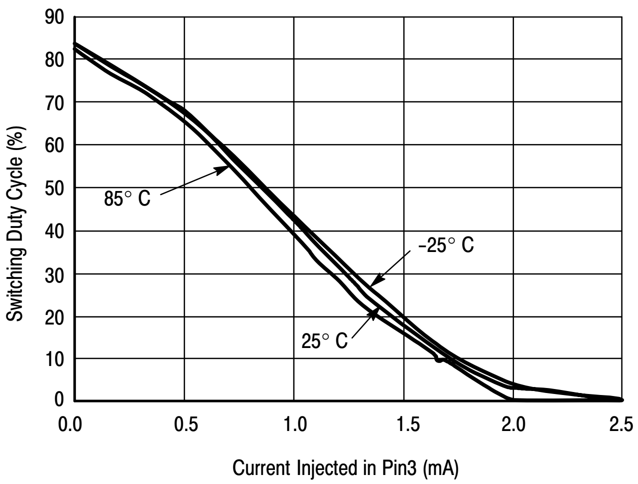


Figure 11. Duty Cycle Control

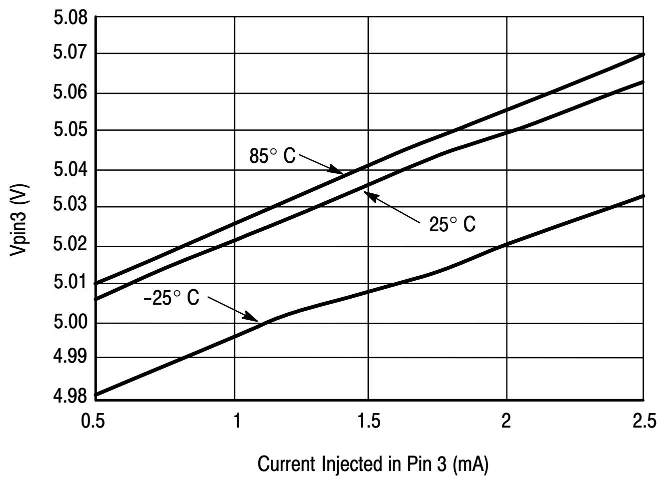


Figure 12. Vpin3 During the Working Period

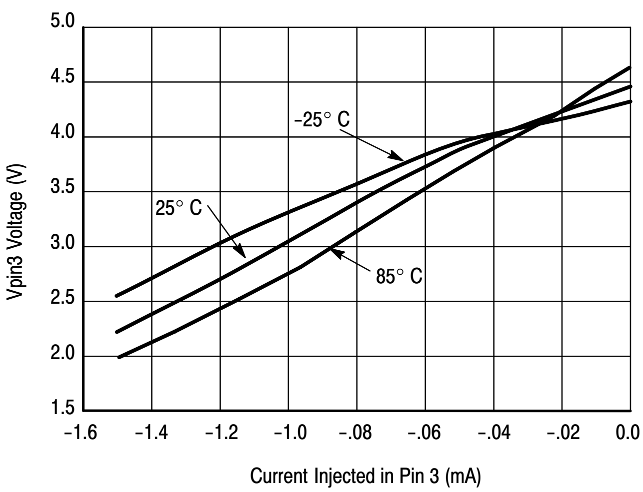


Figure 13. Vpin3 During the Latched Off Period

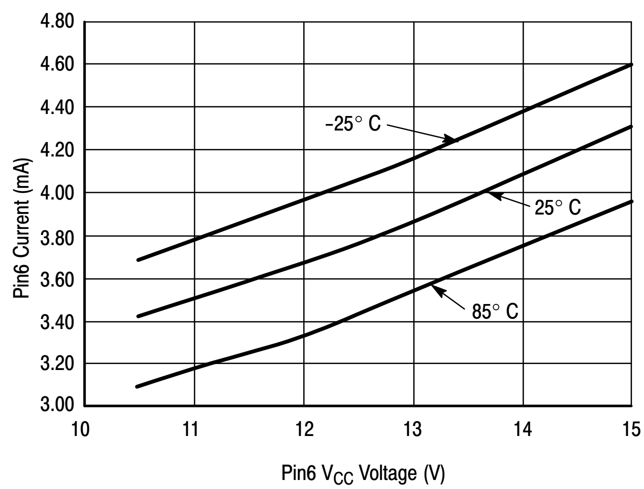


Figure 14. Device Consumption when Switching

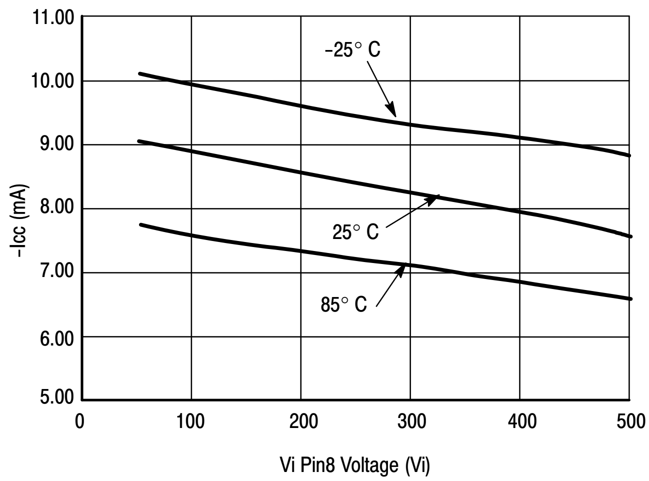


Figure 15. High Voltage Current Source

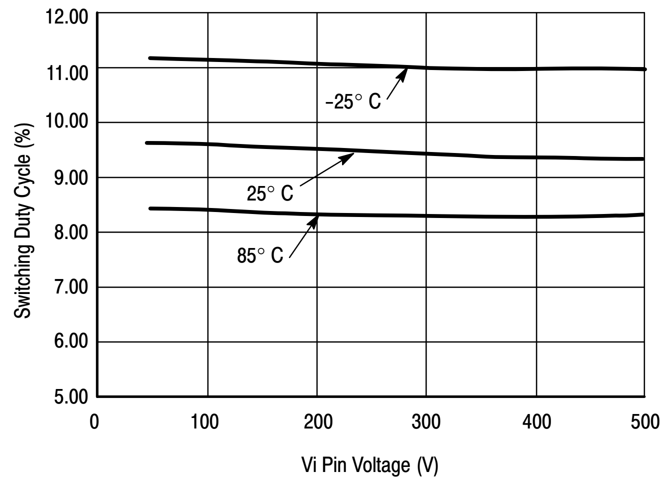


Figure 16. Overload Burst Mode

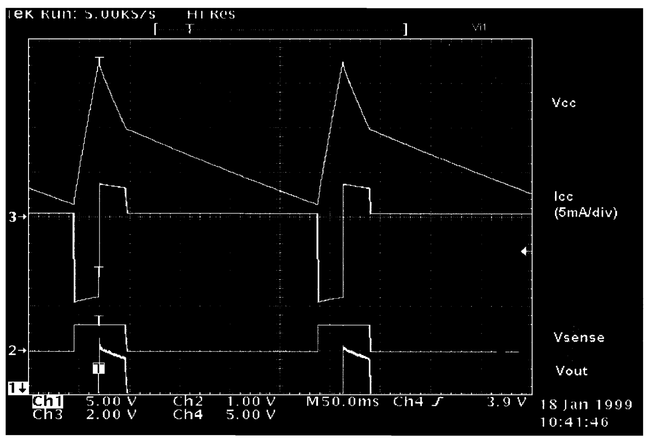


Figure 17. Hiccup Mode Waveforms

The data in Figure 16 corresponds to the waveform in Figure 17. The Figure 17 shows V_{CC}, I_{CC}, I_{sense} (pin 2) and V_{out} (pin 5). V_{out} (pin 5) in fact shows the envelope of the output switching pulses. This mode corresponds to an overload condition.

The Figure 19 represents a complete power supply using the secondary reconfiguration.

The specification is as follows:	Input source:	85 Vac to 265 Vac
	3 Outputs	112 V/0.45 A
		16 V/1.5 A
		8.0 V/1.0 A
	Output power	80 W
	Standby mode	@ Pout = 300 mW, 1.3 W

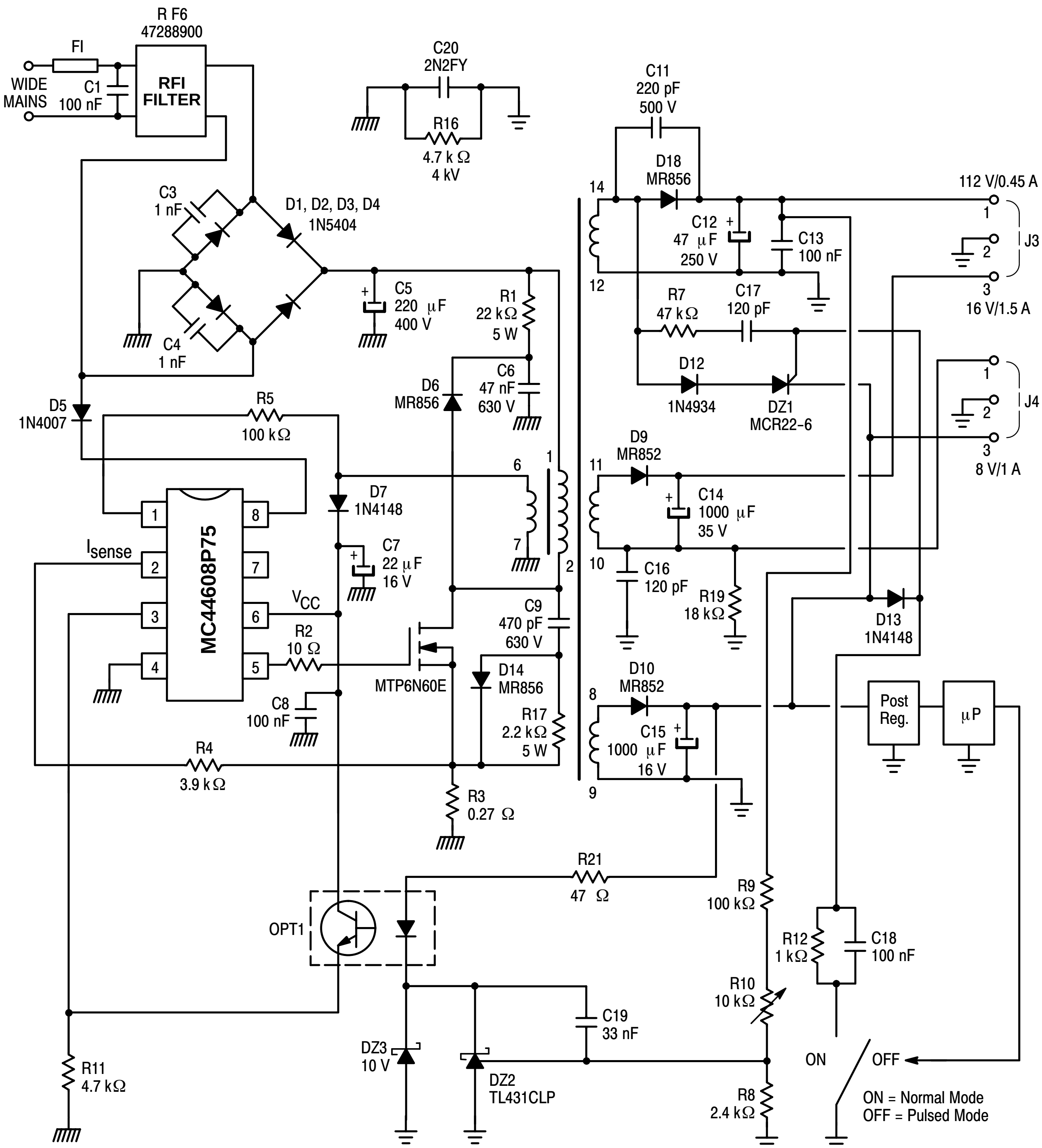


Figure 18. Typical Application

The secondary reconfiguration is activated by the µP through the switch. The dV/dt appearing on the high voltage winding (pins 14 of the transformer) at every TMOS switch off, produces a current spike through the series RC network R7, C17. According to the switch position this spike is either absorbed by the ground (switch closed) or flows into the thyristor gate (switch open) thus firing the MCR22−6. The closed position of the switch corresponds to the Pulsed Mode activation. In this secondary side SMPS status the high voltage winding (12−14) is connected through D12 and DZ1 to the 8.0 V low voltage secondary rail. The voltages applied to the secondary windings 12−14, 10−11 and 6−7 (Vaux) are thus divided by ratio N12−14 / N9−8 (number of turns of the winding 12−14 over number of turns of the winding 9−8). In this reconfigured status all the secondary voltages are lowered except the 8.0 V one. The regulation during every pulsed or burst is performed by the zener diode DZ3 which value has to be chosen higher than the normal mode regulation level. This working mode creates a voltage ripple on the 8.0 V rail which generally must be post regulated for the microProcessor supply.

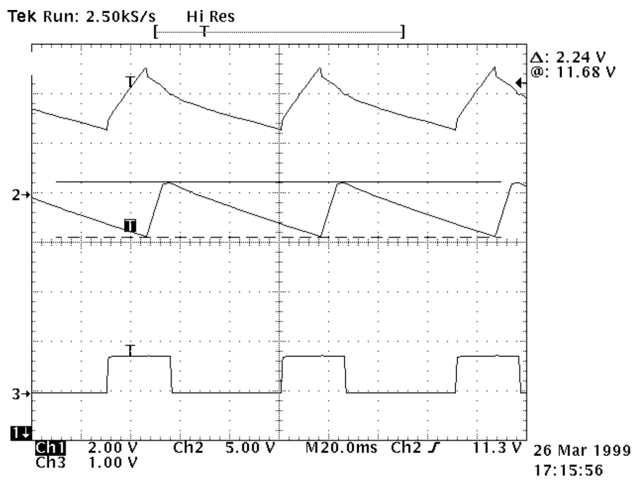
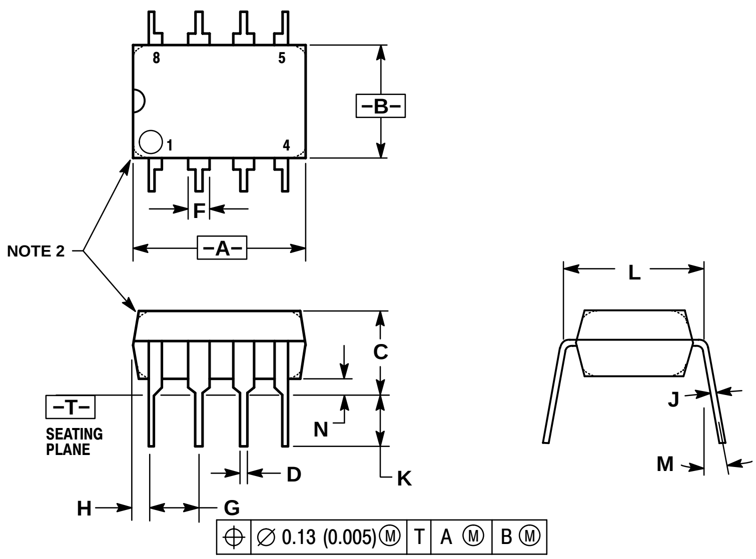


Figure 19. SMPS Pulsed Mode

The Figure 19 shows the SMPS behavior while working in the reconfigured mode. The top curve represents the V_{CC} voltage (pin 6 of the MC44608). The middle curve represents the 8.0 V rail. The regulation is taking place at 11.68 V. On the bottom curve the pin 2 voltage is shown. This voltage represents the current sense signal. The pin 2 voltage is the result of the 200 µA current source activated during the startup phase and also during the working phase which flows through the R4 resistor. The used high resolution mode of the oscilloscope does not allow to show the effective ton current flowing in the sensing resistor R11.

PACKAGE DIMENSIONS

PDIP−8
P SUFFIX
PLASTIC PACKAGE
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

The product described herein (MC44608), may be covered by one or more of the following U.S. patents: 6,208,538 B1; 6,392,906 B2. There may be other patents pending.

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