

# MC74LVX08

## Quad 2-Input NAND Gate

### With 5 V-Tolerant Inputs

The MC74LVX08 is an advanced high speed CMOS 2-input AND gate. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

#### Features

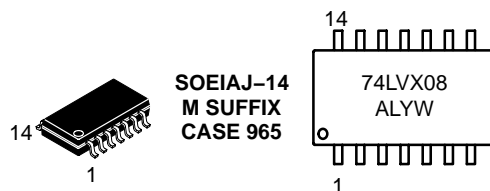
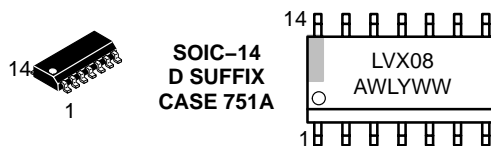
- High Speed:  $t_{PD} = 4.8$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 2$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Pb-Free Packages are Available\*



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#### MARKING DIAGRAMS



A = Assembly Location  
WL or L = Wafer Lot  
Y = Year  
WW or W = Work Week

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74LVX08

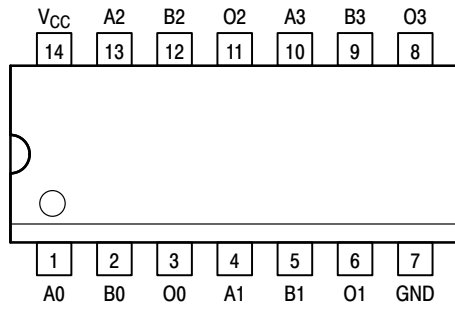


Figure 1. 14-Lead Pinout (Top View)

## PIN NAMES

Pins	Function
An, Bn On	Data Inputs Outputs

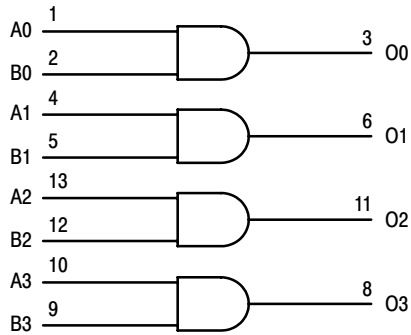


Figure 2. Logic Diagram

## FUNCTION TABLE

INPUTS		OUTPUTS
An	Bn	On
L	L	L
L	H	L
H	L	L
H	H	H

## ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX08DR2	SOIC-14	2500 Tape & Reel
MC74LVX08DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LVX08DT	TSSOP-14*	96 Units / Rail
MC74LVX08DTR2	TSSOP-14*	2500 Tape & Reel
MC74LVX08M	SOEIAJ-14	50 Units / Rail
MC74LVX08MG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC74LVX08MEL	SOEIAJ-14	2000 Tape & Reel
MC74LVX08MELG	SOEIAJ-14 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74LVX08

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage	-0.5 to +7.0	V
$V_{out}$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Diode Current	-20	mA
$I_{OK}$	Output Diode Current	±20	mA
$I_{out}$	DC Output Current, per Pin	±25	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	±50	mA
$P_D$	Power Dissipation	180	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	2.0	3.6	V
$V_{in}$	DC Input Voltage	0	5.5	V
$V_{out}$	DC Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	$V_{CC}$ V	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
$V_{IH}$	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.0			2.0		
			3.6	2.4			2.4		
$V_{IL}$	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.8		0.8	
			3.6			0.8		0.8	
$V_{OH}$	High-Level Output Voltage ( $V_{in} = V_{IH}$ or $V_{IL}$ )	$I_{OH} = -50 \mu\text{A}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{ mA}$	2.0	1.9	2.0		1.9		V
			3.0	2.9	3.0		2.9		
			3.0	2.58			2.48		
$V_{OL}$	Low-Level Output Voltage ( $V_{in} = V_{IH}$ or $V_{IL}$ )	$I_{OL} = 50 \mu\text{A}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 4 \text{ mA}$	2.0		0.0	0.1		0.1	V
			3.0		0.0	0.1		0.1	
			3.0			0.36		0.44	
$I_{in}$	Input Leakage Current	$V_{in} = 5.5 \text{ V}$ or GND	3.6			±0.1		±1.0	μA
$I_{CC}$	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			2.0		20.0	μA

# MC74LVX08

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40$ to $85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay, Input to Output	$V_{CC} = 2.7\text{V}$ $C_L = 15$ pF		6.3	11.4	1.0	13.5	ns
		$C_L = 50$ pF		8.8	14.9	1.0	17.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15$ pF		4.8	7.1	1.0	8.5	
		$C_L = 50$ pF		7.3	10.6	1.0	12.0	
$t_{OSHL}$ $t_{OSLH}$	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7\text{V}$ $C_L = 50$ pF $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50$ pF			1.5		1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40$ to $85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
$C_{in}$	Input Capacitance		4	10		10	pF
$C_{PD}$	Power Dissipation Capacitance (Note 2)		18				pF

2.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$  (per gate).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.3	0.5	V
$V_{QLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.3	-0.5	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

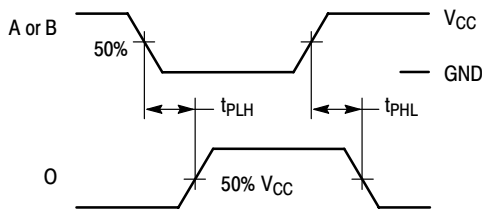
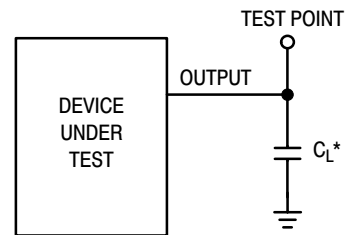


Figure 3. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 4. Test Circuit

# MC74LVX08

## PACKAGE DIMENSIONS

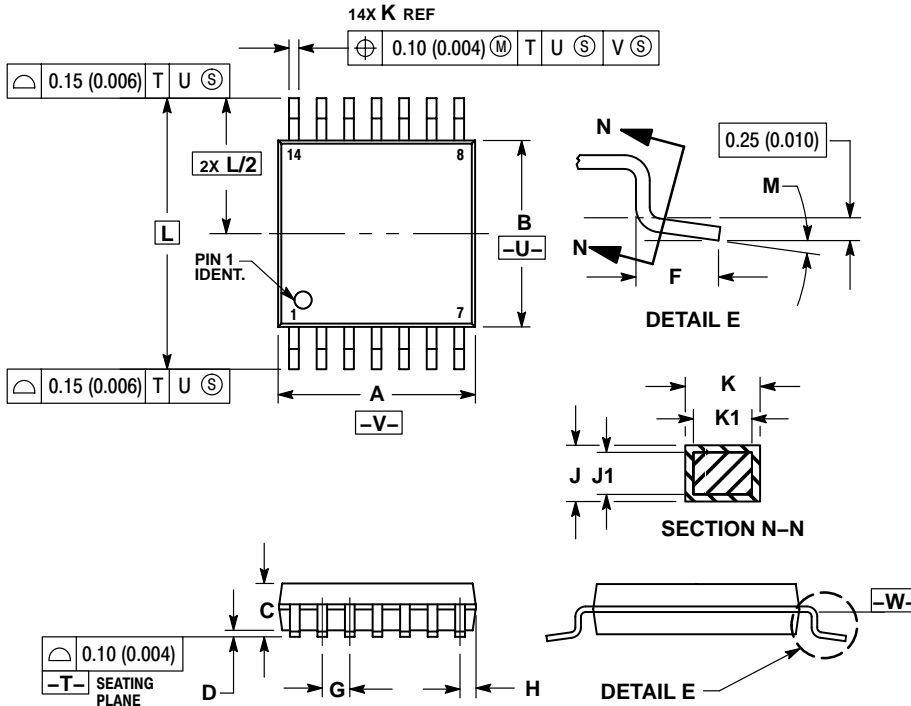
**SOIC-14**  
**D SUFFIX**  
CASE 751A-03  
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

**TSSOP-14**  
**DT SUFFIX**  
CASE 948G-01  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# MC74LVX08

## PACKAGE DIMENSIONS

SOEIAJ-14  
M SUFFIX  
CASE 965-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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