P3P2043B

LCD Panel EMI Reduction IC

ON Semiconductor®

http://onsemi.com

Product Description

The P3P2043B is a versatile spread spectrum frequency modulator designed specifically for digital flat panel applications. The P3P2043B reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P3P2043B allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The P3P2043B uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The P3P2043B modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

Features

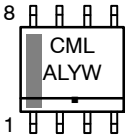
- FCC Approved Method of EMI Attenuation
- Provides Up to 15 dB of EMI Suppression
- Generates a Low EMI Spread Spectrum Clock of the Input Frequency
- Input Frequency Range: 30 MHz to 110 MHz
- Optimized for 32.5 MHz, 54 MHz, 65 MHz, 74 MHz and 108 MHz Pixel Clock Frequencies
- Internal Loop Filter Minimizes External Components and Board Space
- Eight Selectable High Spread Ranges Up to ±2%
- SSON# Control Pin for Spread Spectrum Enable and Disable Options
- Low Cycle−to−Cycle Jitter
- 3.3 V ± 0.3 V Operating Range
- Low power CMOS Design
- Supports Most Mobile Graphic Accelerator and LCD Timing Controller Specifications
- Available in 8−pin SOIC Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- The P3P2043B is targeted towards digital flat panel applications for notebook PCs, palm−size PCs, office automation equipments and LCD monitors.

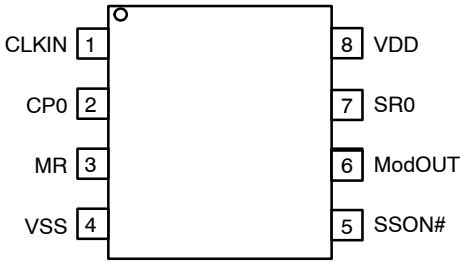
SOIC−8
CASE 751

MARKING DIAGRAMS



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

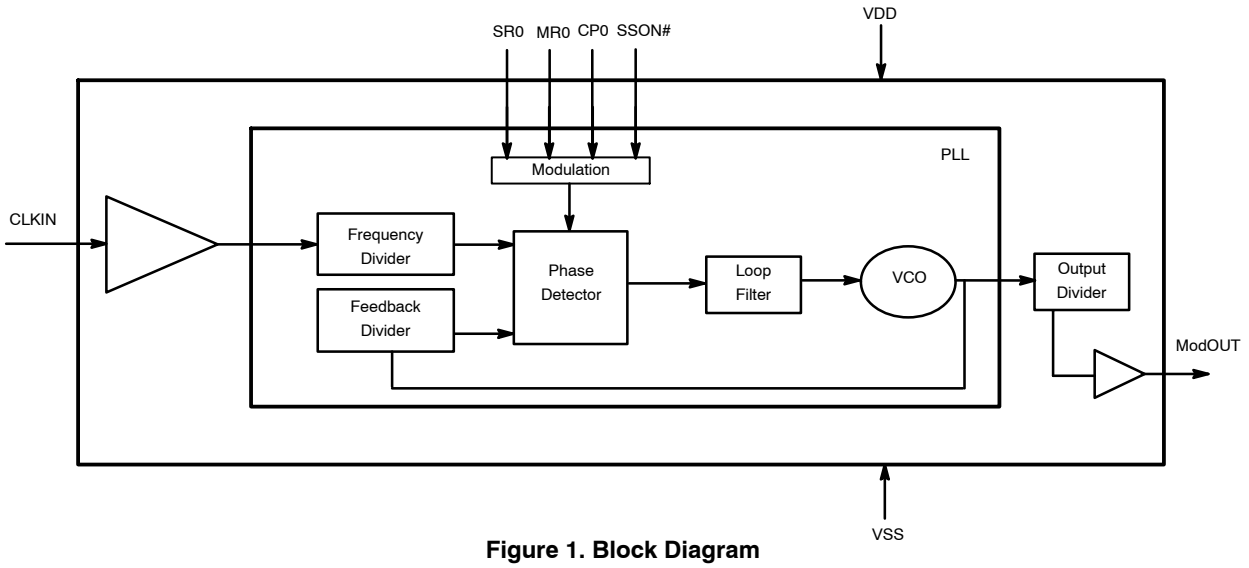


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN	Input	External reference frequency input. Connect to externally generated reference signal.
2	CP0	Input	Digital logic input used to select Spreading Range. This pin has an internal pull−up resistor. Refer *Modulation Selection Table.*
3	MR	Input	Digital logic input used to select two different Modulation Rate. This pin has an internal pull−up resistor. Refer *Modulation Selection Table.*
4	VSS	Power	Ground to entire chip. Connect to system ground.
5	SSON#	Input	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull−low resistor.
6	ModOUT	Output	Spread spectrum clock output.
7	SR0	Input	Digital logic input used to select Spreading Range. This pin has an internal pullup resistor. Refer *Modulation Selection Table.*
8	VDD	Power	Power supply for the entire chip

Table 2. MODULATION SELECTION

			Spreading Range (± %)					
MR	CP0	SR0	32.5 MHz	54 MHz	65 MHz	81 MHz	108 MHz	Modulation Rate (kHz)
0	0	0	1.47	1.19	1.08	0.96	0.88	$(F_{IN} / 40) * 94.33$
0	0	1	2.26	1.82	1.66	1.48	1.31	
0	1	0	0.75	0.59	0.55	0.50	0.46	
0	1	1	3.03	2.43	2.20	1.98	1.74	
1	0	0	1.39	1.21	1.11	0.98	0.86	$(F_{IN} / 40) * 62.89$
1	0	1	2.06	1.85	1.67	1.47	1.27	
1	1	0	0.74	0.61	0.56	0.50	0.43	
1	1	1	2.88	2.49	2.26	2.00	1.71	

Spread Spectrum Selection

The *Modulation Selection Table* defines the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency. (Note: The center frequency is the frequency of the external reference input on CLKIN, pin1).

For example, P3P2043B is designed for high−resolution, flat panel applications and is able to support an XGA (1024 x 768) flat panel operating at 65 MHz (F_{IN}) clock speed. A spreading selection of CP0 = 0, CP1 = 1 and SR0 = 0 provides a percentage deviation of $\pm 1.00\%$ from F_{IN}. This results in the frequency on ModOUT being swept from 65.65 to 64.35 MHz at a modulation rate of 102.19 kHz. *Refer Modulation Selection Table*. The example in the following illustration is a common EMI reduction method for a notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

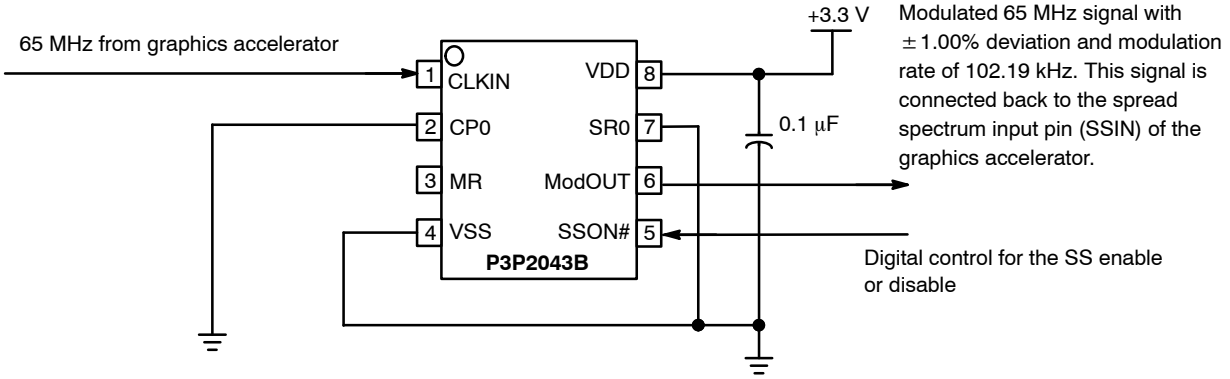


Figure 2. Application Schematic for Mobile LCD Graphics Controllers

Table 3. ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_A	Operating temperature	−40 to +85	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22−A114−B)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage with respect to Ground		3.0	3.3	3.6	V
T_A	Operating temperature		0		+70	°C
T_J	Junction temperature (0°C to +70°C)	SOIC			82.39	°C
θ_{JC}	SOIC			156.5		°C/W

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	V_{SS} − 0.3		0.8	V
V_{IH}	Input high voltage	2.0		V_{DD} + 0.3	V
I_{IL}	Input low current (pullup resistor on inputs CP0, CP1 and SR0)			−50	μA
I_{IH}	Input high current (pulldown resistor on input SSON#)			50	μA
V_{OL}	Output low voltage (I_{OL} = 8 mA)			0.4	V
V_{OH}	Output high voltage (I_{OH} = −8 mA)	2.5			V
I_{DD}	Static supply current (CLKIN pulled LOW)			300	μA
I_{CC}	Dynamic supply current (3.3 V and 10 pF loading)	6	15	22	mA
V_{DD}	Operating voltage	3.0	3.3	3.6	V
t_{ON}	Power−up time (first locked cycle after power up)			3	ms
Z_{OUT}	Clock output impedance		35		Ω

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input Clock frequency		30	74	110	MHz
f_{OUT}	Output Clock frequency		30	74	110	MHz
t_{LH}*	Output rise time (measured between 20% to 80%)		1.1	1.5	2	ns
t_{HL}*	Output fall time (measured between 80% to 20%)		0.8	1.2	1.8	ns
t_{JC}	Jitter (cycle−to−cycle)	< 50 MHz			±250	ps
		≥ 50 MHz			±200	
t_D	Output duty cycle		45	50	55	%

*t_{LH} and t_{HL} are measured into a capacitive load of 10 pF.

ORDERING INFORMATION

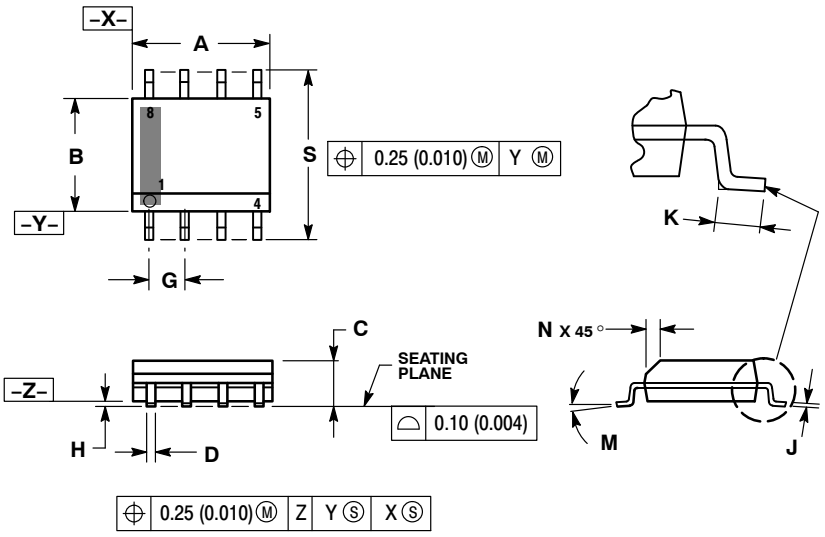
Part Number	Top Marking	Temperature	Package Type	Shipping†
P3P2043BG−08SR	CML	0°C to +70°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

PACKAGE DIMENSIONS

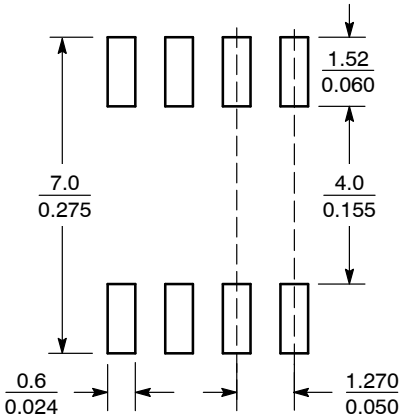
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative