

MC74LCX374

Low-Voltage CMOS Octal D-Type Flip-Flop

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX374 is a high performance, non-inverting octal D-type flip-flop operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX374 inputs to be safely driven from 5 V devices.

The MC74LCX374 consists of 8 edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable (\overline{OE}) are common to all flip-flops. The eight flip-flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the \overline{OE} LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. The \overline{OE} input level does not affect the operation of the flip-flops.

Features

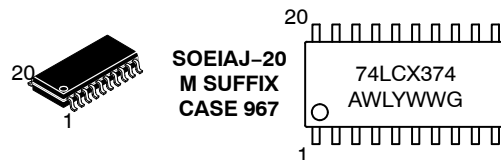
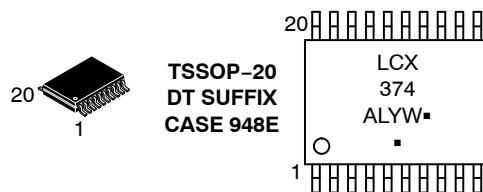
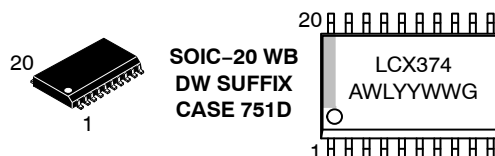
- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μ A)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
 - ◆ Human Body Model >2000 V
 - ◆ Machine Model >200 V
- These Devices are Pb-Free and are RoHS Compliant



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MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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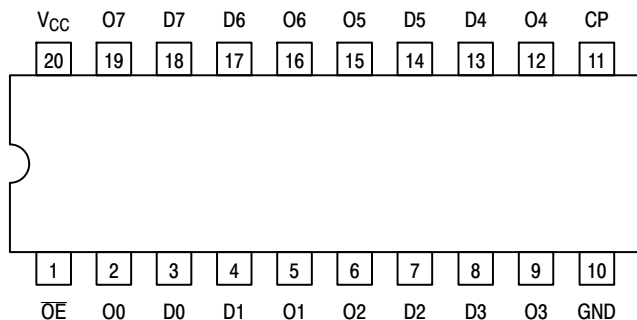


Figure 1. Pinout: 20-Lead (Top View)

PIN NAMES

Pins	Function
OE	Output Enable Input
CP	Clock Pulse Input
D0-D7	Data Inputs
O0-O7	3-State Outputs

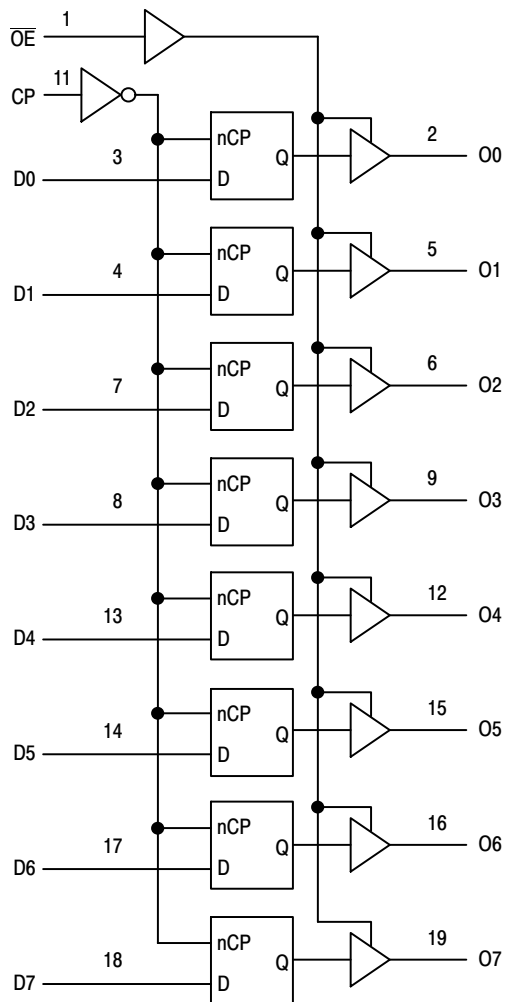


Figure 2. LOGIC DIAGRAM

TRUTH TABLE

INPUTS			OUTPUTS	OPERATING MODE
OE	CP	Dn	On	
L	↑	l	L	Load and Read Register
L	↑	h	H	
L	↑	X	NC	Hold and Read Register
H	↑	X	Z	Hold and Disable Outputs
H	↑	l	Z	Load Internal Register and Disable Outputs
H	↑	h	Z	

- H = High Voltage Level
- h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
- L = Low Voltage Level
- l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
- NC = No Change, State Prior to Low-to-High Clock Transition
- X = High or Low Voltage Level and Transitions are Acceptable
- Z = High Impedance State
- ↑ = Low-to-High Transition
- ↑ = Not a Low-to-High Transition; For I_{CC} Reasons, DO NOT FLOAT Inputs

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MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Units
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _I	DC Input Voltage		-0.5 ≤ V _I ≤ +7.0	V
V _O	DC Output Voltage	Output in 3-State	-0.5 ≤ V _O ≤ +7.0	V
		(Note 1)	-0.5 ≤ V _O ≤ V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	V _I < GND	-50	mA
I _{OK}	DC Output Diode Current	V _O < GND	-50	mA
		V _O > V _{CC}	+50	mA
I _O	DC Output Source/Sink Current		±50	mA
I _{CC}	DC Supply Current Per Supply Pin		±100	mA
I _{GND}	DC Ground Current Per Ground Pin		±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V _{CC}	Supply Voltage Operating Data Retention Only	2.0	3.3	3.6	V
		1.5	3.3	3.6	
V _I	Input Voltage	0		5.5	V
V _O	Output Voltage (HIGH or LOW State) (3-State)	0		V _{CC}	V
		0		5.5	
I _{OH}	HIGH Level Output Current, V _{CC} = 3.0 V – 3.6 V			-24	mA
I _{OL}	LOW Level Output Current, V _{CC} = 3.0 V – 3.6 V			24	mA
I _{OH}	HIGH Level Output Current, V _{CC} = 2.7 V – 3.0 V			-12	mA
I _{OL}	LOW Level Output Current, V _{CC} = 2.7 V – 3.0 V			12	mA
T _A	Operating Free-Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8 V to 2.0 V, V _{CC} = 3.0 V	0		10	ns/V

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LCX374DWR2G	SOIC-20 WB (Pb-Free)	1000 Tape & Reel
MC74LCX374DTR2G	TSSOP-20*	2500 Tape & Reel
MC74LCX374MELG	SOEIAJ-20 (Pb-Free)	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Units
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2)	2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		V
V _{IL}	LOW Level Input Voltage (Note 2)	2.7 V ≤ V _{CC} ≤ 3.6 V		0.8	V
V _{OH}	HIGH Level Output Voltage	2.7 V ≤ V _{CC} ≤ 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2		V
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		
V _{OL}	LOW Level Output Voltage	2.7 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA		0.2	V
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	
I _I	Input Leakage Current	2.7 V ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _I ≤ 5.5 V		±5.0	μA
I _{OZ}	3-State Output Current	2.7 ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _O ≤ 5.5 V; V _I = V _{IH} or V _{IL}		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0 V; V _I or V _O = 5.5 V		10	μA
I _{CC}	Quiescent Supply Current	2.7 ≤ V _{CC} ≤ 3.6 V; V _I = GND or V _{CC}		10	μA
		2.7 ≤ V _{CC} ≤ 3.6 V; 3.6 ≤ V _I or V _O ≤ 5.5 V		±10	μA
ΔI _{CC}	Increase in I _{CC} per Input	2.7 ≤ V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS (t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω)

Symbol	Parameter	Waveform	Limits				Units
			T _A = -40°C to +85°C				
			V _{CC} = 3.0 V to 3.6 V		V _{CC} = 2.7 V		
			Min	Max	Min	Max	
f _{max}	Clock Pulse Frequency	1	150				MHz
t _{PLH} t _{PHL}	Propagation Delay CP to O _n	1	1.5 8.5	8.5 1.5	1.5 9.5	9.5 1.5	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH and LOW Levels	2	1.5 8.5	8.5 1.5	1.5 9.5	9.5 1.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time from HIGH and LOW Levels	2	1.5 7.5	7.5 1.5	1.5 8.5	8.5 1.5	ns
t _s	Setup Time, HIGH or LOW D _n to CP	1	2.5		2.5		ns
t _h	Hold Time, HIGH or LOW D _n to CP	1	1.5		1.5		ns
t _w	CP Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 3)			1.0 1.0			ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

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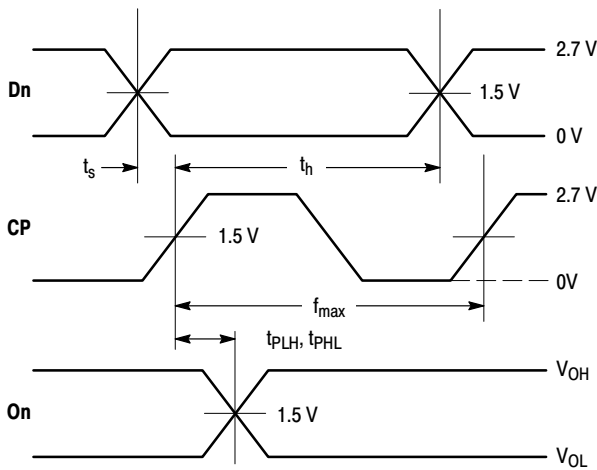
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = +25°C			Units
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 4)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V		0.8		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V		0.8		V

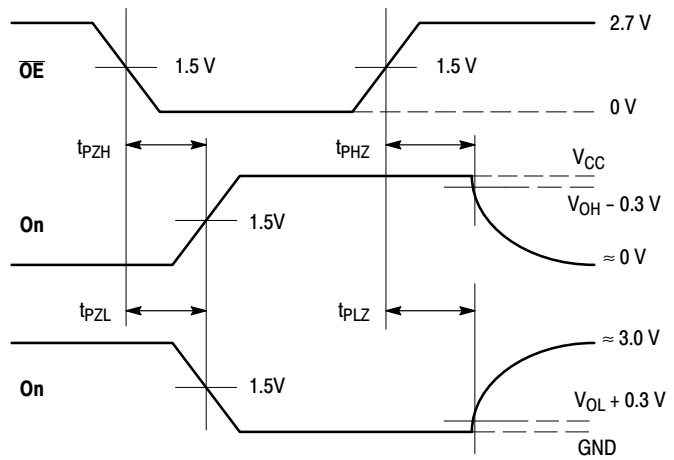
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

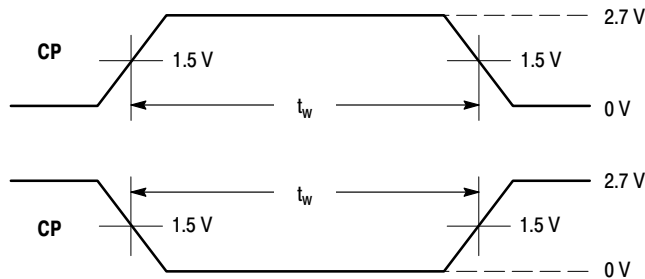
Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	25	pF



WAVEFORM 1 - PROPAGATION DELAYS, SETUP AND HOLD TIMES
 $t_R = t_F = 2.5$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns



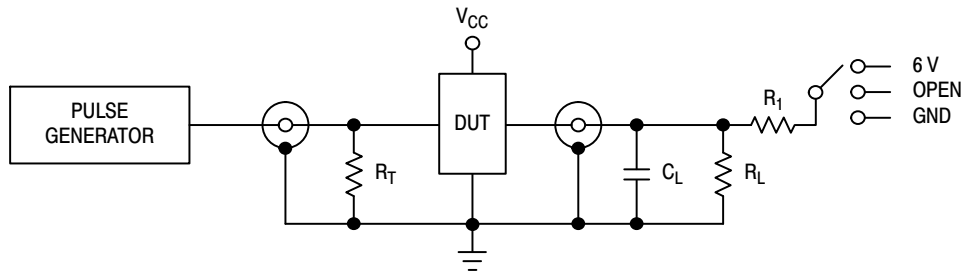
WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns



WAVEFORM 3 - PULSE WIDTH
 $t_R = t_F = 2.5$ ns (or fast as required) from 10% to 90%;
 Output requirements: V_{OL} ≤ 0.8 V, V_{OH} ≥ 2.0 V

Figure 3. AC Waveforms

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TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6 V
Open Collector/Drain t_{PLH} and t_{PHL}	6 V
t_{PZH} , t_{PHZ}	GND

$C_L = 50 \text{ pF}$ or equivalent (Includes jig and probe capacitance)

$R_L = R_1 = 500 \text{ } \Omega$ or equivalent

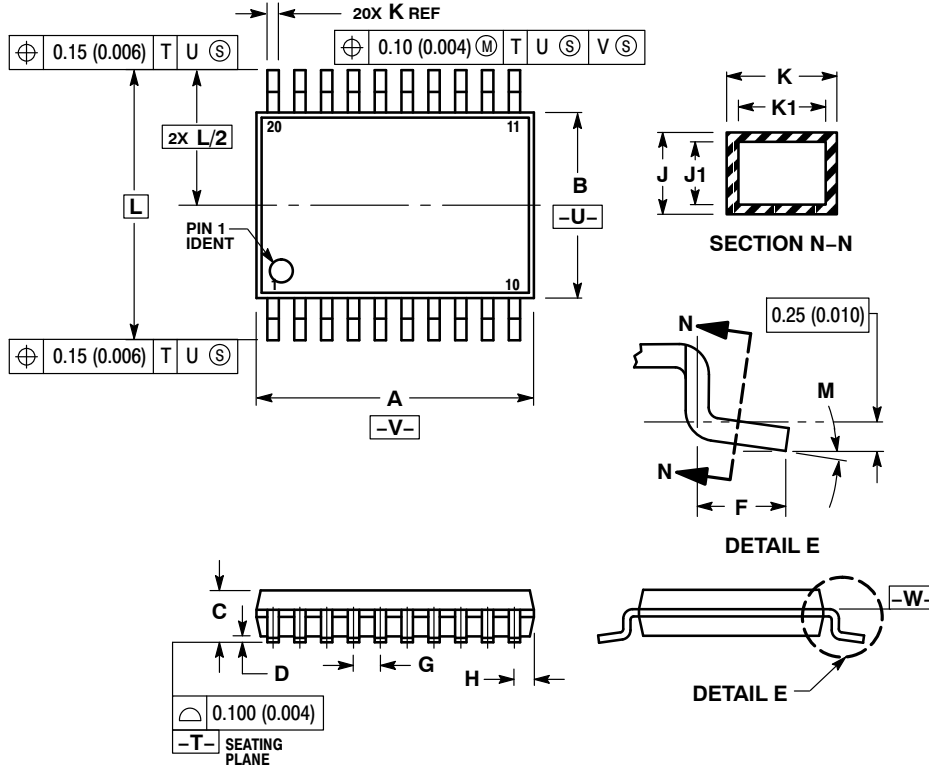
$R_T = Z_{OUT}$ of pulse generator (typically $50 \text{ } \Omega$)

Figure 4. Test Circuit

MC74LCX374

PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE C

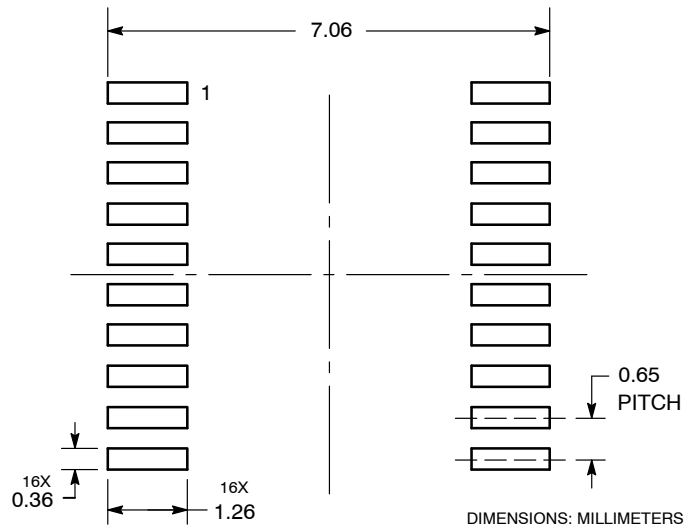


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

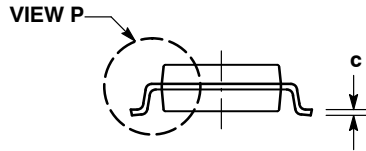
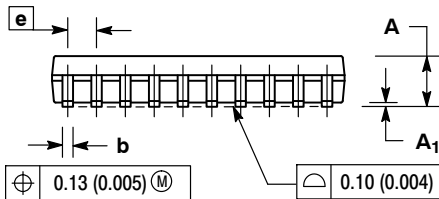
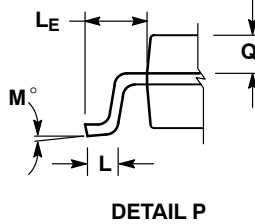
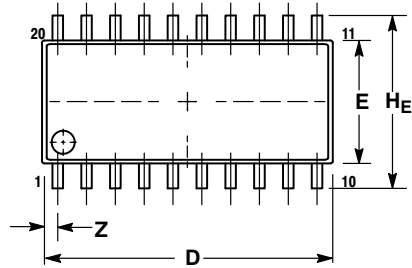
SOLDERING FOOTPRINT



MC74LCX374

PACKAGE DIMENSIONS

SOEIAJ-20
M SUFFIX
CASE 967-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°		10°	
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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