

NTD4810N

Power MOSFET

30 V, 54 A, Single N-Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb-Free Devices

Applications

- CPU Power Delivery
- DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DSS}	30	V		
Gate-to-Source Voltage	V_{GS}	± 20	V		
Continuous Drain Current ($R_{\theta JA}$) (Note 1)	I_D	$T_A = 25^\circ\text{C}$	12.4	A	
		$T_A = 85^\circ\text{C}$	9.6		
Power Dissipation ($R_{\theta JA}$) (Note 1)	P_D	2.62	W		
Continuous Drain Current ($R_{\theta JA}$) (Note 2)	I_D	$T_A = 25^\circ\text{C}$	9	A	
		$T_A = 85^\circ\text{C}$	7		
Power Dissipation ($R_{\theta JA}$) (Note 2)	P_D	1.4	W		
Continuous Drain Current ($R_{\theta JC}$) (Note 1)	I_D	$T_C = 25^\circ\text{C}$	54	A	
		$T_C = 85^\circ\text{C}$	42		
Power Dissipation ($R_{\theta JC}$) (Note 1)	P_D	50	W		
Pulsed Drain Current	$t_p = 10\mu\text{s}$	$T_A = 25^\circ\text{C}$	I_{DM}	120	A
Current Limited by Package	$T_A = 25^\circ\text{C}$	$I_{DmaxPkg}$	45	A	
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175		$^\circ\text{C}$	
Source Current (Body Diode)	I_S	41		A	
Drain to Source dV/dt	dV/dt	6.0		V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 24\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 1.0\text{ mH}$, $I_{L(pk)} = 14\text{ A}$, $R_G = 25\ \Omega$)	E_{AS}	98		mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260		$^\circ\text{C}$	

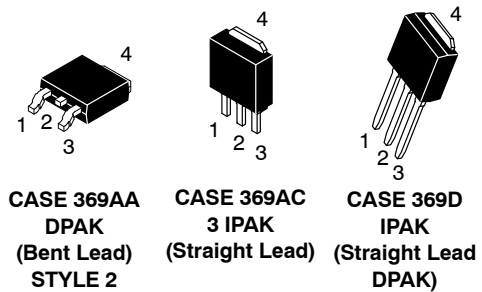
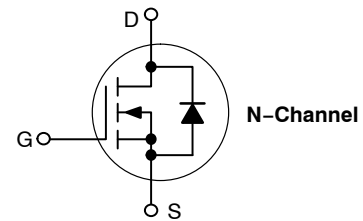
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



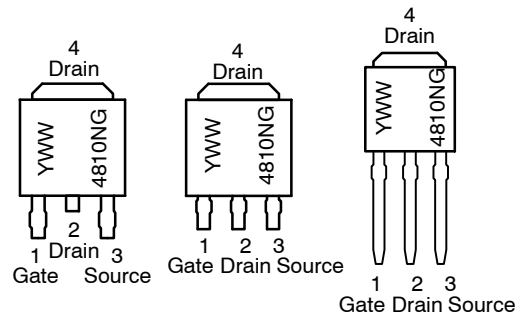
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<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	10 m Ω @ 10 V	54 A
	15.7 m Ω @ 4.5 V	



MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
 WW = Work Week
 4810N = Device Code
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NTD4810N

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.0	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	57.2	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	107.3	

1. Surface-mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			27		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.2		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ to }11.5\text{ V}$	$I_D = 30\text{ A}$		8.0	10	m Ω
			$I_D = 15\text{ A}$		7.8		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$		12	15.7	
			$I_D = 15\text{ A}$		11		
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		9.0		S	

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 12\text{ V}$		1165	1350	pF
Output Capacitance	C_{oss}			284	330	
Reverse Transfer Capacitance	C_{rss}			154	200	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		9.2	11	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.3		
Gate-to-Source Charge	Q_{GS}			3.3		
Gate-to-Drain Charge	Q_{GD}			4.4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		21		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		11.5		ns
Rise Time	t_r			20.7		
Turn-Off Delay Time	$t_{d(off)}$			13.8		
Fall Time	t_f			3.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		7.2		ns
Rise Time	t_r			20.7		
Turn-Off Delay Time	$t_{d(off)}$			21.8		
Fall Time	t_f			2.6		

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

NTD4810N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 30 A	T _J = 25°C		0.92	1.2	V
			T _J = 125°C		0.79		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A			18.2		ns
Charge Time	t _a				10.6		
Discharge Time	t _b				7.6		
Reverse Recovery Time	Q _{RR}				8.8		

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C		2.49		nH
Drain Inductance, DPAK	L _D			0.0164		
Drain Inductance, IPAK	L _D			1.88		
Gate Inductance	L _G			3.46		
Gate Resistance	R _G			2.4		

NTD4810N

TYPICAL PERFORMANCE CURVES

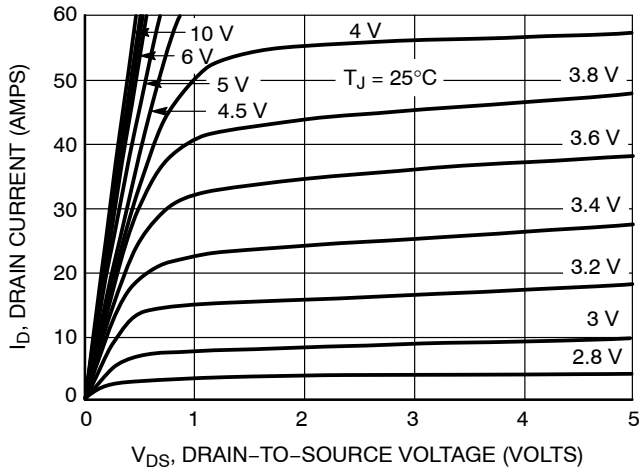


Figure 1. On-Region Characteristics

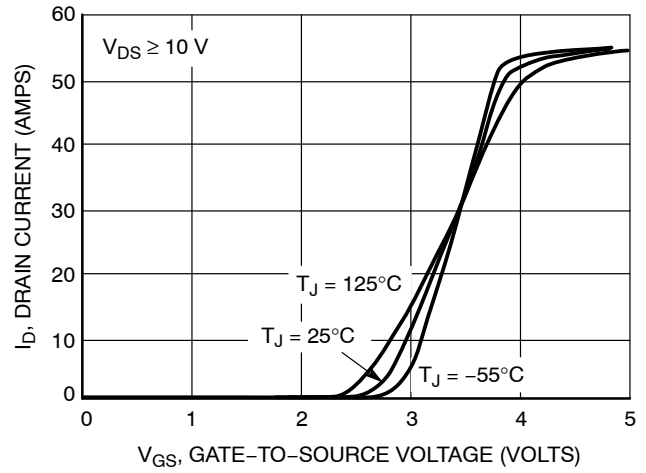


Figure 2. Transfer Characteristics

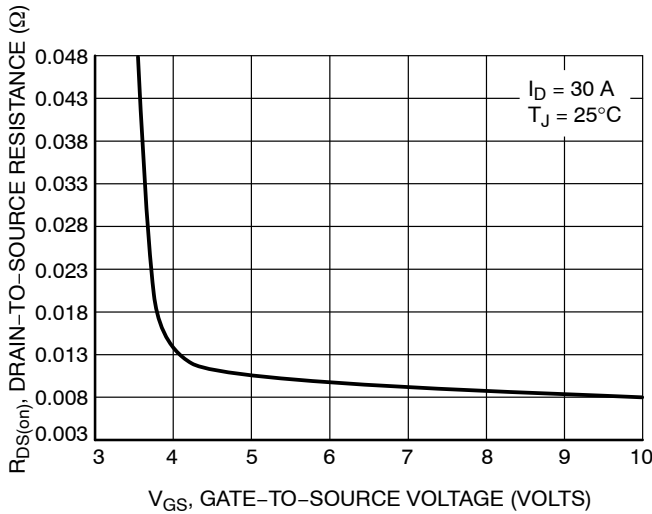


Figure 3. On-Resistance vs. Gate-to-Source Voltage

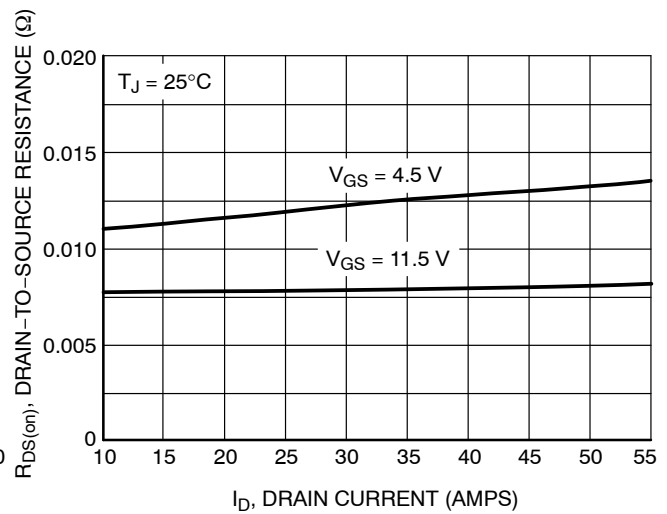


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

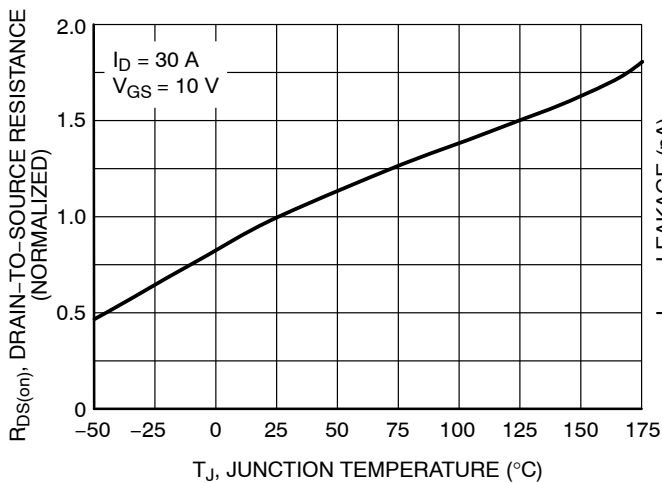


Figure 5. On-Resistance Variation with Temperature

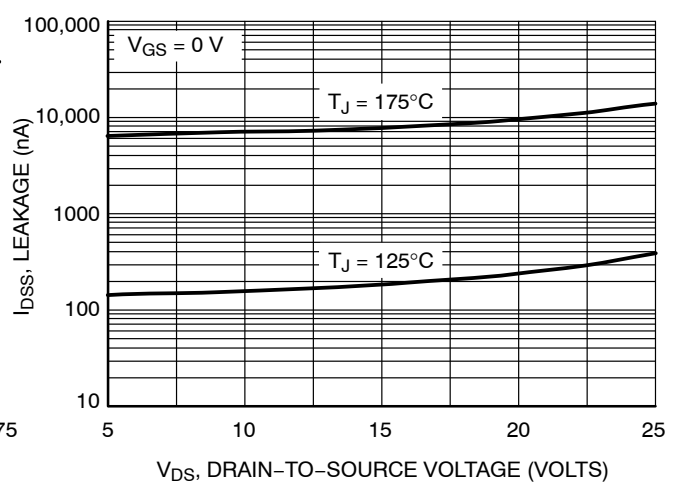


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

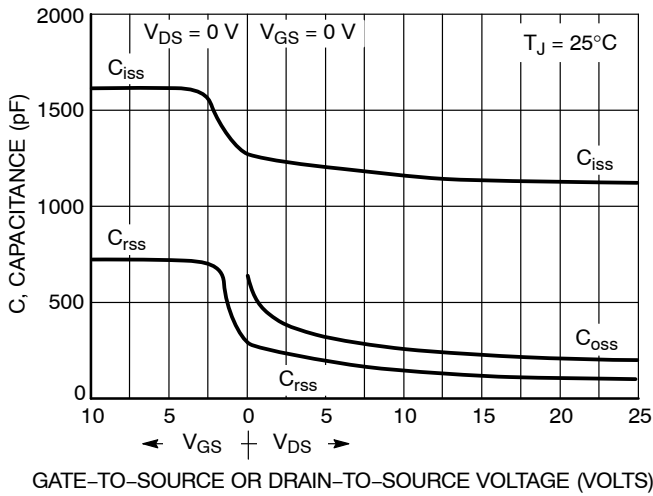


Figure 7. Capacitance Variation

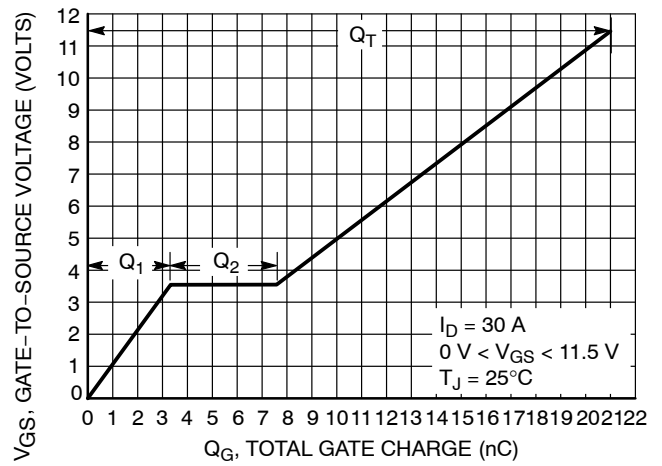


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

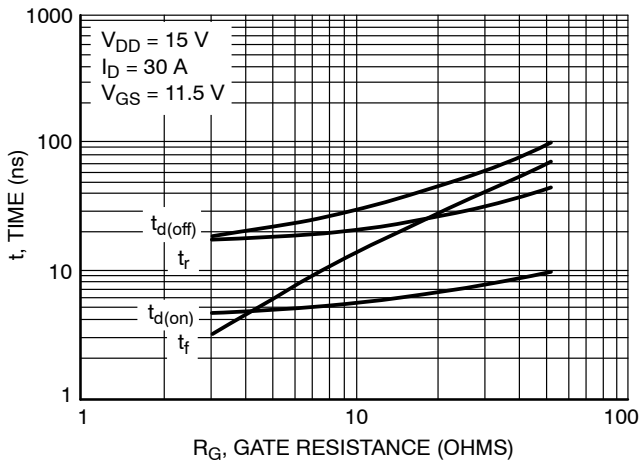


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

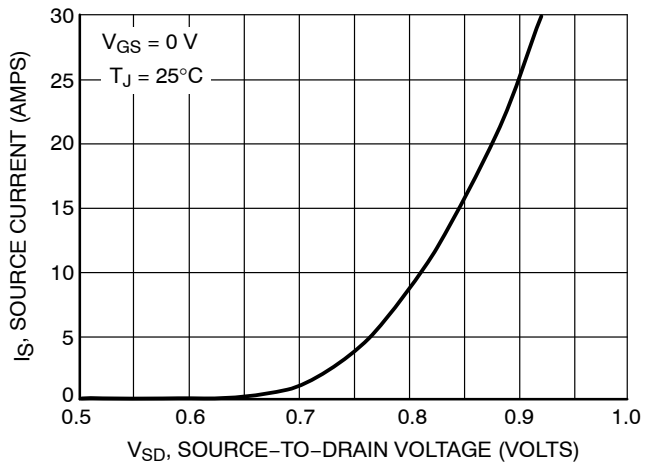


Figure 10. Diode Forward Voltage vs. Current

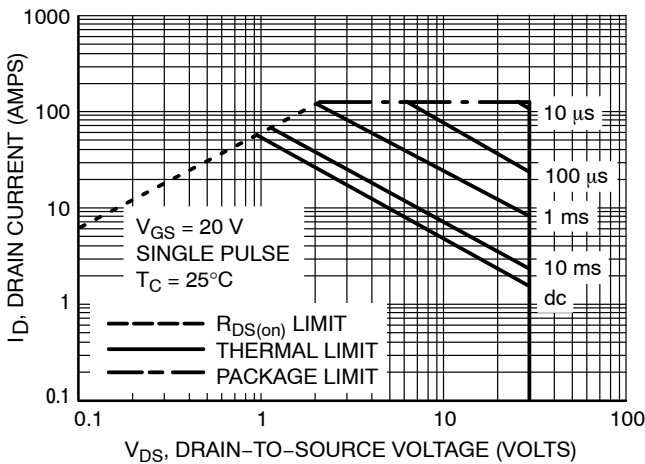


Figure 11. Maximum Rated Forward Biased Safe Operating Area

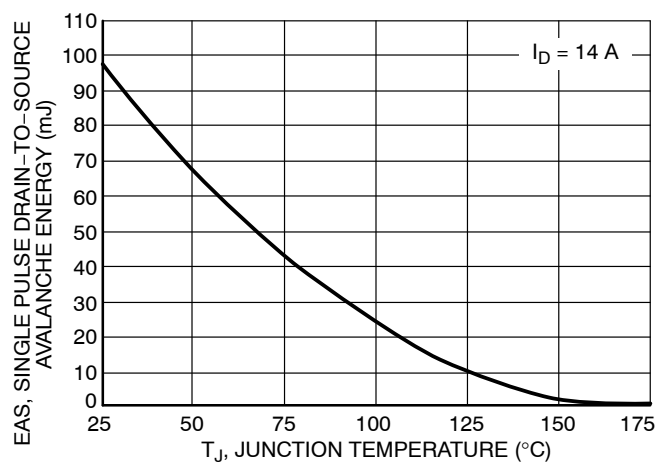


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTD4810N

TYPICAL PERFORMANCE CURVES

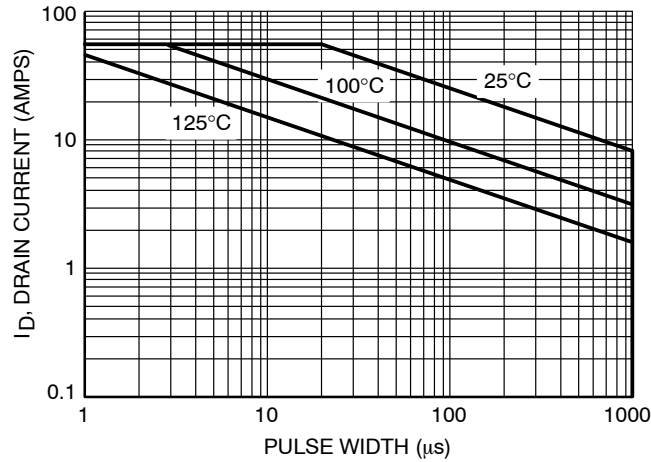


Figure 13. Avalanche Characteristics

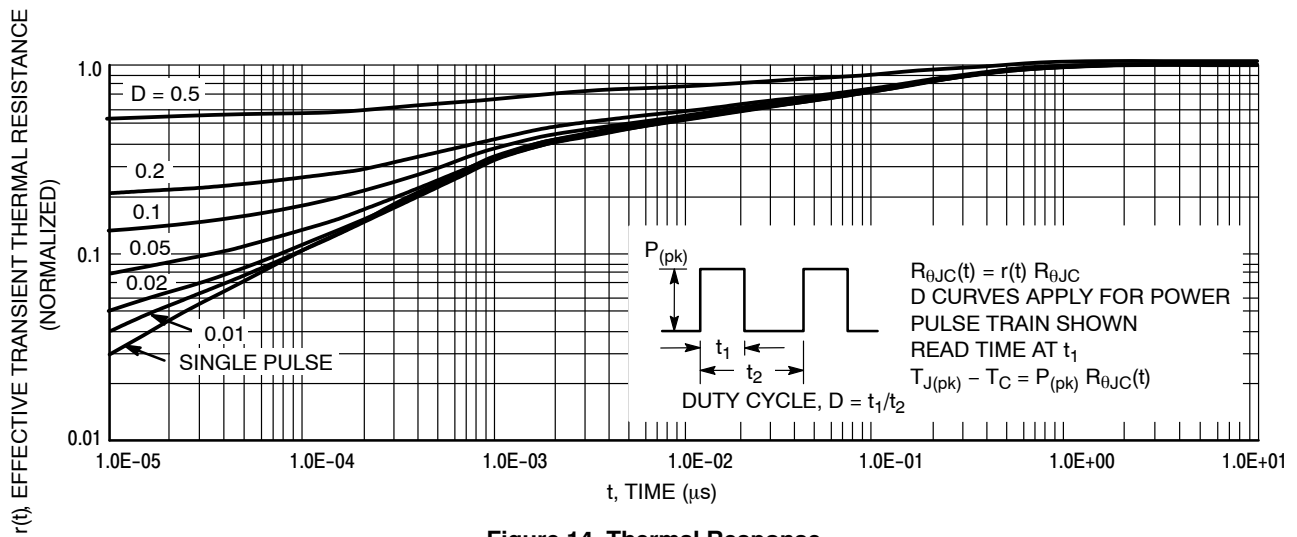


Figure 14. Thermal Response

ORDERING INFORMATION

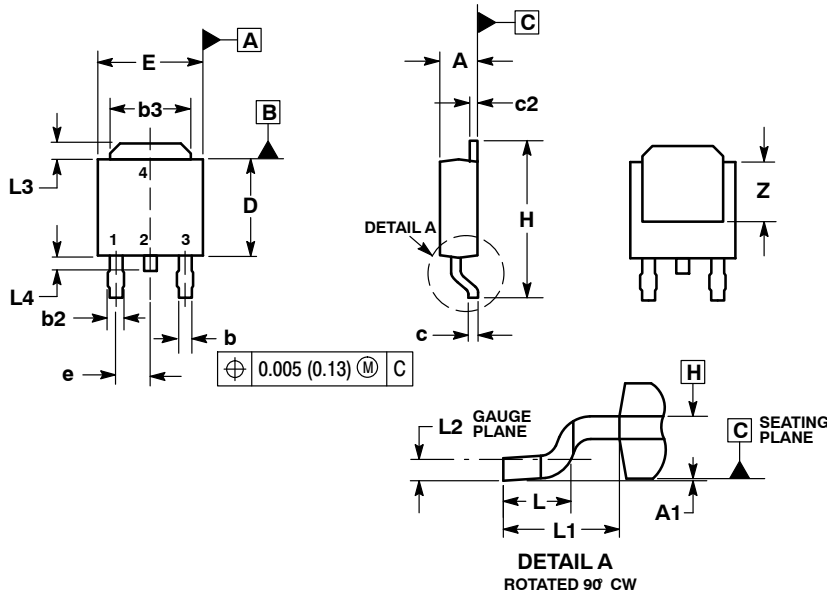
Order Number	Package	Shipping [†]
NTD4810NT4G	DPAK (Pb-Free)	2500 Tape & Reel
NTD4810N-1G	IPAK (Pb-Free)	75 Units/Rail
NTD4810N-35G	IPAK Trimmed Lead (3.5 ± 0.15 mm) (Pb-Free)	75 Units/Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD4810N

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE)
CASE 369AA-01
ISSUE B

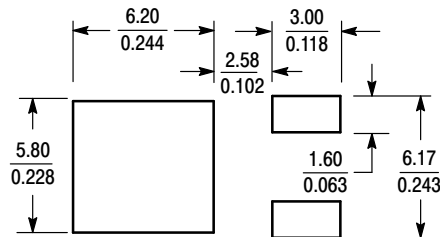


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

STYLE 2:

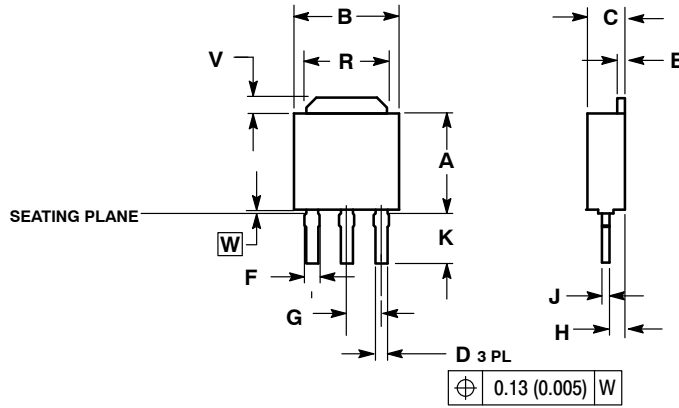
- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD4810N

PACKAGE DIMENSIONS

3 IPAK, STRAIGHT LEAD CASE 369AC-01 ISSUE O

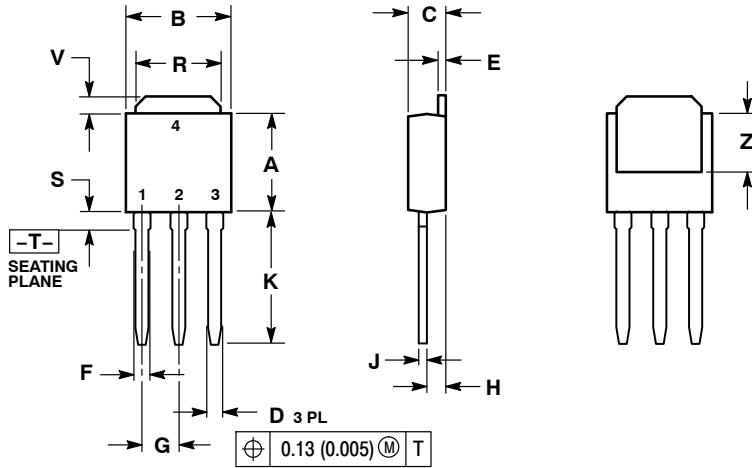


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

IPAK CASE 369D-01 ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

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