MC74HC125A, MC74HC126A

Quad 3-State Noninverting Buffers

High−Performance Silicon−Gate CMOS

The MC74HC125A and MC74HC126A are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC125A and HC126A noninverting buffers are designed to be used with 3−state memory address drivers, clock drivers, and other bus−oriented systems. The devices have four separate output enables that are active−low (HC125A) or active−high (HC126A).
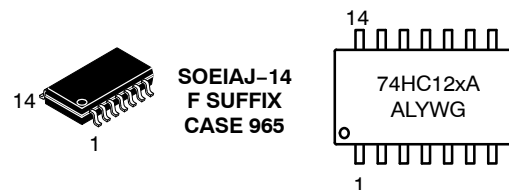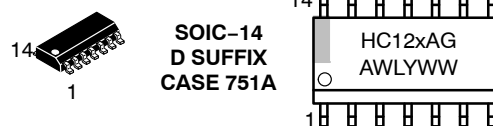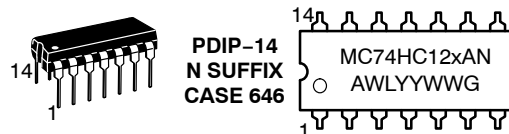
Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

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MARKING DIAGRAMS

PDIP–14
N SUFFIX
CASE 646

MC74HC12xAN
AWLYYWWG

SOIC–14
D SUFFIX
CASE 751A

HC12xAG
AWLYWW

TSSOP–14
DT SUFFIX
CASE 948G

HC
12xA
ALYW■

SOEIAJ–14
F SUFFIX
CASE 965

74HC12xA
ALYWG

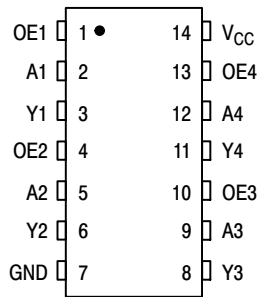| x | = 5, 6 |
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ■	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.
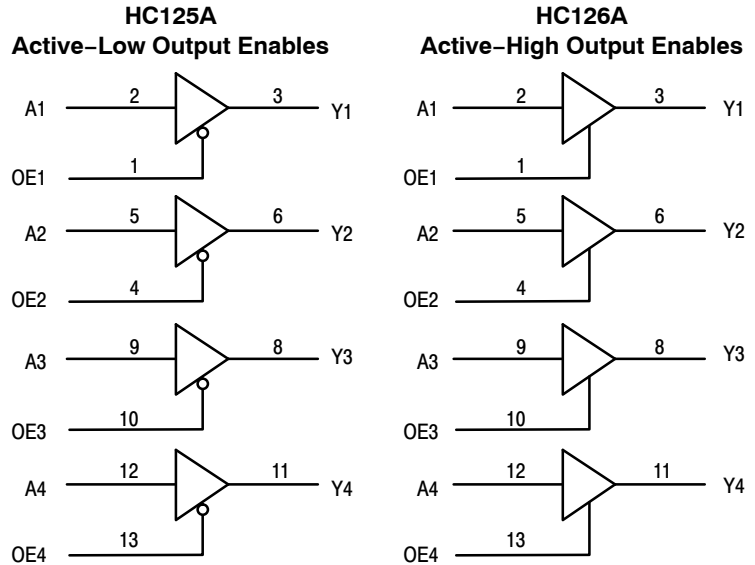
MC74HC125A, MC74HC126A

PIN ASSIGNMENT

OE1	1 ●	14	V$_{CC}$
A1	2	13	OE4
Y1	3	12	A4
OE2	4	11	Y4
A2	5	10	OE3
Y2	6	9	A3
GND	7	8	Y3

LOGIC DIAGRAM

HC125A
Active−Low Output Enables

HC126A
Active−High Output Enables

PIN 14 = V$_{CC}$
PIN 7 = GND

FUNCTION TABLE

HC125A				HC126A		
Inputs		Output		Inputs		Output
A	OE	Y		A	OE	Y
H	L	H		H	H	H
L	L	L		L	H	L
X	H	Z		X	L	Z

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V$_{CC}$	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V$_{in}$	DC Input Voltage (Referenced to GND)	− 0.5 to V$_{CC}$ + 0.5	V
V$_{out}$	DC Output Voltage (Referenced to GND)	− 0.5 to V$_{CC}$ + 0.5	V
I$_{in}$	DC Input Current, per Pin	± 20	mA
I$_{out}$	DC Output Current, per Pin	± 35	mA
I$_{CC}$	DC Supply Current, V$_{CC}$ and GND Pins	± 75	mA
P$_D$	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T$_{stg}$	Storage Temperature	− 65 to + 150	°C
T$_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: − 10 mW/°C from 65° to 125°C
SOIC Package: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V$_{in}$ and V$_{out}$ should be constrained to the range GND ≤ (V$_{in}$ or V$_{out}$) ≤ V$_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V$_{CC}$). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V$_{CC}$	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V$_{in}$, V$_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)		0	V$_{CC}$	V
T$_A$	Operating Temperature, All Package Types		− 55	+ 125	°C
t$_r$, t$_f$	Input Rise and Fall Time (Figure 1)	V$_{CC}$ = 2.0 V V$_{CC}$ = 4.5 V V$_{CC}$ = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V, $|I_{out}| \leq 20$ μA	2.0 / 3.0 / 4.5 / 6.0	1.5 / 2.1 / 3.15 / 4.2	1.5 / 2.1 / 3.15 / 4.2	1.5 / 2.1 / 3.15 / 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	$V_{out} = 0.1$ V, $|I_{out}| \leq 20$ μA	2.0 / 3.0 / 4.5 / 6.0	0.5 / 0.9 / 1.35 / 1.8	0.5 / 0.9 / 1.35 / 1.8	0.5 / 0.9 / 1.35 / 1.8	V
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IH}$, $|I_{out}| \leq 20$ μA	2.0 / 4.5 / 6.0	1.9 / 4.4 / 5.9	1.9 / 4.4 / 5.9	1.9 / 4.4 / 5.9	V
		$V_{in} = V_{IH}$, $|I_{out}| \leq 3.6$ mA / ≤ 6.0 mA / ≤ 7.8 mA	3.0 / 4.5 / 6.0	2.48 / 3.98 / 5.48	2.34 / 3.84 / 5.34	2.2 / 3.7 / 5.2	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IL}$, $|I_{out}| \leq 20$ μA	2.0 / 4.5 / 6.0	0.1 / 0.1 / 0.1	0.1 / 0.1 / 0.1	0.1 / 0.1 / 0.1	V
		$V_{in} = V_{IL}$, $|I_{out}| \leq 3.6$ mA / ≤ 6.0 mA / ≤ 7.8 mA	3.0 / 4.5 / 6.0	0.26 / 0.26 / 0.26	0.33 / 0.33 / 0.33	0.4 / 0.4 / 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND, $I_{out} = 0$ μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 / 3.0 / 4.5 / 6.0	90 / 36 / 18 / 15	115 / 45 / 23 / 20	135 / 60 / 27 / 23	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 / 3.0 / 4.5 / 6.0	120 / 45 / 24 / 20	150 / 60 / 30 / 26	180 / 80 / 36 / 31	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 / 3.0 / 4.5 / 6.0	90 / 36 / 18 / 15	115 / 45 / 23 / 20	135 / 60 / 27 / 23	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 / 3.0 / 4.5 / 6.0	60 / 22 / 12 / 10	75 / 28 / 15 / 13	90 / 34 / 18 / 15	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum 3–State Output Capacitance (Output in High–Impedance State)	–	15	15	15	pF

		Typical @ 25°C, V_{CC} = 5.0 V	Unit
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	30	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC125ANG	PDIP−14 (Pb−Free)	25 Units / Rail
MC74HC125ADG	SOIC−14 (Pb−Free)	55 Units / Rail
MC74HC125ADR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74HC125ADTG	TSSOP−14*	96 Units / Rail
MC74HC125ADTR2G	TSSOP−14*	2500 / Tape & Reel
MC74HC125AFG	SOEIAJ−14 (Pb−Free)	50 Units / Rail
MC74HC125AFELG	SOEIAJ−14 (Pb−Free)	2000 / Tape & Reel
MC74HC126ANG	PDIP−14 (Pb−Free)	25 Units / Rail
MC74HC126ADG	SOIC−14 (Pb−Free)	55 Units / Rail
MC74HC126ADR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74HC126ADTR2G	TSSOP−14*	2500 / Tape & Reel
MC74HC126AFELG	SOEIAJ−14 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging
  Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

SWITCHING WAVEFORMS
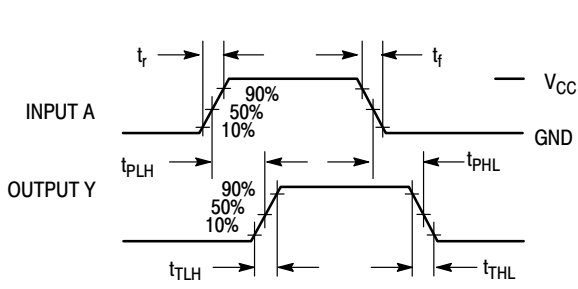
Figure 1.
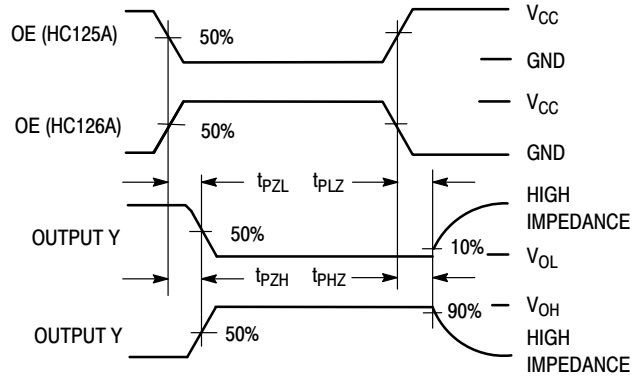
Figure 2.
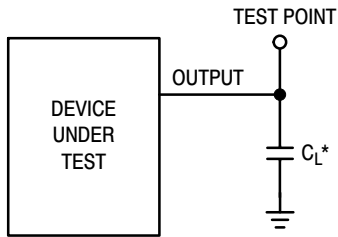
*Includes all probe and jig capacitance

Figure 3. Test Circuit
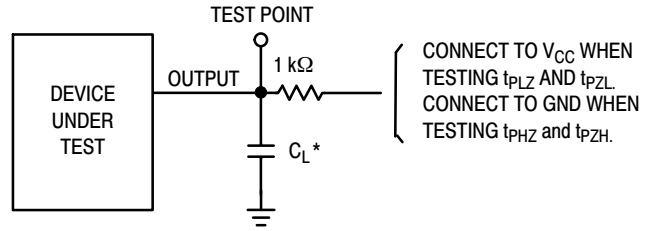
*Includes all probe and jig capacitance

Figure 4. Test Circuit

**HC125A
(1/4 OF THE DEVICE)**

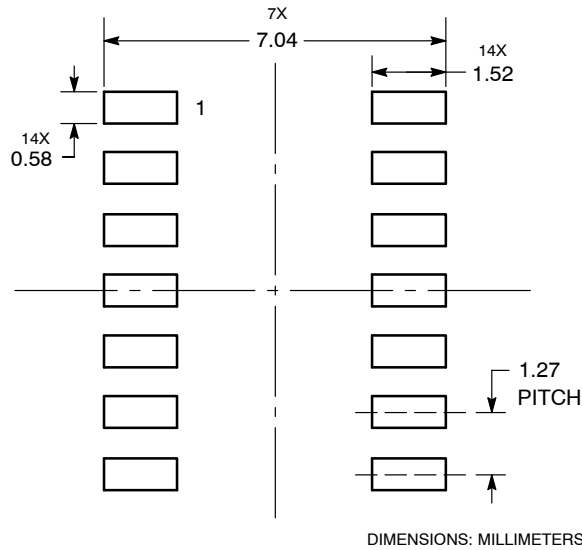

**HC126A
(1/4 OF THE DEVICE)**

PACKAGE DIMENSIONS

PDIP−14
N SUFFIX
CASE 646−06
ISSUE P
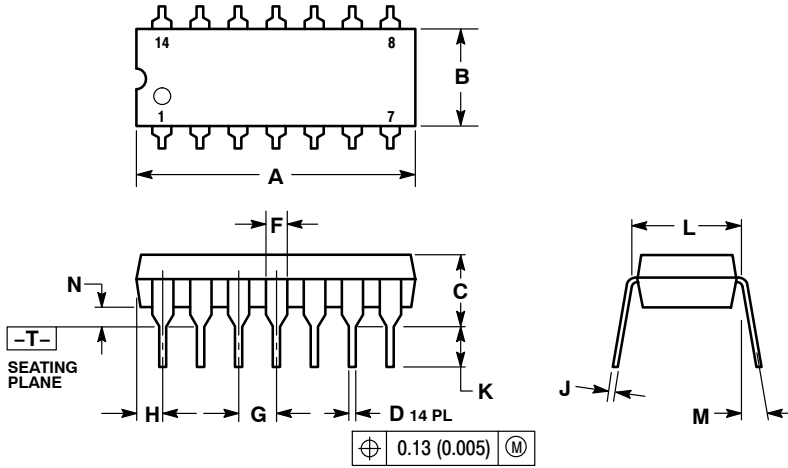
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 °	−−−	10 °
N	0.015	0.039	0.38	1.01

MC74HC125A, MC74HC126A

PACKAGE DIMENSIONS

SOIC−14
D SUFFIX
CASE 751A−03
ISSUE J
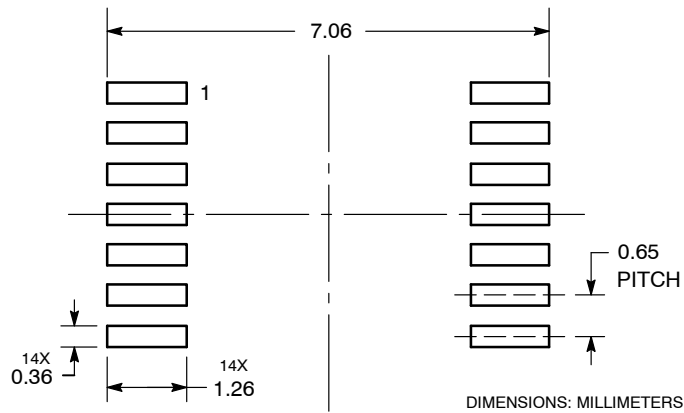
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

7X 7.04
14X 1.52
14X 0.58
1.27 PITCH

DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

TSSOP−14
DT SUFFIX
CASE 948G−01
ISSUE B
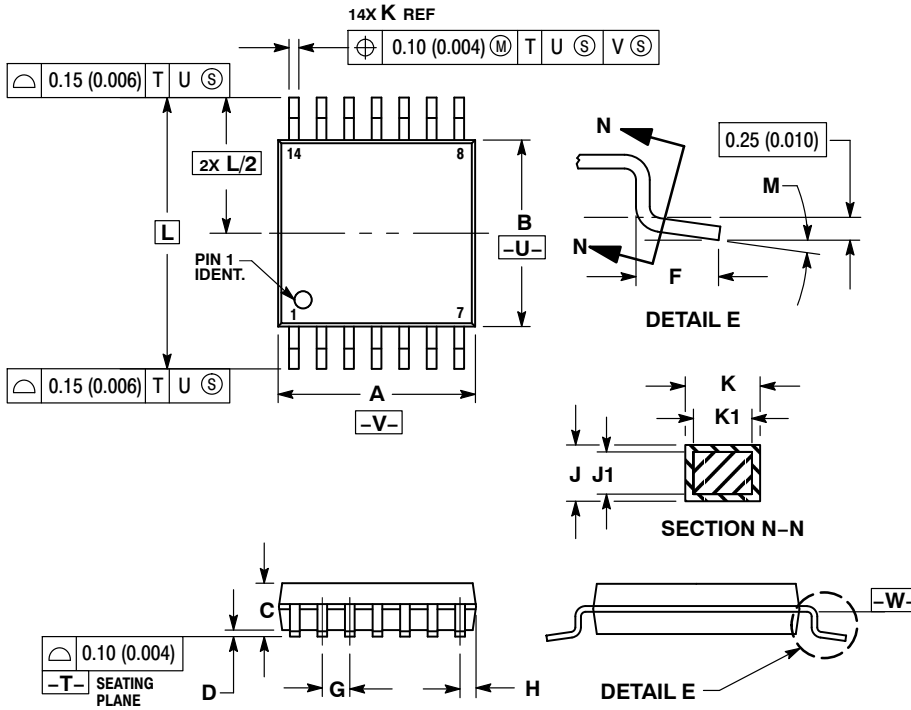
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

SOEIAJ–14
F SUFFIX
CASE 965–01
ISSUE B
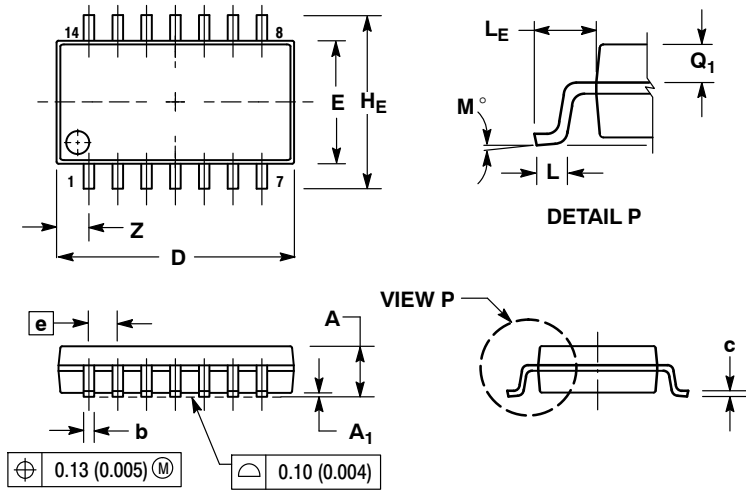
DETAIL P

VIEW P

⊕ | 0.13 (0.005) Ⓜ   △ | 0.10 (0.004)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

MC74HC125A/D