# NBSG111

# 2.5V/3.3V SiGe Differential 1:10 Clock/Data Driver with RSECL* Outputs

## *Reduced Swing ECL

ON Semiconductor®

http://onsemi.com

### Description

The NBSG111 is a 1−to−10 differential clock/data driver. The device is functionally equivalent to the LVEP111 device with much higher bandwidth and lower EMI capabilities.

Inputs incorporate internal 50 Ω termination resistors (input to VT pad) and accept NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

The Q[0:9] / $\overline{Q[0:9]}$ outputs have a differential synchronous enable (EN/$\overline{EN}$) pin. The synchronous enable pin is used to avoid a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of selected clock (CLK0/$\overline{CLK0}$ or CLK1/$\overline{CLK1}$), therefore all associated specification limits are referenced to the negative edge of the selected clock input.

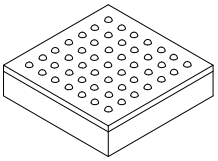
The $V_{BB}$ and $V_{MM}$ pins are internally generated voltage supplies available to this device only. The $V_{BB}$ is used for single−ended NECL or PECL inputs and the $V_{MM}$ pin is used for LVCMOS inputs. For single−ended input operation, the unused differential input is connected to $V_{BB}$ or $V_{MM}$ as a switching reference voltage. $V_{BB}$ or $V_{MM}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{MM}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ and $V_{MM}$ outputs should be left open.

### Features

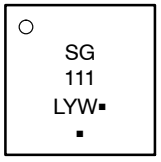
- Maximum Input Clock Frequency > 6 GHz Typical
- Maximum Input Data Rate > 6 Gb/s Typical
- 300 ps Typical Propagation Delay
- 60 ps Typical Rise and Fall Times
- RSPECL Output with Operating Range: $V_{CC}$ = 2.375 V to 3.465 V with $V_{EE}$ = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: $V_{CC}$ = 0 V with $V_{EE}$ = −2.375 V to −3.465 V
- RSECL Output Level (400 mV Peak−to−Peak Output), Differential Output
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP and EP Devices
- $V_{BB}$ and $V_{MM}$ Reference Voltage Output
- Pb−Free Package is Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**MARKING DIAGRAM***



FCBGA−49
BA SUFFIX
CASE 489A




SG111 = Device Code
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For further details, refer to Application Note AND8002/D

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

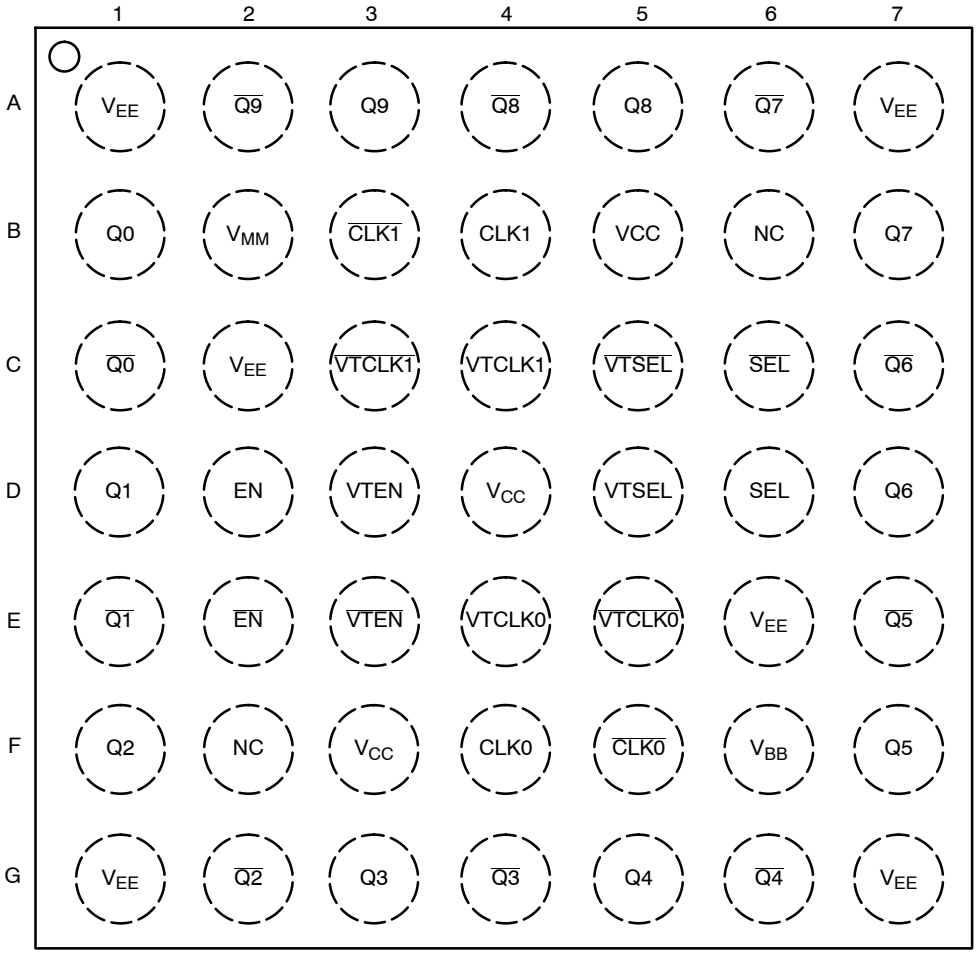



**Figure 1. BGA−49 Pinout** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin | Name | I/O | Description |
|---|---|---|---|
| A1,A7,G1,G7,C2,E6 | $V_{EE}$ | – | Negative Supply Voltage. All $V_{EE}$ Pins Must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| F3,D4,B5 | $V_{CC}$ | – | Positive Supply Voltage. All $V_{CC}$ Pins Must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| B2 | $V_{MM}$ | – | LVCMOS Reference Voltage Output ($V_{CC}$ – $V_{EE}$) / 2. |
| F6 | $V_{BB}$ | – | ECL Reference Voltage Output |
| E4 | VTCLK0 | – | Internal 50 Ω Termination Pin for CLK0. See Table 4. (Note 1) |
| F4 | CLK0 | ECL, CML, LVCMOS, LVDS, LVTTL Input | Noninverted Differential Input CLK0. Internal 75 kΩ to $V_{EE}$. |
| E5 | $\overline{\text{VTCLK0}}$ | – | Internal 50 Ω Termination Pin for $\overline{\text{CLK0}}$. See Table 4. (Note 1) |
| F5 | $\overline{\text{CLK0}}$ | ECL, CML, LVCMOS, LVDS, LVTTL Input | Inverted Differential Input $\overline{\text{CLK0}}$. Internal 75 kΩ to $V_{EE}$ and 36.5 kΩ to $V_{CC}$. |
| C4 | VTCLK1 | – | Internal 50 Ω Termination Pin 1. See Table 4. (Note 1) |
| B4 | CLK1 | ECL, CML, LVCMOS, LVDS, LVTTL Input | Noninverted Differential Input CLK1. Internal 75 kΩ to $V_{EE}$. |
| C3 | $\overline{\text{VTCLK1}}$ | – | Internal 50 Ω Termination Pin for $\overline{\text{CLK1}}$. See Table 4. (Note 1) |
| B3 | $\overline{\text{CLK1}}$ | ECL, CML, LVCMOS, LVDS, LVTTL Input | Inverted Differential Input $\overline{\text{CLK1}}$. Internal 75 kΩ to $V_{EE}$ and 36.5 kΩ to $V_{CC}$. |
| B1,D1,F1,G3,G5,F7, D7,B7,A5,A3 | Q[0:9] | RSECL Output | Noninverted Differential Outputs [0:9]. Typically Terminated with 50 Ω to $V_{TT}$ = $V_{CC}$ – 1.5 V |
| C1,E1,G2,G4,G6,E7, C7,A6,A4,A2 | $\overline{\text{Q[0:9]}}$ | RSECL Output | Inverted Differential Outputs [0:9]. Typically Terminated with 50 Ω to $V_{TT}$ = $V_{CC}$ – 1.5 V |
| D5 | VTSEL | – | Internal 50 Ω Termination Pin for SEL. See Table 4. (Note 1) |
| D6 | SEL | ECL, CML, LVCMOS, LVDS, LVTTL Input | Noninverted Differential Select Logic Input. Internal 75 kΩ to $V_{EE}$. |
| C5 | $\overline{\text{VTSEL}}$ | – | Internal 50 Ω Termination Pin for $\overline{\text{SEL}}$. See Table 4. (Note 1) |
| C6 | $\overline{\text{SEL}}$ | ECL, CML, LVCMOS, LVDS, LVTTL Input | Inverted Differential Select Logic Input. Internal 75 kΩ to $V_{EE}$ and 36.5 kΩ to $V_{CC}$. |
| D3 | VTEN | – | Internal 50 Ω Termination Pin for EN. See Table 4. (Note 1) |
| D2 | EN | ECL, CML, LVCMOS, LVDS, LVTTL Input | Noninverted Differential Output Enable Pin. Internal 75 kΩ to $V_{EE}$. |
| E3 | $\overline{\text{VTEN}}$ | – | Internal 50 Ω termination Pin for $\overline{\text{EN}}$. See Table 4. (Note 1) |
| E2 | $\overline{\text{EN}}$ | ECL, CML, LVCMOS, LVDS, LVTTL Input | Inverted Differential Output Enable Pin. Internal 75 kΩ to $V_{EE}$ and 36.5 kΩ to $V_{CC}$. |
| F2,B6 | NC | – | No Connect. The NC Pins are Electrically Connected to the Die and ”MUST BE” Left Open. |

1. In the differential configuration when the input termination pins (VTCLK, $\overline{\text{VTDCLK}}$) are connected to a common termination voltage and if no signal is applied, then the device will be susceptible to self−oscillation.

**Table 2. FUNCTION TABLE**

| SEL | EN | Active Input |
|---|---|---|
| L | L | Disabled Outputs |
| L | H | CLK0, $\overline{CLK0}$ |
| H | L | Disabled Outputs |
| H | H | CLK1, $\overline{CLK1}$ |

2. $\overline{SEL}$/$\overline{EN}$ are the inverse of SEL/EN unless specified otherwise.

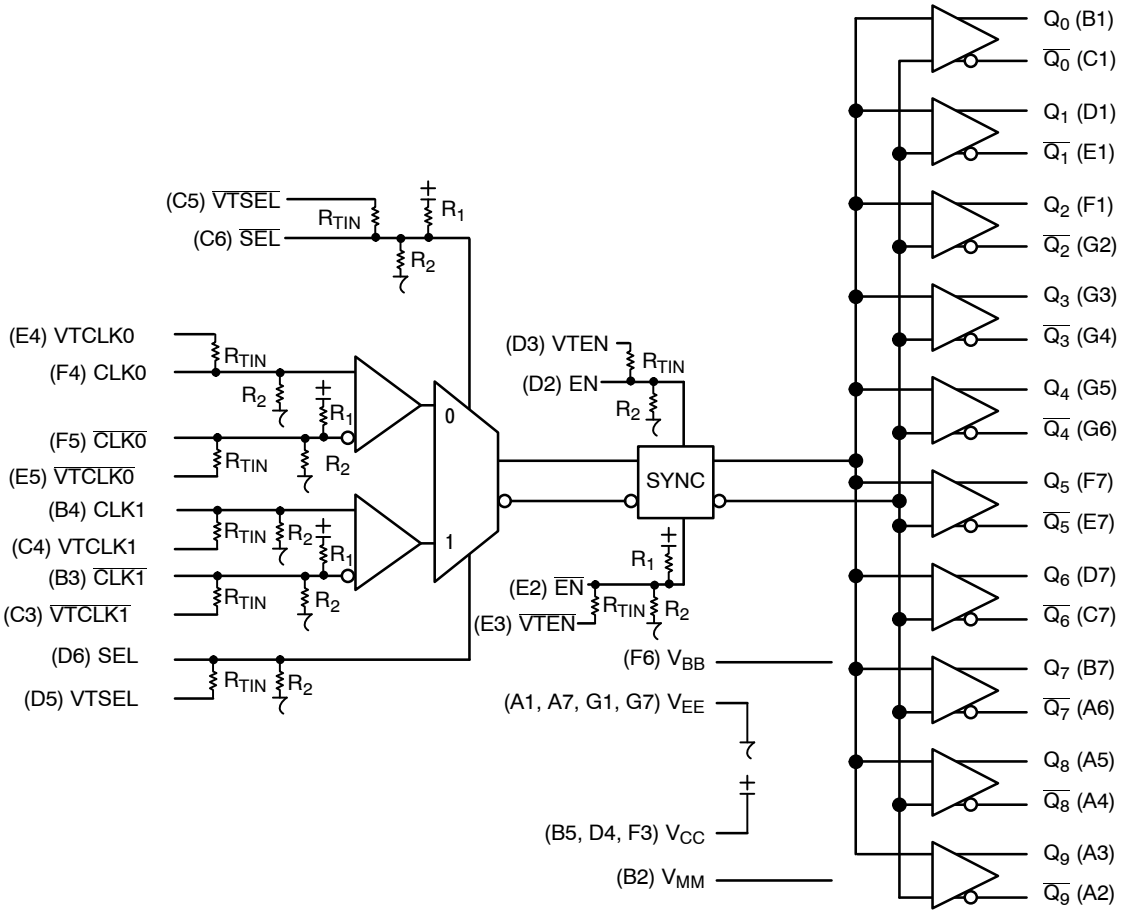



**Figure 2. Logic Diagram**

**Table 3. INTERFACING OPTIONS**

| INTERFACING OPTIONS | CONNECTIONS |
|---|---|
| CML | Connect VTCLK0, VTCLK1, VTEN, VTSEL and $\overline{VTCLK0}$, $\overline{VTCLK1}$, $\overline{VTEN}$, $\overline{VTSEL}$ to $V_{CC}$ |
| LVDS | Connect VTCLK0, VTCLK1, VTEN, VTSEL and $\overline{VTCLK0}$, $\overline{VTCLK1}$, $\overline{VTEN}$, $\overline{VTSEL}$ Together |
| AC−COUPLED | Bias VTCLK0, VTCLK1, VTEN, VTSEL and $\overline{VTCLK0}$, $\overline{VTCLK1}$, $\overline{VTEN}$, $\overline{VTSEL}$ Inputs within Common Mode Range ($V_{IHCMR}$) |
| RSECL, PECL, NECL | Standard ECL Termination Techniques |
| LVTTL, LVCMOS | See Text on Page 1. Unused Differential Input Switching Voltage Reference Range is from $V_{EE}$ + 1125 mV to $V_{CC}$ − 75 mV |

**Table 4. ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| Internal Input Pulldown Resistor, R2 (CLK0, $\overline{\text{CLK0}}$, CLK1, $\overline{\text{CLK1}}$, SEL, $\overline{\text{SEL}}$, EN, $\overline{\text{EN}}$) | | 75 kΩ |
| Internal Input Pullup Resistor, R1 ($\overline{\text{CLK0}}$, $\overline{\text{CLK1}}$, $\overline{\text{SEL}}$, $\overline{\text{EN}}$) | | 36.5 kΩ |
| ESD Protection | Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 100 V<br>> 1 kV |
| Moisture Sensitivity (Note 3) | | Level 3 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 479 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

3. For additional information, see Application Note AND8003/D.

**Table 5. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | $V_{EE}$ = 0 V | | 3.6 | V |
| $V_I$ | Positive Input<br>Negative Input | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 3.6<br>−3.6 | V<br>V |
| $V_{EE}$ | Negative Power Supply | $V_{CC}$ = 0 V | | −3.6 | V |
| $V_{INPP}$ | Differential Input Voltage \|CLK − $\overline{\text{CLK}}$\| | $V_{CC} - V_{EE} \geq$ 2.8 V<br>$V_{CC} - V_{EE} <$ 2.8 V | | 2.8<br>$\|V_{CC} - V_{EE}\|$ | V<br>V |
| $I_{OUT}$ | Output Current | Continuous<br>Surge | | 25<br>50 | mA<br>mA |
| $I_{IN}$ | Input Current Through $R_T$ (50 Ω Resistor) | Static<br>Surge | | 45<br>80 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | 1 | mA |
| $I_{MM}$ | $V_{MM}$ Sink/Source | | | 1 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +70 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note 4) | 0 LFPM<br>500 LFPM | 49 FCBGA<br>49 FCBGA | 67<br>57 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | 2S2P (Note 4) | 49 FCBGA | 2 to 4 | °C/W |
| $T_{sol}$ | Wave Solder | < 15 sec. | | 225 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard 51−6, multilayer board − 2S2P (2 signal, 2 power).

**Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT** $V_{CC}$ = 2.5 V; $V_{EE}$ = 0 V (Note 5)

| Symbol | Characteristic | −40°C | | | 25°C | | | 70°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Negative Power Supply Current | 70 | 85 | 110 | 70 | 85 | 110 | 70 | 85 | 110 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 6) | 1365 | 1520 | 1615 | 1410 | 1530 | 1660 | 1435 | 1560 | 1685 | mV |
| $V_{OUTPP}$ | Output Voltage Amplitude | 305 | 420 | 545 | 305 | 420 | 545 | 305 | 420 | 545 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Notes 8 and 9) | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Notes 8 and 10) | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | mV |
| $V_{BB}$ | PECL Output Voltage Reference | 1025 | 1100 | 1265 | 1025 | 1100 | 1265 | 1025 | 1100 | 1265 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| $V_{MM}$ | LVCMOS Output Voltage Reference (@ 2.5 $V_{CC}$) | 1050 | 1250 | 1450 | 1050 | 1250 | 1450 | 1050 | 1250 | 1450 | mV |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | 30 | 100 | | 30 | 100 | | 30 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$) | | 25 | 100 | | 25 | 100 | | 25 | 100 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 7. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0 V (Note 11)

| | | −40°C | | | 25°C | | | 70°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Negative Power Supply Current | 70 | 85 | 110 | 70 | 85 | 110 | 70 | 85 | 110 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 6) | 2165 | 2320 | 2415 | 2210 | 2330 | 2460 | 2235 | 2360 | 2485 | mV |
| $V_{OUTPP}$ | Output Voltage Amplitude | 305 | 420 | 545 | 305 | 420 | 545 | 305 | 420 | 545 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Notes 8 and 9) | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Notes 8 and 10) | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | mV |
| $V_{BB}$ | PECL Output Voltage Reference | 1825 | 1900 | 2065 | 1825 | 1900 | 2065 | 1825 | 1900 | 2065 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| $V_{MM}$ | LVCMOS Output Voltage Reference (@ 3.3 $V_{CC}$) | 1450 | 1650 | 1850 | 1450 | 1650 | 1850 | 1450 | 1650 | 1850 | mV |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | 30 | 100 | | 30 | 100 | | 30 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$) | | 25 | 100 | | 25 | 100 | | 25 | 100 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.125 V to −0.965 V. $V_{MM}$ varies ($V_{CC}$ − $V_{EE}$) / 2 with $V_{CC}$ and $V_{EE}$.
6. All outputs loaded with 50 Ω to $V_{CC}$ − 1.5 V. $V_{OH}$/$V_{OL}$ measured at $V_{IH}$/$V_{IL}$ (Typical).
7. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
8. $V_{THR}$ is the voltage applied to the complementary input, typically $V_{BB}$ or $V_{MM}$. $V_{THR(MIN)}$ = $V_{IHCMR}$ + 75 mV. $V_{THR(MAX)}$ = $V_{IHCMR}$ − 75 mV.
9. $V_{IH}$ cannot exceed $V_{CC}$.
10. $V_{IL}$ always ≥ $V_{EE}$.
11. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.925 V to −0.165 V. $V_{MM}$ varies ($V_{CC}$ − $V_{EE}$) / 2 with $V_{CC}$ and $V_{EE}$.

*Typicals used for testing purposes.

**Table 8. DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT**

$V_{CC}$ = 0 V; $V_{EE}$ = −3.465 V to −2.375 V (Note 12)

| | | −40°C | | | 25°C | | | 70°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Negative Power Supply Current | 70 | 85 | 110 | 70 | 85 | 110 | 70 | 85 | 110 | mA |
| VOH | Output HIGH Voltage (Note 13) | −1135 | −980 | −885 | −1090 | −970 | −840 | −1065 | −940 | −815 | mV |
| $V_{OUTPP}$ | Output Voltage Amplitude | 305 | 420 | 545 | 305 | 420 | 545 | 305 | 420 | 545 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Notes 15 and 16) | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Notes 15 and 17) | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | mV |
| $V_{BB}$ | NECL Output Voltage Reference | −1475 | −1400 | −1235 | −1475 | −1400 | −1235 | −1475 | −1400 | −1235 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 14) | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | V |
| $V_{MM}$ | LVCMOS Output Voltage Reference (@ − 2.5 $V_{EE}$) (@ − 3.3 $V_{EE}$) | −1450 −1850 | −1250 −1650 | −1050 −1450 | −1450 −1850 | −1250 −1650 | −1050 −1450 | −1450 −1850 | −1250 −1650 | −1050 −1450 | mV |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | 30 | 100 | | 30 | 100 | | 30 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$) | | 25 | 100 | | 25 | 100 | | 25 | 100 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Input and output parameters vary 1:1 with $V_{CC}$.
13. All outputs loaded with 50 Ω to $V_{CC}$ − 1.5 V. $V_{OH}/V_{OL}$ measured at $V_{IH}/V_{IL}$ (Typical).
14. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
15. $V_{THR}$ is the voltage applied to the complementary input, typically $V_{BB}$ or $V_{MM}$. $V_{THR(MIN)} = V_{IHCMR} + 75$ mV. $V_{THR(MAX)} = V_{IHCMR} − 75$ mV.
16. $V_{IH}$ cannot exceed $V_{CC}$.
17. $V_{IL}$ always $\geq V_{EE}$.

*Typicals used for testing purposes.

**Table 9. AC CHARACTERISTICS** $V_{CC}$ = 0 V; $V_{EE}$ = −3.465 V to −2.375 V or $V_{CC}$ = 2.375 V to 3.465 V; $V_{EE}$ = 0 V

| | | −40°C | | | 25°C | | | 70°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{OUTPP}$ | Output Voltage Amplitude ($f_{in}$ < 3 GHz)<br>(See Figure 3) (Note 18) ($f_{in}$ = 5.5 GHz) | 305<br>180 | 420<br>250 | | 305<br>150 | 420<br>220 | | 305<br>100 | 420<br>200 | | mV |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential<br>Output Enable<br>Clock Select | 250<br>430<br>400 | 300<br>550<br>450 | 350<br>700<br>500 | 250<br>430<br>400 | 300<br>550<br>450 | 350<br>700<br>500 | 250<br>430<br>400 | 300<br>600<br>480 | 350<br>750<br>550 | ps |
| $t_{SKEW}$ | Duty Cycle Skew (Note 19)<br>Within−Device Skew (Note 20)<br>Device−to−Device Skew (Note 21) | | 2<br>5<br>15 | 15<br>20<br>85 | | 2<br>5<br>15 | 15<br>20<br>85 | | 2<br>5<br>15 | 15<br>20<br>85 | ps |
| $t_S$ | Setup Time to CLK (EN to Selected CLK0:1) | 110 | 70 | | 110 | 70 | | 115 | 80 | | ps |
| $t_H$ | Hold Time (EN to Selected CLK0:1) | 110 | 70 | | 110 | 70 | | 115 | 80 | | ps |
| $t_{JITTER}$ | RMS Random Clock Jitter(Figure 3)<br>(Note 23) ($f_{in}$ = 5 GHz)<br>Peak−to−Peak Data Dependent Jitter<br>(Note 24) ($f_{in}$ = 5 Gb/s) | | 0.5 | 2.0 | | 0.5<br><br>14 | 2.0 | | 0.5 | 2.0 | ps |
| $V_{INPP}$ | Input Voltage Swing/Sensitivity<br>(Differential Configuration) (Note 22) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times (20% − 80%) @ 1 GHz<br>Q, $\overline{Q}$ | 40 | 60 | 80 | 40 | 60 | 80 | 40 | 60 | 80 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

18. Measured using a 500 mV source, 50% duty cycle clock source. All outputs loaded with 50 Ω to $V_{CC}$ − 1.5 V. Input edge rates 40 ps (20% − 80%).
19. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform (Figure 4).
20. Within−Device skew is measured between outputs under identical transitions and conditions on any one device.
21. Device−to−Device skew for identical transitions at identical $V_{CC}$ levels.
22. $V_{INPP}$ (MAX) cannot exceed $V_{CC} - V_{EE}$ (applicable only when $V_{CC} - V_{EE} < 2600$ mV).
23. Additive RMS jitter with 50% duty cycle clock signal at 5 GHz.
24. Additive Peak−to−Peak jitter with input NRZ data at PRBS $2^{31}-1$ at 5 Gb/s.

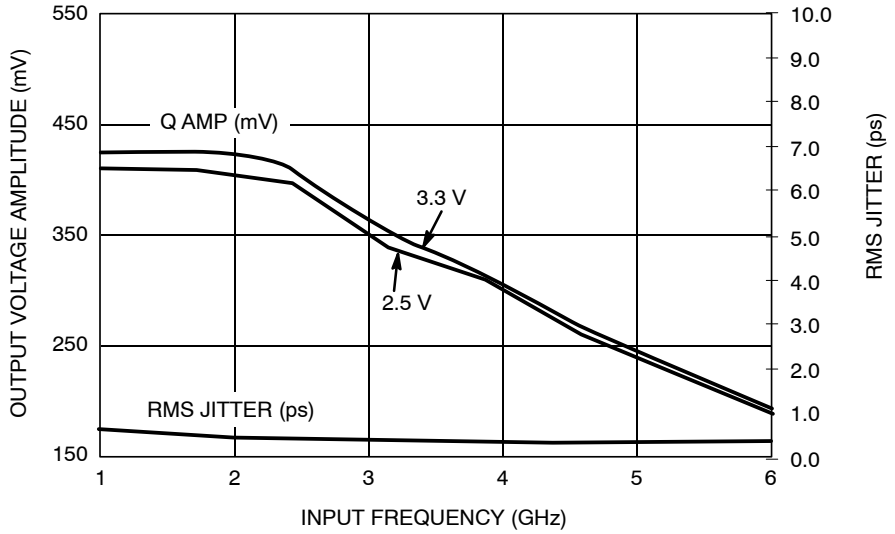



**Figure 3. Output Voltage Amplitude ($V_{OUTPP}$) / RMS Jitter vs. Input Frequency ($f_{in}$) at Ambient Temperature (Typical)**

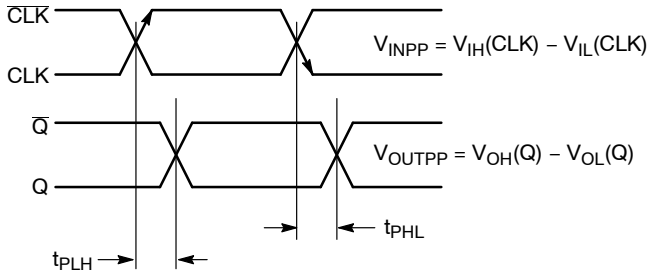



**Figure 4. AC Reference Measurement**

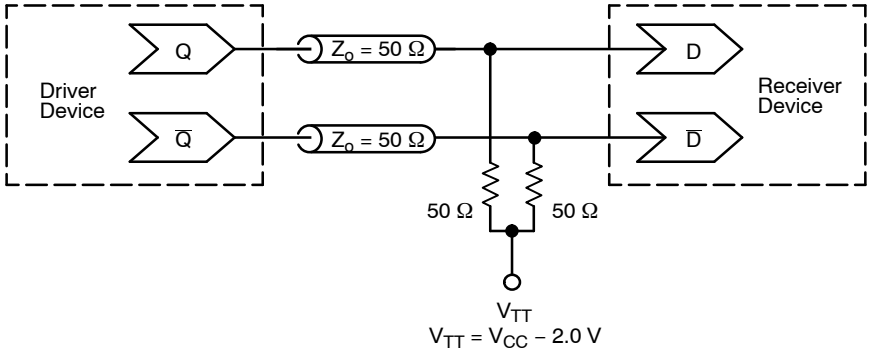



**Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)**

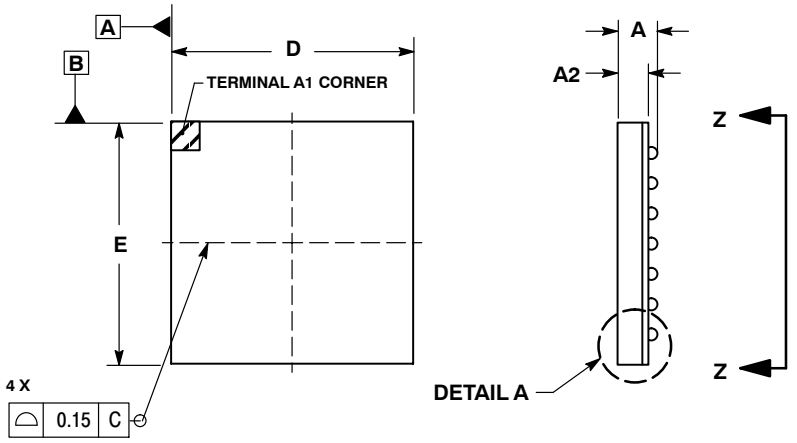
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NBSG111BAHTBG | FCBGA−49 (Pb−Free) | 100 / Tape & Reel |
| NBSG111BA | FCBGA−49 | 100 Units / Tray (Contact Sales Representative) |
| NBSG111BAR2 | FCBGA−49 | 500 / Tape & Reel (Contact Sales Representative) |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

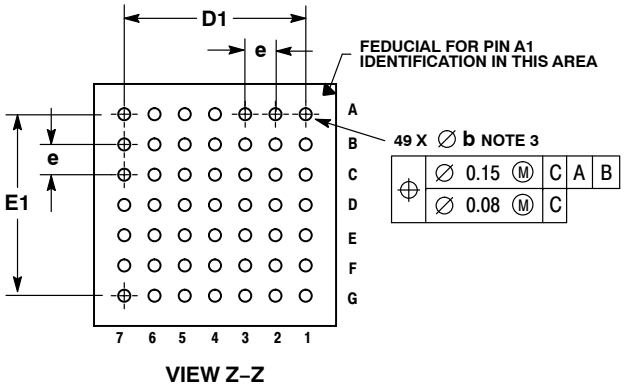
## PACKAGE DIMENSIONS

**FCBGA−49**
**BA SUFFIX**
PLASTIC 8x8 mm (1.0 mm pitch) BGA FLIP CHIP PACKAGE
CASE 489A−02
ISSUE A

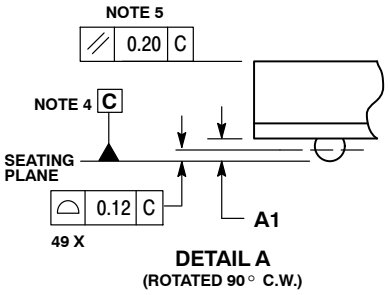



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
4. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. 489A−01 OBSOLETE, NEW STANDARD 489A−02.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 1.40 |
| A1 | 0.3 | 0.5 |
| A2 | 0.91 REF | |
| b | 0.40 | 0.60 |
| D | 8.00 BSC | |
| D1 | 6.00 BSC | |
| E | 8.00 BSC | |
| E1 | 6.00 BSC | |
| e | 1.00 BSC | |




VIEW Z−Z




DETAIL A
(ROTATED 90° C.W.)



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**NBSG111/D**