

# MC74VHC74

## Dual D-Type Flip-Flop with Set and Reset

The MC74VHC74 is an advanced high speed CMOS D-type flip-flop fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

Reset ( $\overline{RD}$ ) and Set ( $\overline{SD}$ ) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed:  $f_{max} = 170\text{MHz}$  (Typ) at  $V_{CC} = 5\text{V}$
- Low Power Dissipation:  $I_{CC} = 2\mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8\text{V}$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- Pb-Free Packages are Available\*

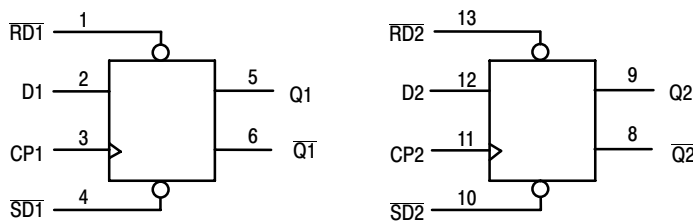


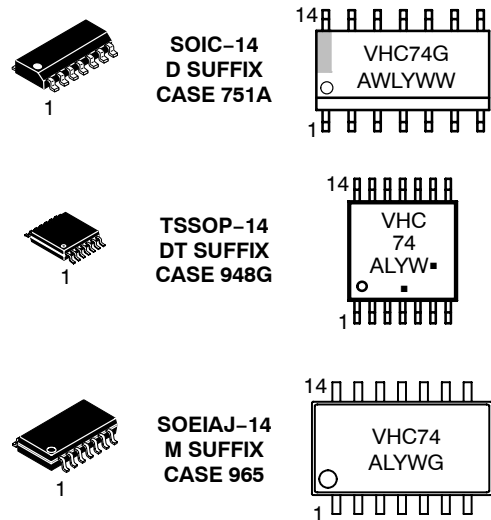
Figure 1. LOGIC DIAGRAM



ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAMS



A = Assembly Location  
 WL, L = Wafer Lot  
 Y, YY = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### FUNCTION TABLE

Inputs				Outputs	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H	↔	X	No Change	No Change

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74VHC74

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage	- 0.5 to + 7.0	V
V <sub>out</sub>	DC Output Voltage	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	- 20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	- 40	+ 85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 3.3V ±0.3V V <sub>CC</sub> = 5.0V ±0.5V	0 100 20	ns/V

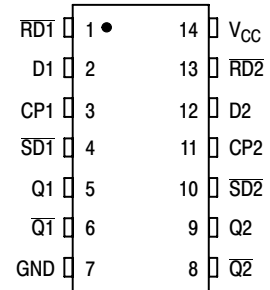


Figure 2. PIN ASSIGNMENT

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7			1.50 V <sub>CC</sub> × 0.7		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V <sub>CC</sub> × 0.3	0.50 V <sub>CC</sub> × 0.3		V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = - 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = - 4mA I <sub>OH</sub> = - 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4mA I <sub>OL</sub> = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5V or GND	0 to 5.5			±0.1	±1.0		μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			2.0	20.0		μA

# MC74VHC74

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, CP to Q or $\bar{Q}$	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		6.7	11.9	1.0	14.0	ns
		$C_L = 50\text{pF}$		9.2	15.4	1.0	17.5	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, $\overline{SD}$ or $\overline{RD}$ to Q or $\bar{Q}$	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		4.6	7.3	1.0	8.5	ns
		$C_L = 50\text{pF}$		6.1	9.3	1.0	10.5	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, $\overline{SD}$ or $\overline{RD}$ to Q or $\bar{Q}$	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$		7.6	12.3	1.0	14.5	ns
		$C_L = 50\text{pF}$		10.1	15.8	1.0	18.0	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$	80	125		70		MHz
		$C_L = 50\text{pF}$	50	75		45		
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$	130	170		110		MHz
		$C_L = 50\text{pF}$	90	115		75		
$C_{in}$	Maximum Input Capacitance			4	10		10	pF

Symbol	Parameter	Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0\text{V}$		Unit
		25		
$C_{PD}$	Power Dissipation Capacitance (Note 1)	25		pF

1.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$  (per flip-flop).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit		Unit
			$T_A = 25^\circ\text{C}$	$T_A = -40 \text{ to } 85^\circ\text{C}$	
$t_w$	Minimum Pulse Width, CP	$3.3 \pm 0.3$	6.0	7.0	ns
		$5.0 \pm 0.5$	5.0	5.0	
$t_w$	Minimum Pulse Width, $\overline{RD}$ or $\overline{SD}$	$3.3 \pm 0.3$	6.0	7.0	ns
		$5.0 \pm 0.5$	5.0	5.0	
$t_{su}$	Minimum Setup Time, D to CP	$3.3 \pm 0.3$	6.0	7.0	ns
		$5.0 \pm 0.5$	5.0	5.0	
$t_h$	Minimum Hold Time, D to CP	$3.3 \pm 0.3$	0.5	0.5	ns
		$5.0 \pm 0.5$	0.5	0.5	
$t_{rec}$	Minimum Recovery Time, $\overline{SD}$ or $\overline{RD}$ to CP	$3.3 \pm 0.3$	5.0	5.0	ns
		$5.0 \pm 0.5$	3.0	3.0	

## ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC74DR2	SOIC-14	2500 Tape & Reel
MC74VHC74DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74VHC74DT	TSSOP-14*	96 Units / Rail
MC74VHC74DTG	TSSOP-14*	96 Units / Rail
MC74VHC74DTR2	TSSOP-14*	2500 Tape & Reel
MC74VHC74DTR2G	TSSOP-14*	2500 Tape & Reel
MC74VHC74MEL	SOEIAJ-14	2000 Tape & Reel
MC74VHC74MELG	SOEIAJ-14 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74VHC74

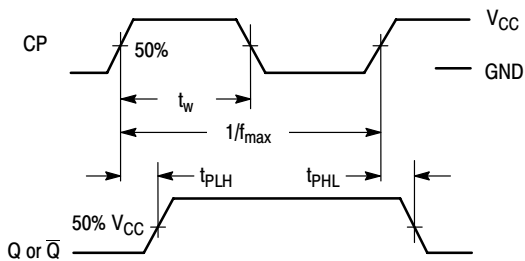


Figure 3.

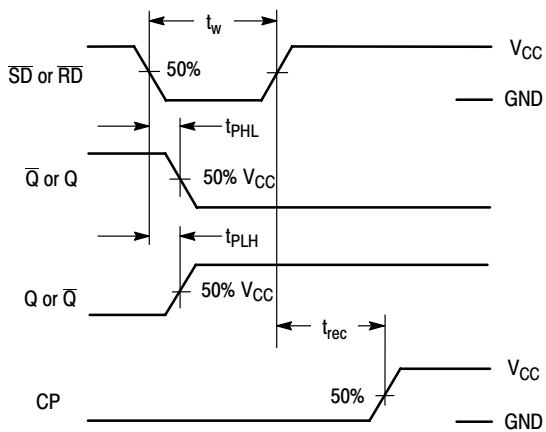


Figure 4.

## Switching Waveforms

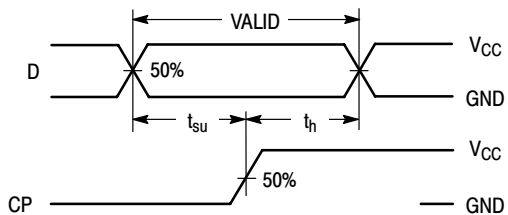
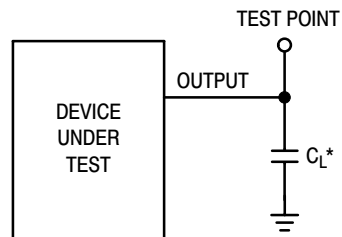


Figure 5.



\*Includes all probe and jig capacitance

Figure 6.

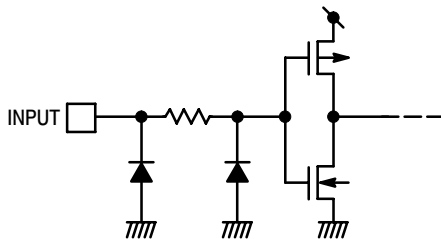
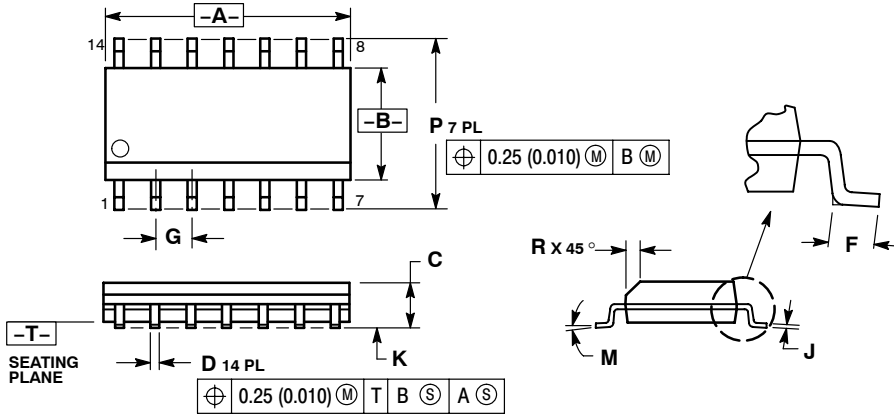


Figure 7. Input Equivalent Circuit

# MC74VHC74

## PACKAGE DIMENSIONS

SOIC-14  
D SUFFIX  
CASE 751A-03  
ISSUE G

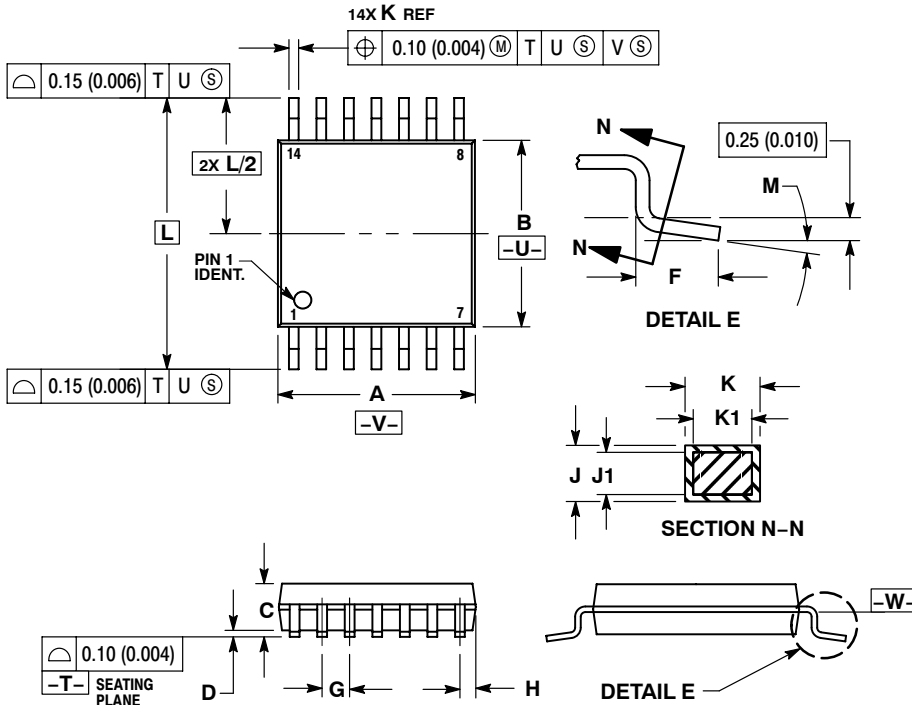


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14  
DT SUFFIX  
CASE 948G-01  
ISSUE A



NOTES:

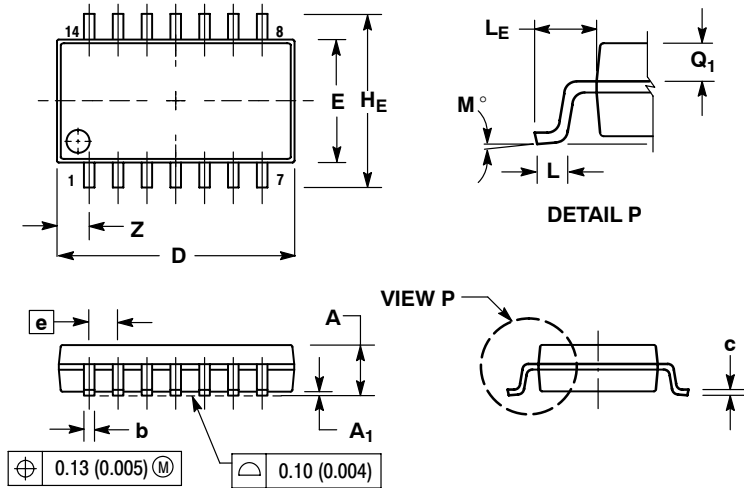
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# MC74VHC74

## PACKAGE DIMENSIONS

SOEIAJ-14  
M SUFFIX  
CASE 965-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85062-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.