

# NTD70N03R

## Power MOSFET

72 A, 25 V, N-Channel DPAK

### Features

- Planar HD3e Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{ISS}$  to Minimize Driver Loss
- Low Gate Charge
- Pb-Free Packages are Available

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	25	$V_{dc}$
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	$V_{dc}$
Thermal Resistance – Junction-to-Case Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Drain Current	$R_{\theta JC}$ $P_D$	2.4 62.5	$^\circ\text{C/W}$ W
– Continuous @ $T_C = 25^\circ\text{C}$ , Chip – Continuous @ $T_C = 25^\circ\text{C}$ , Limited by Package – Continuous @ $T_A = 25^\circ\text{C}$ , Limited by Wires – Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_D$	72.0	A
	$I_D$	62.8	A
	$I_D$	32	A
	$I_{DM}$	140	A
Thermal Resistance – Junction-to-Ambient (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ $P_D$ $I_D$	80 1.87 12.0	$^\circ\text{C/W}$ W A
Thermal Resistance – Junction-to-Ambient (Note 2) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ $P_D$ $I_D$	110 1.36 10.0	$^\circ\text{C/W}$ W A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 30 V_{dc}$ , $V_{GS} = 10 V_{dc}$ , $I_L = 12 A_{pk}$ , $L = 1 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	71.7	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 s	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

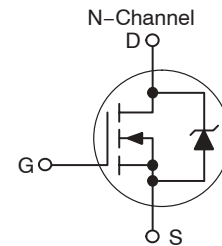
1. When surface mounted to an FR4 board using 0.5 sq. in. pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.



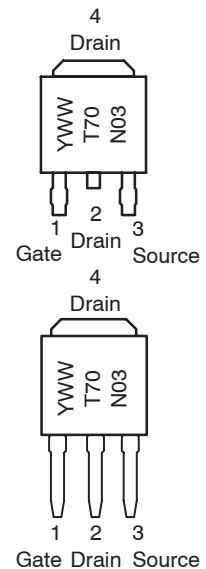
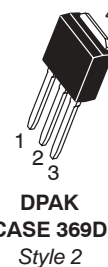
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
25 V	5.6 m $\Omega$	72 A



### MARKING DIAGRAMS



70N03 Device Code  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 501 of this data sheet.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 V <sub>dc</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Temperature Coefficient (Positive)	V <sub>(br)DSS</sub>	25 –	28 20.5	– –	V <sub>dc</sub> mV/°C	
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	– –	– –	1.5 10	μA <sub>dc</sub>	
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 V <sub>dc</sub> , V <sub>DS</sub> = 0 V <sub>dc</sub> )	I <sub>GSS</sub>	–	–	±100	nA <sub>dc</sub>	
<b>ON CHARACTERISTICS</b> (Note 3)						
Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 –	1.5 4.0	2.0 –	V <sub>dc</sub> mV/°C	
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 20 A <sub>dc</sub> ) (V <sub>GS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 20 A <sub>dc</sub> )	R <sub>DS(on)</sub>	– –	8.1 5.6	13 8.0	mΩ	
Forward Transconductance (Note 3) (V <sub>DS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 15 A <sub>dc</sub> )	g <sub>FS</sub>	–	27	–	Mhos	
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V, f = 1 MHz	C <sub>ISS</sub>	–	1333	–	pF
Output Capacitance		C <sub>OSS</sub>	–	600	–	
Transfer Capacitance		C <sub>RSS</sub>	–	218	–	
<b>SWITCHING CHARACTERISTICS</b> (Note 4)						
Turn-On Delay Time	V <sub>GS</sub> = 10 V <sub>dc</sub> , V <sub>DD</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 36 A <sub>dc</sub> , R <sub>G</sub> = 3 Ω	t <sub>d(on)</sub>	–	6.9	–	ns
Rise Time		t <sub>r</sub>	–	1.3	–	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	18.4	–	
Fall Time		t <sub>f</sub>	–	5.5	–	
Gate Charge	V <sub>GS</sub> = 5 V <sub>dc</sub> , I <sub>D</sub> = 36 A <sub>dc</sub> , V <sub>DS</sub> = 10 V <sub>dc</sub> (Note 3)	Q <sub>T</sub>	–	13.2	–	nC
		Q <sub>GS</sub>	–	3.3	–	
		Q <sub>DS</sub>	–	6.5	–	
<b>SOURCE-DRAIN DIODE CHARACTERISTICS</b>						
Forward On-Voltage	(I <sub>S</sub> = 20 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (Note 3) (I <sub>S</sub> = 20 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 125°C)	V <sub>SD</sub>	– –	0.86 0.73	1.2 –	V <sub>dc</sub>
Reverse Recovery Time	I <sub>S</sub> = 36 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , dI <sub>S</sub> /dt = 100 A/μs (Note 3)	t <sub>rr</sub>	–	15.6	–	ns
		t <sub>a</sub>	–	13.8	–	
		t <sub>b</sub>	–	1.78	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.004	–	μC

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

4. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

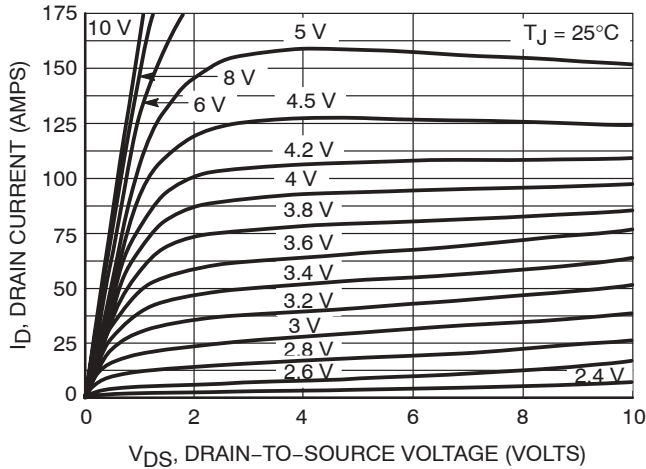


Figure 1. On-Region Characteristics

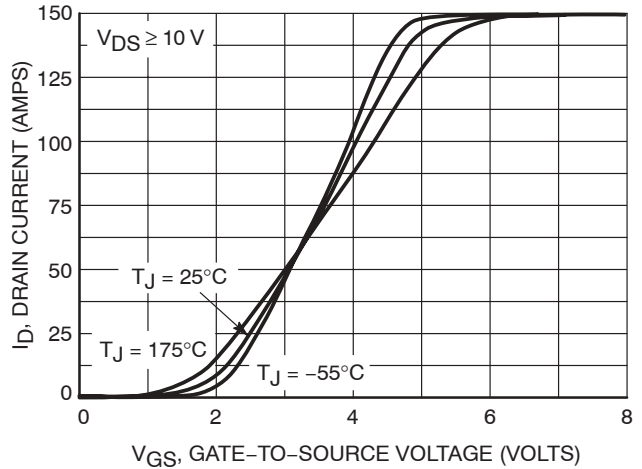


Figure 2. Transfer Characteristics

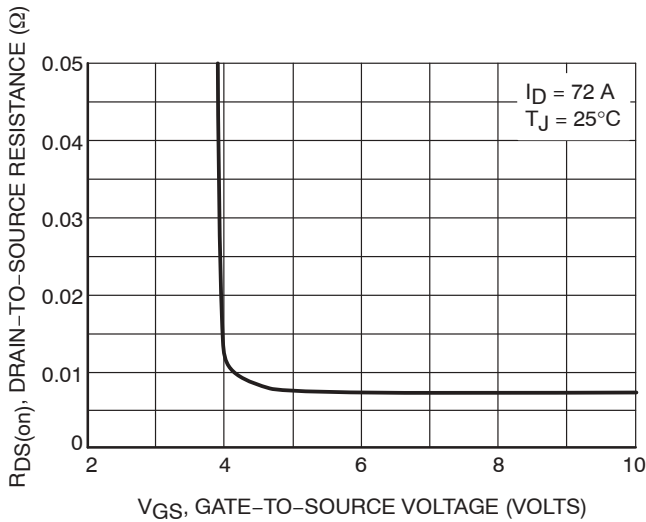


Figure 3. On-Resistance versus Gate-to-Source Voltage

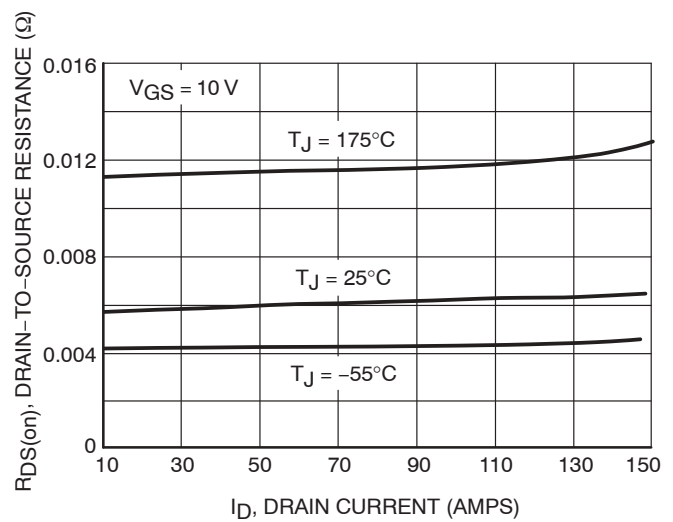


Figure 4. On-Resistance versus Drain Current and Gate Voltage

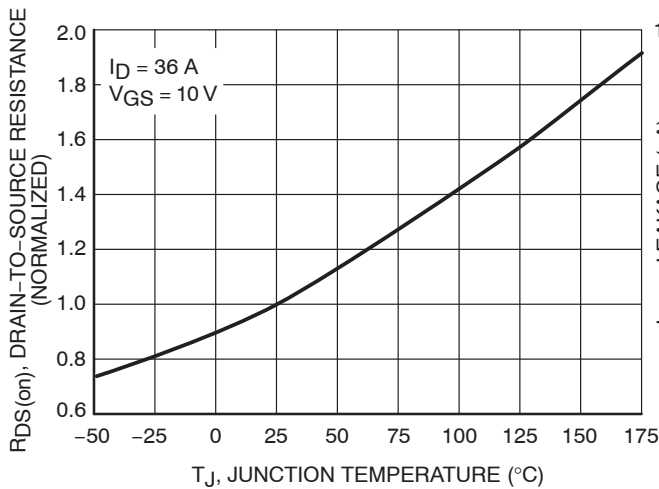


Figure 5. On-Resistance Variation with Temperature

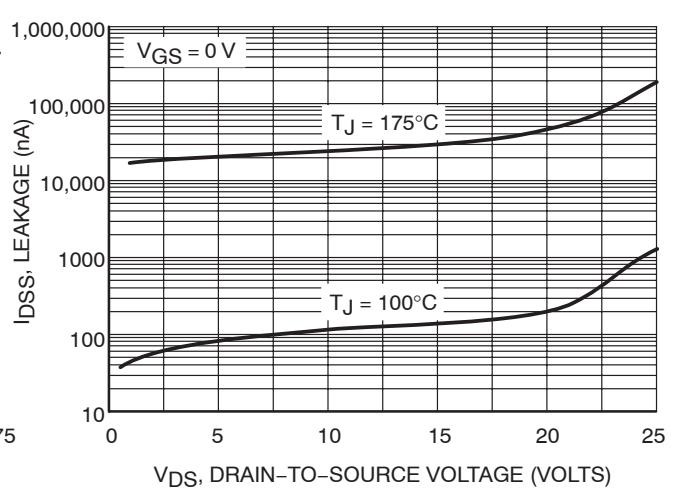


Figure 6. Drain-to-Source Leakage Current versus Voltage

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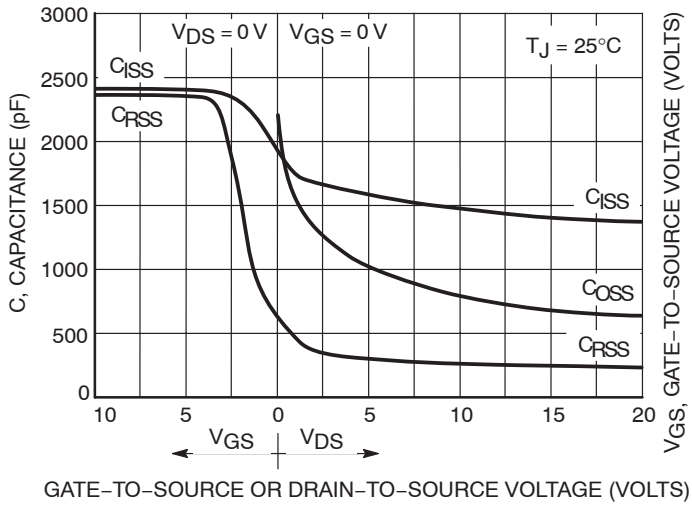


Figure 7. Capacitance Variation

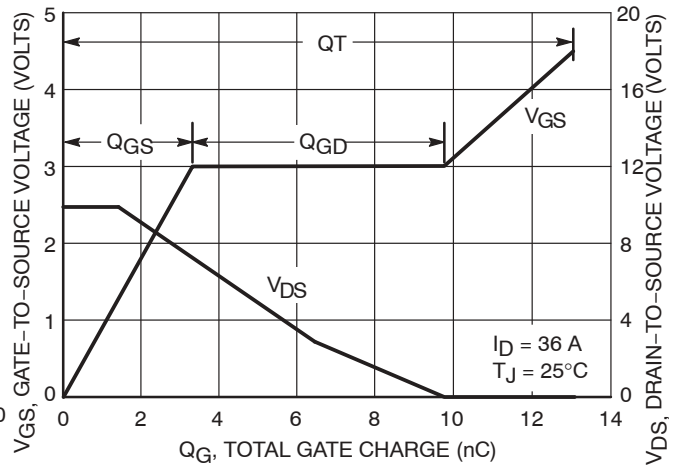


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

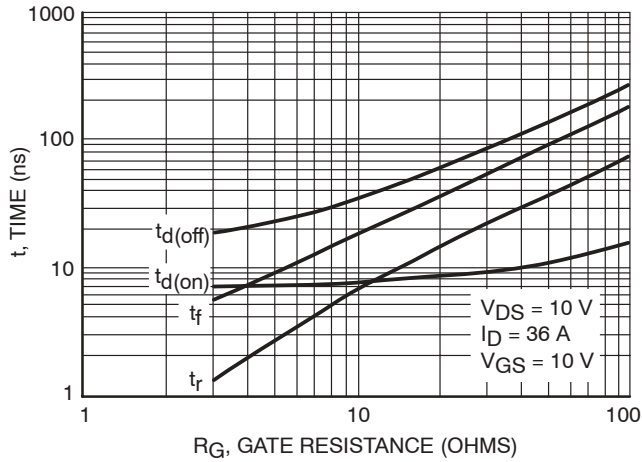


Figure 9. Resistive Switching Time Variation versus Gate Resistance

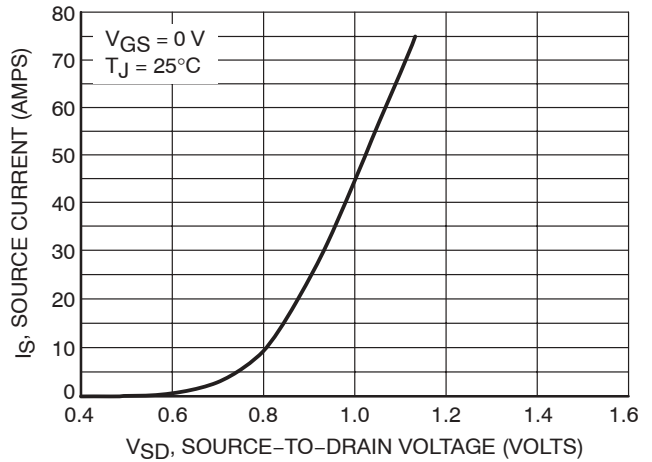


Figure 10. Diode Forward Voltage versus Current

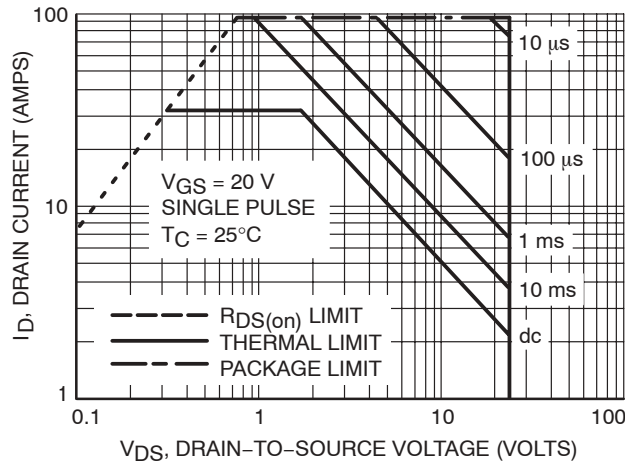
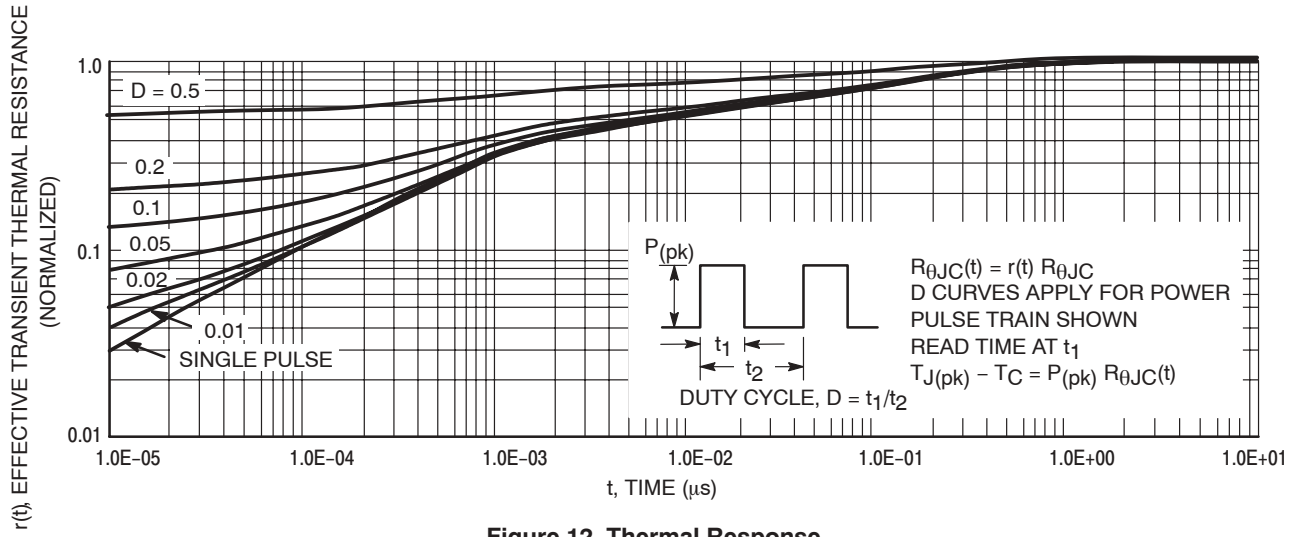


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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**Figure 12. Thermal Response**

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## ORDERING INFORMATION

Order Number	Package	Shipping†
NTD70N03R	DPAK-3	75 Units / Rail
NTD70N03RG	DPAK-3 (Pb-Free)	75 Units / Rail
NTD70N03RT4	DPAK-3	2500 / Tape & Reel
NTD70N03RT4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD70N03R-1	DPAK-3 Straight Lead	75 Units / Rail
NTD70N03R-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail
NTD70N03R-001	DPAK	75 Units / Rail
NTD70N03R-001G	DPAK (Pb-Free)	75 Units / Tubes

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.