# MC74LVX374

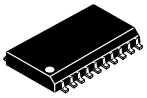
# Octal D-Type Flip-Flop with 3-State Outputs

## With 5V–Tolerant Inputs

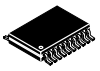
The MC74LVX374 is an advanced high speed CMOS octal D–type flip–flop with 3–state outputs. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

This 8–bit D–type flip–flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

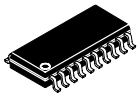
- High Speed: $f_{max}$ = 160MHz (Typ) at $V_{CC}$ = 3.3V
- Low Power Dissipation: $I_{CC}$ = 4μA (Max) at $T_A$ = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP}$ = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V



**DW SUFFIX**
20–LEAD SOIC PACKAGE
CASE 751D–04



**DT SUFFIX**
20–LEAD TSSOP PACKAGE
CASE 948E–02



**M SUFFIX**
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

**PIN NAMES**

| Pins | Function |
|---|---|
| $\overline{OE}$ | Output Enable Input |
| CP | Clock Pulse Input |
| D0–D7 | Data Inputs |
| O0–O7 | 3–State Outputs |

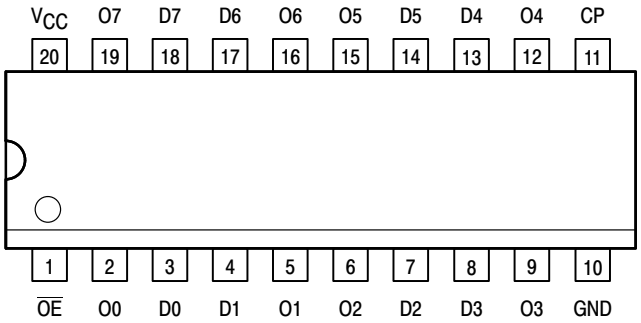



**Figure 1. 20–Lead Pinout (Top View)**



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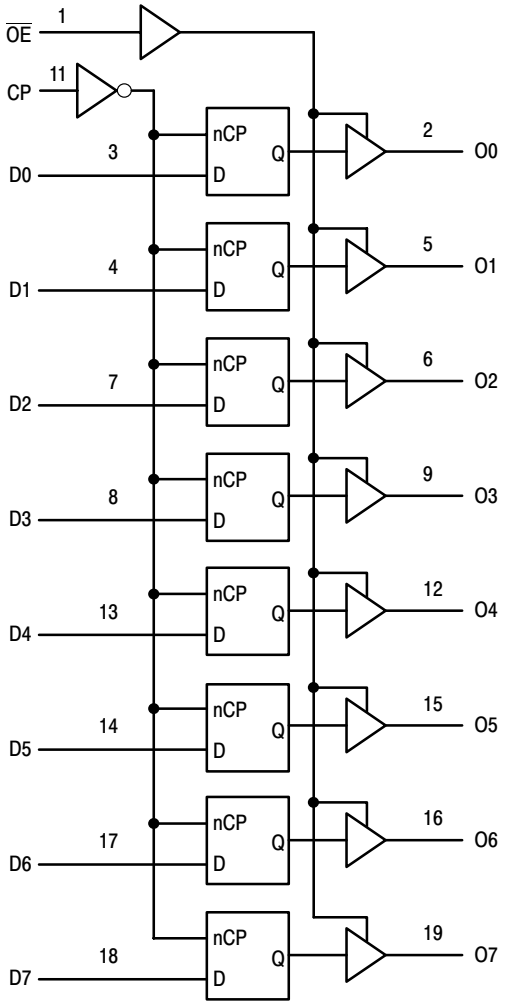



**Figure 2. Logic Diagram**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{OE}$ | CP | Dn | On | OPERATING MODE |
| L<br>L | ↑<br>↑ | l<br>h | L<br>H | Load and Read Register |
| L | ↥ | X | NC | Hold and Read Register |
| H | ↥ | X | Z | Hold and Disable Outputs |
| H<br>H | ↑<br>↑ | l<br>h | Z<br>Z | Load Internal Register and Disable Outputs |

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change, State Prior to Low–to–High Clock Transition; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↑ = Low–to–High Transition; ↥ = Not a Low–to–High Transition; For $I_{CC}$ Reasons DO NOT FLOAT Inputs

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | –0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage | –0.5 to +7.0 | V |
| $V_{out}$ | DC Output Voltage | –0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | Input Diode Current | –20 | mA |
| $I_{OK}$ | Output Diode Current | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±75 | mA |
| $P_D$ | Power Dissipation | 180 | mW |
| $T_{stg}$ | Storage Temperature | –65 to +150 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | 2.0 | 3.6 | V |
| $V_{in}$ | DC Input Voltage | 0 | 5.5 | V |
| $V_{out}$ | DC Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | –40 | +85 | °C |
| $\Delta t/\Delta V$ | Input Rise and Fall Time | 0 | 100 | ns/V |

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $T_A$ = 25°C | | | $T_A$ = – 40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | High–Level Input Voltage | | 2.0<br>3.0<br>3.6 | 1.5<br>2.0<br>2.4 | | | 1.5<br>2.0<br>2.4 | | V |
| $V_{IL}$ | Low–Level Input Voltage | | 2.0<br>3.0<br>3.6 | | | 0.5<br>0.8<br>0.8 | | 0.5<br>0.8<br>0.8 | V |
| $V_{OH}$ | High–Level Output Voltage ($V_{in}$ = $V_{IH}$ or $V_{IL}$) | $I_{OH}$ = –50μA<br>$I_{OH}$ = –50μA<br>$I_{OH}$ = –4mA | 2.0<br>3.0<br>3.0 | 1.9<br>2.9<br>2.58 | 2.0<br>3.0 | | 1.9<br>2.9<br>2.48 | | V |
| $V_{OL}$ | Low–Level Output Voltage ($V_{in}$ = $V_{IH}$ or $V_{IL}$) | $I_{OL}$ = 50μA<br>$I_{OL}$ = 50μA<br>$I_{OL}$ = 4mA | 2.0<br>3.0<br>3.0 | | 0.0<br>0.0 | 0.1<br>0.1<br>0.36 | | 0.1<br>0.1<br>0.44 | V |
| $I_{in}$ | Input Leakage Current | $V_{in}$ = 5.5V or GND | 3.6 | | | ±0.1 | | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three–State Leakage Current | $V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 3.6 | | | ±0.25 | | ±2.5 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{in}$ = $V_{CC}$ or GND | 3.6 | | | 4.0 | | 40.0 | μA |

**AC ELECTRICAL CHARACTERISTICS** (Input $t_r = t_f = 3.0$ns)

| Symbol | Parameter | Test Conditions | $T_A = 25°C$ Min | $T_A = 25°C$ Typ | $T_A = 25°C$ Max | $T_A = -40$ to $85°C$ Min | $T_A = -40$ to $85°C$ Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency (50% Duty Cycle) | $V_{CC}$ = 2.7V $C_L$ = 15pF | 60 | 115 | | 50 | | MHz |
| | | $V_{CC}$ = 2.7V $C_L$ = 50pF | 45 | 60 | | 40 | | |
| | | $V_{CC}$ = 3.3 ± 0.3V $C_L$ = 15pF | 100 | 160 | | 85 | | |
| | | $V_{CC}$ = 3.3 ± 0.3V $C_L$ = 50pF | 60 | 95 | | 55 | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay CP to O | $V_{CC}$ = 2.7V $C_L$ = 15pF | | 8.5 | 16.3 | 1.0 | 19.5 | ns |
| | | $V_{CC}$ = 2.7V $C_L$ = 50pF | | 11.0 | 19.8 | 1.0 | 23.0 | |
| | | $V_{CC}$ = 3.3 ± 0.3V $C_L$ = 15pF | | 6.7 | 10.6 | 1.0 | 12.5 | |
| | | $V_{CC}$ = 3.3 ± 0.3V $C_L$ = 50pF | | 9.2 | 14.1 | 1.0 | 16.0 | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time $\overline{OE}$ to O | $V_{CC}$ = 2.7V $C_L$ = 15pF $R_L$ = 1kΩ | | 7.6 | 14.5 | 1.0 | 17.5 | ns |
| | | $V_{CC}$ = 2.7V $C_L$ = 50pF $R_L$ = 1kΩ | | 10.1 | 18.0 | 1.0 | 21.0 | |
| | | $V_{CC}$ = 3.3 ± 0.3V $C_L$ = 15pF $R_L$ = 1kΩ | | 5.9 | 9.3 | 1.0 | 11.0 | |
| | | $V_{CC}$ = 3.3 ± 0.3V $C_L$ = 50pF $R_L$ = 1kΩ | | 8.4 | 12.8 | 1.0 | 14.5 | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to O | $V_{CC}$ = 2.7V $C_L$ = 50pF $R_L$ = 1kΩ | | 11.5 | 18.5 | 1.0 | 22.0 | ns |
| | | $V_{CC}$ = 3.3 ± 0.3V $C_L$ = 50pF $R_L$ = 1kΩ | | 9.6 | 13.2 | 1.0 | 15.0 | |
| $t_{OSHL}$ $t_{OSLH}$ | Output–to–Output Skew (Note 1.) | $V_{CC}$ = 2.7V $C_L$ = 50pF | | | 1.5 | | 1.5 | ns |
| | | $V_{CC}$ = 3.3 ±0.3V $C_L$ = 50pF | | | 1.5 | | 1.5 | |

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW ($t_{OSHL}$) or LOW–to–HIGH ($t_{OSLH}$); parameter guaranteed by design.

**CAPACITIVE CHARACTERISTICS**

| Symbol | Parameter | $T_A = 25°C$ Min | $T_A = 25°C$ Typ | $T_A = 25°C$ Max | $T_A = -40$ to $85°C$ Min | $T_A = -40$ to $85°C$ Max | Unit |
|---|---|---|---|---|---|---|---|
| $C_{in}$ | Input Capacitance | | 4 | 10 | | 10 | pF |
| $C_{out}$ | Maximum Three–State Output Capacitance | | 6 | | | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 2.) | | 32 | | | | pF |

2. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip–flop). $C_{PD}$ is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

**NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

| Symbol | Characteristic | $T_A = 25°C$ Typ | $T_A = 25°C$ Max | Unit |
|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 0.5 | 0.8 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | –0.5 | –0.8 | V |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

**TIMING REQUIREMENTS** (Input $t_r = t_f = 3.0$ns)

| Symbol | Parameter | Test Conditions | $T_A = 25°C$ | | $T_A = -40$ to $85°C$ | Unit |
|---|---|---|---|---|---|---|
| | | | Typ | Limit | Limit | |
| $t_w$ | Minimum Pulse Width, CP | $V_{CC}$ = 2.7V<br>$V_{CC}$ = 3.3 ±0.3V | | 7.5<br>5.0 | 8.0<br>5.5 | ns |
| $t_{su}$ | Minimum Setup Time, D to CP | $V_{CC}$ = 2.7V<br>$V_{CC}$ = 3.3 ±0.3V | | 6.5<br>4.5 | 6.5<br>4.5 | ns |
| $t_h$ | Minimum Hold Time, D to CP | $V_{CC}$ = 2.7V<br>$V_{CC}$ = 3.3 ±0.3V | | 2.0<br>2.0 | 2.0<br>2.0 | ns |

## SWITCHING WAVEFORMS

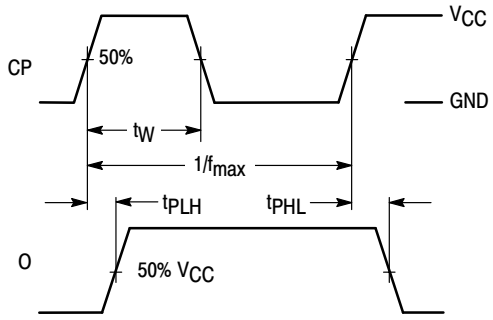



**Figure 3.**

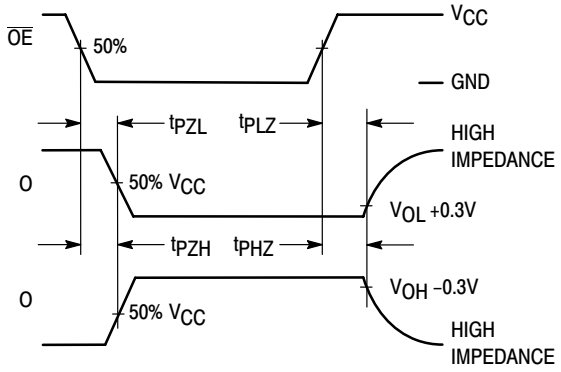



**Figure 4.**

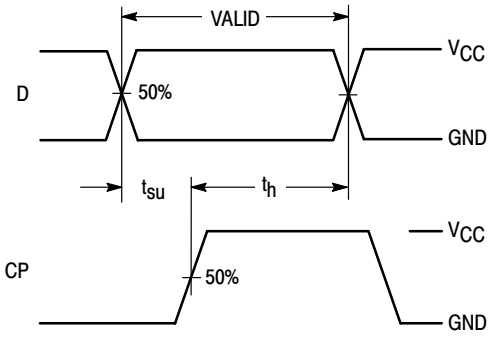
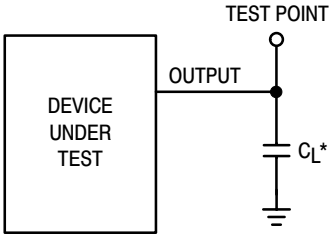


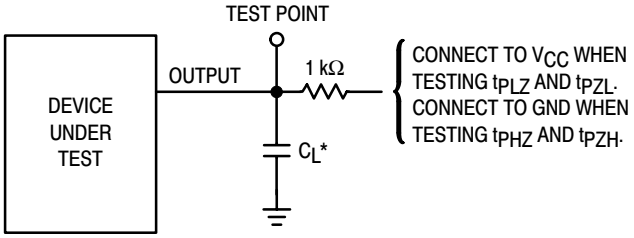

**Figure 5.**

## TEST CIRCUITS




*Includes all probe and jig capacitance

**Figure 6. Propagation Delay Test Circuit**




*Includes all probe and jig capacitance

**Figure 7. Three–State Test Circuit**