NCP1605, NCP1605A, NCP1605B

Enhanced, High Voltage and Efficient Standby Mode, Power Factor Controller

The NCP1605 is a controller that exhibits near−unity power factor while operating in fixed frequency, Discontinuous Conduction Mode (DCM) or in Critical Conduction Mode (CRM).

Housed in a SOIC−16 package, the circuit incorporates all the features necessary for building robust and compact PFC stages, with a minimum of external components. In addition, it integrates the skip cycle capability to lower the standby losses to a minimum.

General Features

- Near−Unity Power Factor
- Fixed Frequency, Discontinuous Conduction Mode Operation
- Critical Conduction Mode Achievable in Most Stressful Conditions
- Lossless High Voltage Current Source for Startup
- Soft Skip™ Cycle for Low Power Standby Mode
- Switching Frequency up to 250 kHz
- Synchronization Capability
- Fast Line / Load Transient Compensation
- Valley Turn On
- High Drive Capability: −500 mA / +800 mA
- Signal to Indicate that the PFC is Ready for Operation ("pfcOK" Pin)
- V_{CC} range: from 10 V to 20 V
- Follower Boost Operation
- Two V_{CC} Turn−On Threshold Options: 15 V for NCP1605 & NCP1605B; 10.5 V for NCP1605A
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Safety Features

- Output Under and Overvoltage Protection
- Brown−Out Detection
- Soft−Start for Smooth Startup Operation
- Overcurrent Limitation
- Zero Current Detection Protecting the PFC stage from Inrush Currents
- Thermal Shutdown
- Latched Off Capability

Typical Applications

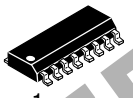
- PC Power Supplies
- All Off Line Appliances Requiring Power Factor Correction

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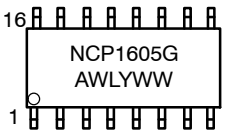
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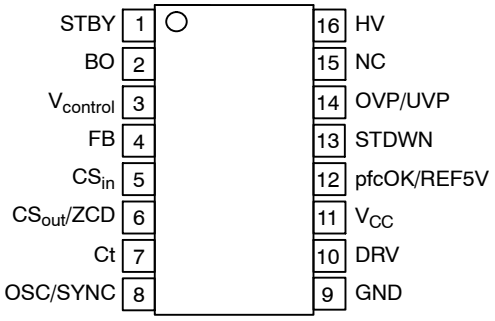
SOIC−16
D SUFFIX
CASE 751B





x = A or B
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1605DR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel
NCP1605ADR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel
NCP1605BDR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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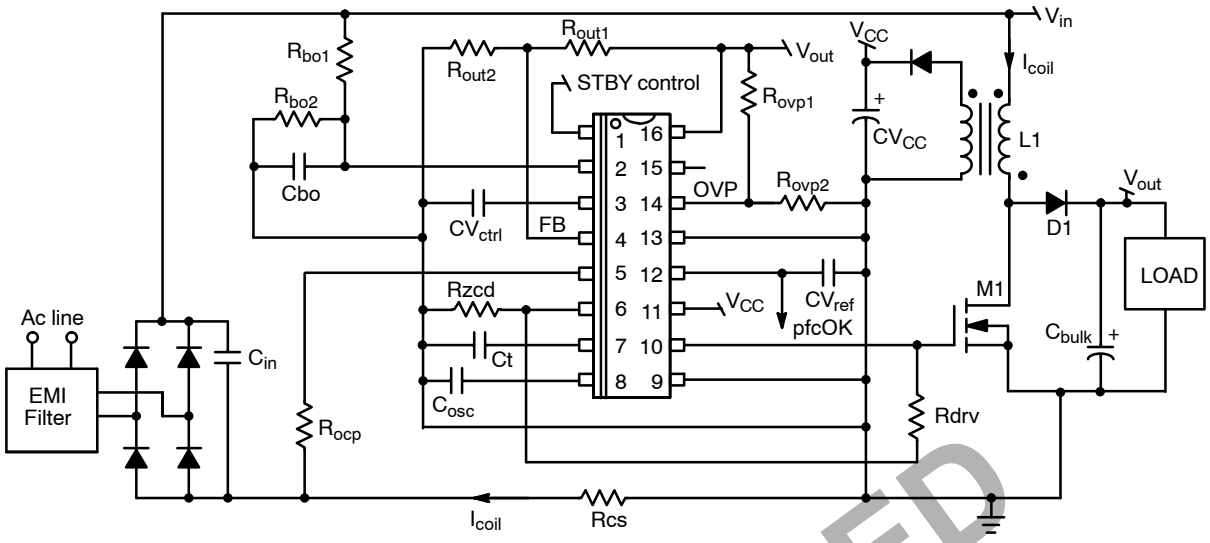


Figure 1.

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MAXIMUM RATINGS

Pin	Rating	Symbol	Value	Unit
11	Power Supply Input	V_{CC}	−0.3, +20	V
11	Maximum Transient Voltage (Note 1)	V_{CC}	−0.3, +25	V
1, 2, 4, 5, 6, 7, 8, 13 and 14	Input Voltage	V_I	−0.3, +9	V
6	Maximum Current	$I_{CSOUT/ZCD}$	−3, 10	mA
3	$V_{CONTROL}$ Pin	$V_{CONTROL}$	−0.3, $V_{CONTROL}$ MAX (Note 2)	V
16	High Voltage Pin	V_{HV}	−0.3, 600 V	V
	Power Dissipation and Thermal Characteristics: Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction−to−Air	 P_D $R_{\theta JA}$	 550 145	 mW °C/W
	Operating Junction Temperature Range	T_J	−55 to +125	°C
	Maximum Junction Temperature	T_{Jmax}	150	°C
	Storage Temperature Range	T_{Smax}	−65 to +150	°C
	Lead Temperature (Soldering, 10 s)	T_{Lmax}	300	°C
	ESD Capability, HBM Model (all pins except HV) (Note 3)	HBM	2000	V
	ESD Capability, MM Model (all pins except HV) (Note 3)	MM	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The maximum transient voltage with a corresponding maximum transient current at 100 mA. The maximum transient power handling capability must be observed as well.
2. "$V_{CONTROL}$MAX" is the pin clamp voltage.
3. This device series contains ESD protection rated using the following tests:
   Human Body Model (HBM) 2000V per JEDEC Standard JESD22, Method A114E.
   Machine Model (MM) 200V per JEDEC Standard JESD22, Method A115A.
4. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

TYPICAL ELECTRICAL CHARACTERISTICS

(Conditions: V_{CC} = 16 V, V_{HV} = 50 V, V_{Pin2} = 2 V, V_{Pin13} = 0 V, T_J from 0°C to +125°C, unless otherwise specified;
For NCP1605DR2G: for typical values T_J = 25°C, for min/max values T_J = −55°C to +125°C, unless otherwise specified) (Note 7)

Symbol	Rating	Min	Typ	Max	Unit
Gate Drive Section					
T_{rise}	Output Voltage Rise Time @ C_L = 1 nF, from 1 V to 10 V	–	40	–	ns
T_{fall}	Output Voltage Fall Time @ C_L = 1 nF, from 10 V to 1 V	–	20	–	ns
R_{OH}	Source Resistance @ I_{Pin10} = 100 mA	–	15	25	Ω
I_{source}	Source Current capability (@ V_{Pin10} = 0 V)	–	500	–	mA
R_{OL}	Sink Resistance @ I_{Pin10} = 100 mA	–	7	15	Ω
I_{sink}	Sink Current Capability (@ V_{Pin10} = 10 V)	–	800	–	mA
Regulation Block					
V_{REF}	Voltage Reference NCP1605/A NCP1605B	2.425 2.430	2.500 2.500	2.575 2.550	V
I_{EA}	Error Amplifier Current Capability	–	±20	–	μA
G_{EA}	Error Amplifier Gain	100	200	300	μS
IB_{Pin4}	Pin 4 Bias Current @ V_{Pin4} = V_{REF}	−500	–	500	nA
$V_{CONTROL}$ – $V_{CONTROL}$MAX – $V_{CONTROL}$MIN – Δ $V_{CONTROL}$I	Pin 2 Voltage: – @ V_{Pin4} = 2 V – @ V_{Pin4} = 3 V	 – – 2.7	 3.6 0.6 3.0	 – – 3.3	V
V_{OUT}L / V_{REF}	Ratio (V_{OUT} Low Detect Threshold / V_{REF}) (Note 6)	95.0	95.5	96.0	%
H_{OUT}L / V_{REF}	Ratio (V_{OUT} Low Detect Hysteresis / V_{REF}) (Note 6)	–	–	0.5	%
I_{BOOST}	Pin 2 Source Current when (V_{OUT} Low Detect) is activated	190	240	290	μA
Shutdown Block					
$I_{LEAKAGE}$	Current Sourced by Pin 13 @ V_{Pin14} = 2.3 V	−500	–	500	nA
V_{STDWN}	Pin 13 Threshold for Shutdown	2.375	2.500	2.625	V
Over and Under Voltage Protections					
V_{OVP}	Overvoltage Protection Threshold	2.425	2.500	2.575	V
V_{OVP} / V_{REF}	Ratio (V_{OVP} / V_{REF}) (Note 5)	99.5	100.0	100.5	%
V_{UVP} / V_{REF}	Ratio UVP threshold over V_{REF}	8	12	16	%
IB_{Pin14}	Pin 13 Bias Current: @ V_{Pin14} = V_{OVP} @ V_{Pin14} = V_{UVP}	 −500 −500	 – –	 500 500	nA
Ramp Control					
I_{RAMP} – 1.00 V	Pin 7 Source Current: @ V_{Pin4} = 1.00 V T_J = 0°C to +125°C NCP1605, T_J = −40°C to +125°C NCP1605, T_J = −55°C to +125°C	 54 52 51	 60 – –	 69 69 69	μA
I_{RAMP} – 1.75 V I_{RAMP} – 2.50 V	Pin 7 Source Current: @ V_{Pin4} = 1.75 V @ V_{Pin4} = 2.50 V	 156 313	 182 370	 214 428	μA
Vcl_ff	Pin 7 Clamp Voltage @ V_{Pin4} = V_{Pin2} = 2 V and V_{Pin6} = 0 V	–	5	–	V
V_{CL}CRM	Pin 7 Clamp Voltage @ V_{Pin4} = 0 V, V_{Pin2} = 2 V and V_{Pin6} = 1 V	0.9	1	1.1	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Not tested; guaranteed by characterization
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7. For coldest temperature, QA sampling at −40°C in production and −55°C specification is Guaranteed by Characterization.

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TYPICAL ELECTRICAL CHARACTERISTICS

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For NCP1605DR2G: for typical values T_J = 25°C, for min/max values T_J = −55°C to +125°C, unless otherwise specified) (Note 7)

Symbol	Rating	Min	Typ	Max	Unit
R_{CT}	Ratio (Pin 7 Clamp Voltage / (Pin 7 Charge Current) ($V_{CL}CRM$ / I_{RAMP}) @ V_{Pin6} = 0 V and				kΩ
	− V_{Pin4} = 1.00 V	−	16.7	−	
	− V_{Pin4} = 1.75 V	−	5.4	−	
	− V_{Pin4} = 2.50 V	−	2.7	−	
$T_{ON}MIN$	Delay (V_{Pin7} > 5 V) to (DRV low)	−	90	200	ns
C_{INT}	Average Pin 7 Internal Capacitance (V_{Pin7} varying from 0 and 1 V) Guaranteed by design	−	15	25	pF
V_{INIT}	Maximum Pin 7 Voltage Allowing the Setting of the PWM Latch	−	50	90	mV
I_{RAMP_SINK}	Pin 7 Sink Current (Drive low) @ V_{Pin7} = 1 V	−	10	−	mA
Current Sense Block					
Off100	Current Sense Pin Voltage, 100 μA being drawn from Pin 5 NCP1605/A	−20	6.0	20	mV
	NCP1605B	−5.0	6.0	15	
Off10	Current Sense Pin Voltage, 10 μA being drawn from Pin 5	3.0	8.0	13	mV
I_{MAX}	Overcurrent Protection Threshold	230	250	265	μA
T_{OCP}	(Ipin5 > 250 μA) to (DRV low) Propagation Delay (Note 5)	−	100	200	ns
K_{CS10}	Ratio (I_{Pin6}/I_{Pin5}) @ I_{Pin5} = 10 μA	99	108	117	%
K_{CS200}	Ratio (I_{Pin6}/I_{Pin5}) @ I_{Pin5} = 200 μA	98	101	103	%
V_{ZCD}	Pin 6 Comparator Threshold	50	100	200	mV
T_{ZCD}	Delay from (V_{Pin6} < V_{ZCD}) to (DRV high)	−	120	240	ns
Standby Input					
V_{STBY}	Standby Mode Threshold (V_{Pin1} falling)	280	310	340	mV
H_{STBY}	Hysteresis for Standby Mode Detection	25	30	50	mV
$V_{SKIP}OUT$ / $V_{OUT}L$	Ratio (Pin 4 Voltage to terminate a SKIP period) over the (V_{OUT} Low Detect Threshold) (Note 6)	99	100	101	%
Oscillator / Synchronization Block					
I_{charge}	Oscillator Charge Current				μA
	T_J = 0°C to +125°C	90	100	110	
	NCP1605, T_J = −40°C to +125°C	89	−	110	
	NCP1605, T_J = −55°C to +125°C	88	−	110	
I_{disch}	Oscillator Discharge Current				μA
	T_J = 0°C to +125°C	90	100	110	
	NCP1605, T_J = −40°C to +125°C	89	−	110	
	NCP1605, T_J = −55°C to +125°C	88	−	110	
V_{sync_H}	Comparator Upper Threshold	−	3.0	−	V
V_{sync_L}	Comparator Lower Threshold	−	2.0	−	V
Swing	Comparator Swing (V_{sync_H} − V_{sync_L})	0.9	1.0	1.1	V
T_{sync_min}	Minimum Synchronization Pulse Width for Detection	−	−	500	ns
pfcOK / REF5V					
$V_{pfcOK}L$	Pin 12 Voltage @ V_{Pin13} = 5 V, 250 μA being sunk by Pin 12	−	60	120	mV

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For NCP1605DR2G: for typical values T_J = 25°C, for min/max values T_J = −55°C to +125°C, unless otherwise specified) (Note 7)

Symbol	Rating		Min	Typ	Max	Unit
$V_{pfcOK}H$	(Pin 12 Voltage @ V_{Pin13} = 0 V and V_{Pin3} = 5 V, with a 250 μA sourced by Pin 12)	NCP1605/A NCP1605B	4.7 4.75	5.0 5.0	5.3 5.3	V
	(Pin 12 Voltage @ V_{Pin13} = 0 V and V_{Pin3} = 5 V, with a 5 mA sourced by Pin 12)	NCP1605/A NCP1605B	4.5 4.5	5.0 4.72	5.3 5.0	
Icap_ref	Current Capability		5 .0	10	–	mA
Brown−Out Detection Block						
V_{BOH}	Brown−Out Comparator Threshold (V_{Pin2} rising)	NCP1605/A NCP1605B	0.9 0.93	1.0 1.0	1.1 1.07	V
V_{BOL}	Brown−Out Comparator Threshold (V_{Pin2} falling)	NCP1605/A NCP1605B	0.45 0.465	0.50 0.50	0.55 0.535	V
IB_{BO}	Pin 2 Bias Current @ V_{Pin2} = 0.5 V and 1 V		−500	–	500	nA
Thermal Shutdown						
T_{LIMIT}	Thermal Shutdown Threshold		–	155	–	°C
H_{TEMP}	Thermal Shutdown Hysteresis		–	15	–	°C
V_{CC} UNDERVOLTAGE Lockout Section						
$V_{CC}ON$	Turn on Threshold Level, V_{CC} Raising Up	NCP1605 NCP1605A NCP1605B	14 9.5 14.2	15 10.5 15	16 11.5 15.55	V
$V_{CC}OFF$	Minimum Operating Voltage after Turn−on	NCP1605/A NCP1605B	8.0 8.6	9.0 9.0	10 9.35	V
H_{UVLO}	Difference ($V_{CC}ON$ − $V_{CC}OFF$)	NCP1605/B NCP1605A	5.0 1.2	6.0 1.5	– –	V
$V_{CC}STUP$	V_{CC} Threshold below which the Startup Current Source Turns on		5.5	7.0	8.0	V
$H_{LATCHOFF}$	Difference ($V_{CC}OFF$ − $V_{CC}STUP$)		0.6	2.0	–	V
$V_{CC}RST$	V_{CC} Level at which the Logic Resets		2.0	4.0	5.0	V
$V_{CC}INHIBIT$	Threshold which IC2 stops working & switches to IC1, I_{C2} = 1 mA					V
		NCP1605, T_J = 0°C to +125°C	–	2.1	–	
		NCP1605, T_J = −40°C to +125°C	0.3	–	2.5	
		NCP1605, T_J = −55°C to +125°C	0.3	–	2.55	
		NCP1605A	–	2.1	–	
		NCP1605B	0.3	1.8	2.2	
Internal STARTUP Current Source						
IC1_hv	(High−Voltage Current Source sunk by Pin 16, V_{CC} = 13.5 V)	NCP1605/A NCP1605B	5.0 7.0	12 12	20 17	mA
IC1_Vcc	(Startup Charge Current flowing out of the V_{CC} Pin, V_{CC} = 13.5 V)	NCP1605/A NCP1605B	5.0 6.5	12 12	20 16.5	mA
IC2	High−Voltage Current Source, V_{CC} = 0 V	NCP1605/A NCP1605B	– 0.375	0.5 0.5	1.0 0.87	mA
Device Consumption						
	Power Supply Current:					
I_{cc_op1}	Operating (@ V_{CC} = 16 V, no load, no switching)		–	2.5	5.0	mA
I_{cc_op2}	Operating (@ V_{CC} = 16 V, no load, switching)		2.0	3.5	7.0	mA
I_{cc_OFF}	Off Mode (@ V_{CC} = 16 V, Pin 2 grounded)		310	570	780	μA
$I_{cc_latchOFF}$	Latched−Off Mode (@ V_{CC} = 13.5 V and V_{Pin13} = 5 V)		310	550	750	μA

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PIN FUNCTION DESCRIPTION

Pin Number	Name	Function
1	STBY	An external signal (typically, a portion of the feedback signal of the downstream converter or a filtered portion of the SMPS drive pulses) should be applied to Pin 1. When the Pin 3 voltage goes below 300 mV, the circuit enters a burst mode operation where the bulk voltage varies between the regulation voltage and 95.5% of this level.
2	Brown−Out / Inhibition	Apply a portion of the averaged input voltage to detect brown−out conditions. If V_{Pin2} is lower than 0.5 V, the circuit stops pulsing until V_{Pin2} exceeds 1 V (0.5 V hysteresis). Ground Pin 6 to disable the part.
3	$V_{CONTROL}$ / Soft−Start	The error amplifier output is available on this Pin. The capacitor connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. Pin 3 is grounded when the circuit is off so that when it starts operation, the power increases slowly (soft−start).
4	Feedback	This pin receives a portion of the pre−converter output voltage. This information is used for the regulation and the "output low" detection (V_{OUT}L) that drastically speed up the loop response when the output voltage drops below 95.5% of the wished level.
5	Current Sense Input	This pin monitors a negative voltage proportional to the coil current. This signal is sensed to limit the maximum coil current and detect the core reset (coil demagnetization).
6	Current Sense Output	This pin sources the Pin 5 current. Place a resistor between Pin 6 and ground to build the voltage proportional to the coil current and detect the core reset. The impedance between Pin 6 and ground should not exceed 3 times that of the Pin 5 to ground. You can further apply the voltage from an auxiliary winding to improve the valley detection of the MOSFET drain source voltage.
7	Ct (Ramp)	The circuit controls the power switch on−time by comparing the Pin 7 ramp to an internal voltage ("V_{ton}") derived from the regulation block and the sensed "dcycle" (relative duration of the current cycle over the corresponding switching period). Pin 7 sources a current proportional to the squared output voltage to allow the Follower Boost operation (optional) where the PFC output voltage stabilizes at a level that varies linearly versus the ac line amplitude. This technique reduces the difference between the output and input voltages, to optimize the boost efficiency and minimize the size and cost of the PFC stage
8	Oscillator / synchronization	Connect a capacitor or apply a synchronization signal to this pin to set the switching frequency. If the coil current cycle is longer than the selected switching period, the circuit delays the next cycle until the core is reset. Hence, the PFC stage can operate in CRM in the most stressful conditions.
9	GND	Connect this pin to the pre−converter ground.
10	Drive	The high current capability of the totem pole gate drive (+0.5/−0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
11	V_{CC}	This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds 15 V (10.5 V for NCP1605A) and turns off when V_{CC} goes below 9 V (typical values). After startup, the operating range is 10 V up to 20 V.
12	PfcOK / REF5V	The Pin 12 voltage is high (5 V) when the PFC stage is in a normal, steady state situation and low otherwise. This signal serves to "inform" the downstream converter that the PFC stage is ready and that hence, it can start operation.
13	STDWN	Apply a voltage higher than 2.5 V on Pin 13 to permanently shutdown the circuit. This pin can be used to monitor the voltage across a thermistor in order to protect the application from an excessive heating and/or to detect an overvoltage condition. To resume operation, it is necessary to decrease the circuit V_{CC} below V_{CC}RST (4 V typically) by for instance, unplugging the PFC stage and replugging it after V_{CC} is discharged.
14	OVP / UVP	The circuit turns off when V_{Pin14} goes below 300 mV (UVP) and disables the drive as long as the pin voltage exceeds 2.5 V (OVP).
15	NC	Creepage distance.
16	HV	Connect Pin 16 to the bulk capacitor. The internal startup current source placed between Pin 16 and the V_{CC} terminal, charges the V_{CC} capacitor at startup.

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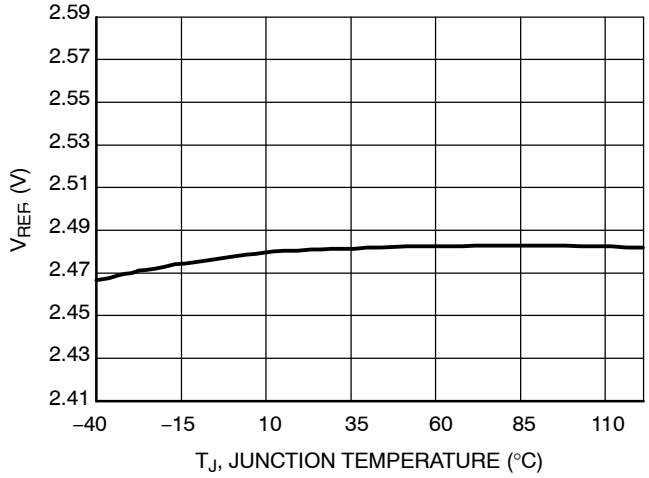


Figure 2. Reference Voltage vs. Temperature

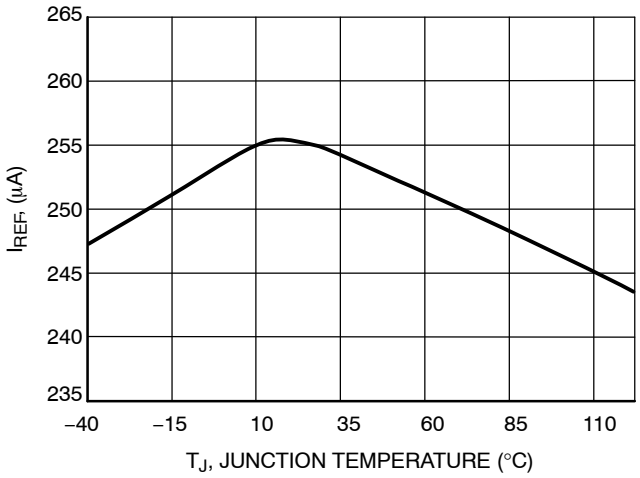


Figure 3. Reference Current vs. Temperature

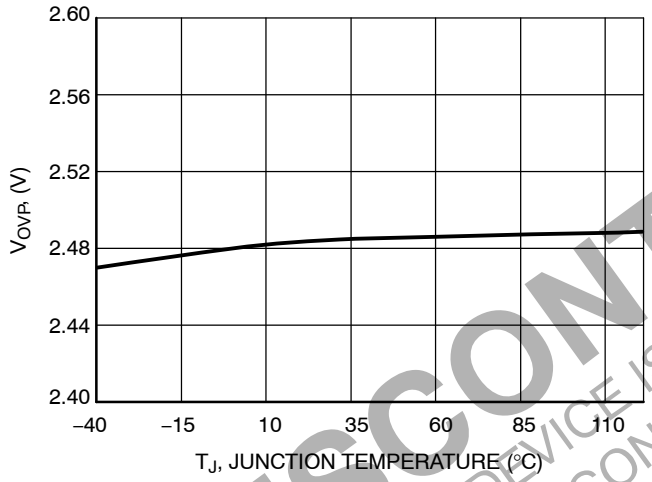


Figure 4. Overvoltage Threshold vs. Temperature

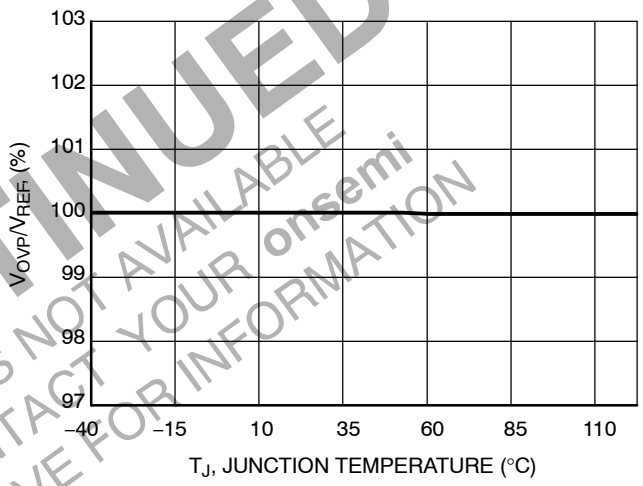


Figure 5. Ratio Overvoltage Threshold Overvoltage Reference vs. Temperature

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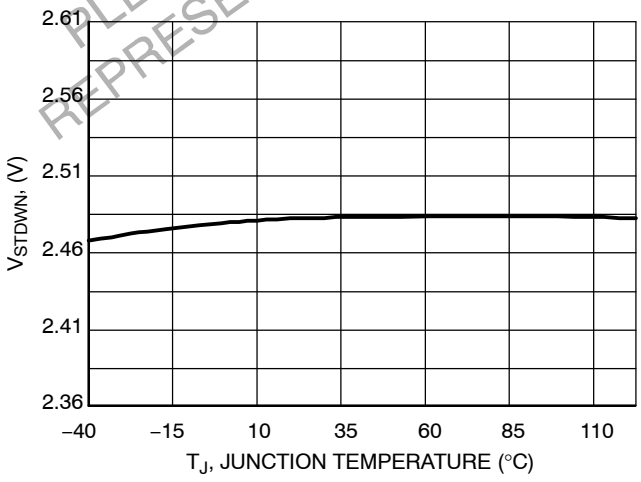


Figure 6. Shutdown Threshold vs. Temperature

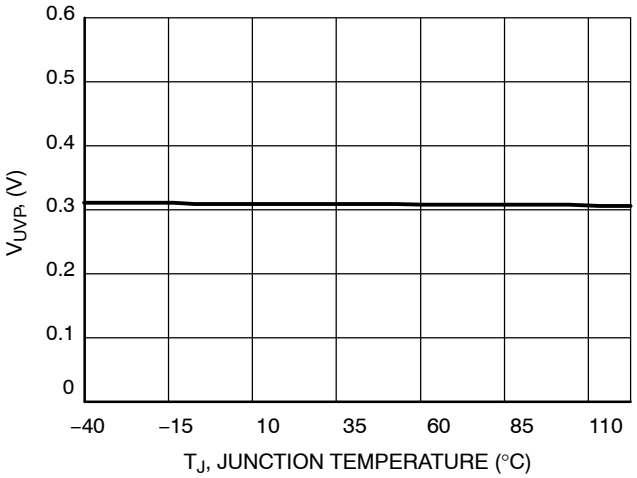


Figure 7. Undervoltage Protection Threshold vs. Temperature

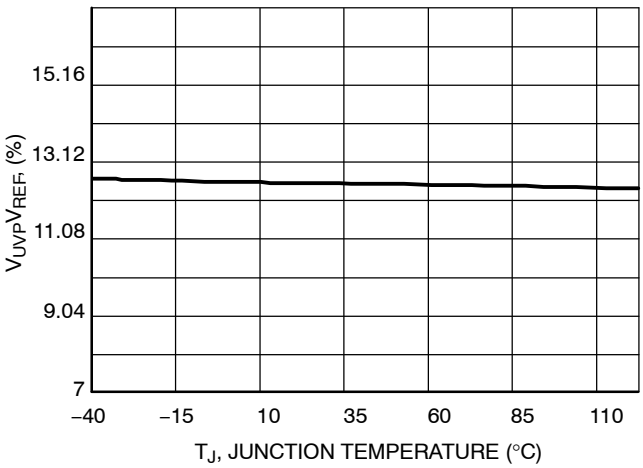


Figure 8. Ratio (V_{UVP}/V_{REF}) vs. Temperature

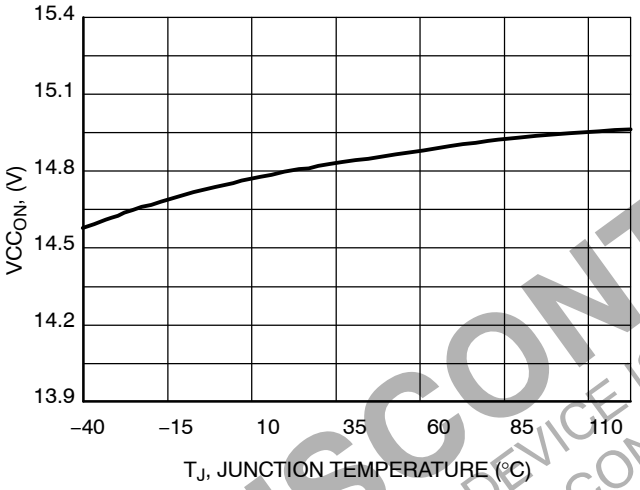


Figure 9. V_{CC} Turn on Threshold vs. Temperature (V_{CC} Raising Up) – NCP1605/B

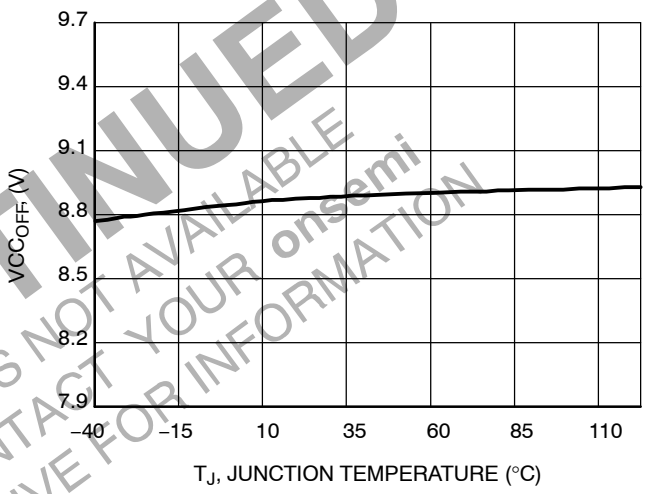


Figure 10. V_{CC} Minimum Operating Voltage After Turn On – NCP1605/B

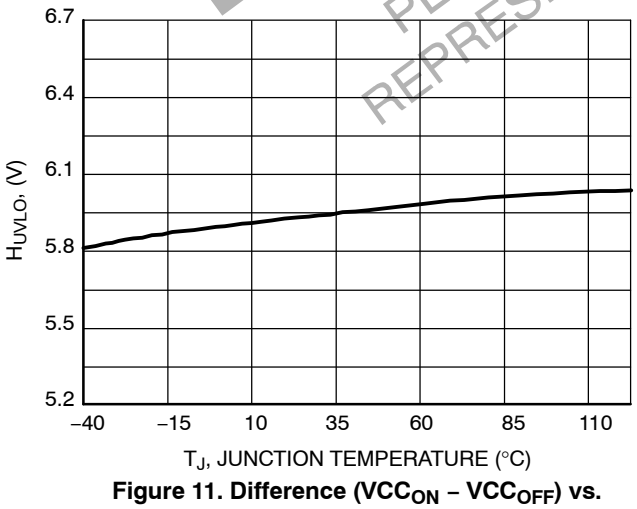


Figure 11. Difference (VCC_{ON} – VCC_{OFF}) vs. Temperature – NCP1605/B

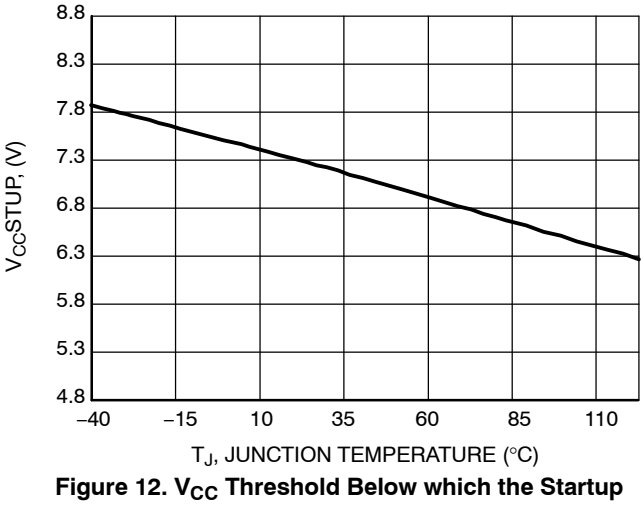


Figure 12. V_{CC} Threshold Below which the Startup Current Source Turns on vs. Temperature

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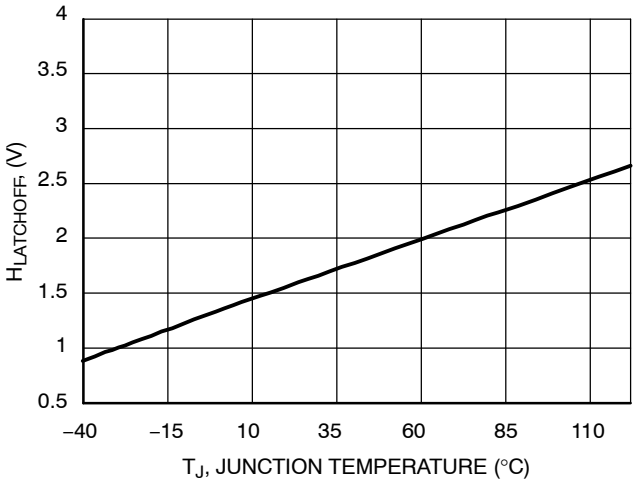


Figure 13. Difference (V_{CC}OFF−V_{CC}STUP) vs. Temperature

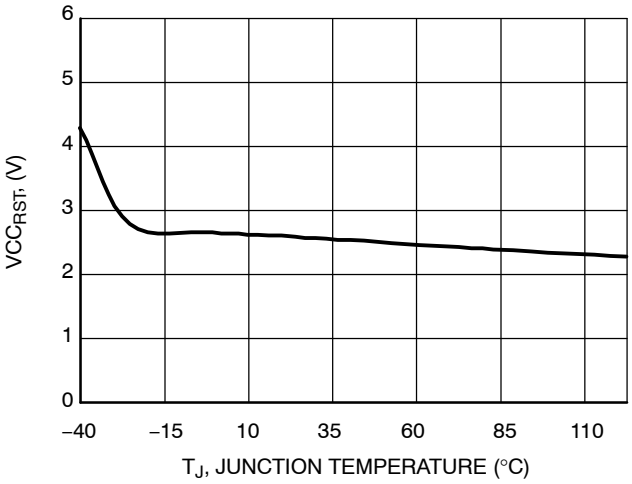


Figure 14. V_{CC} Level Below Which the Logic Resets vs. Temperature

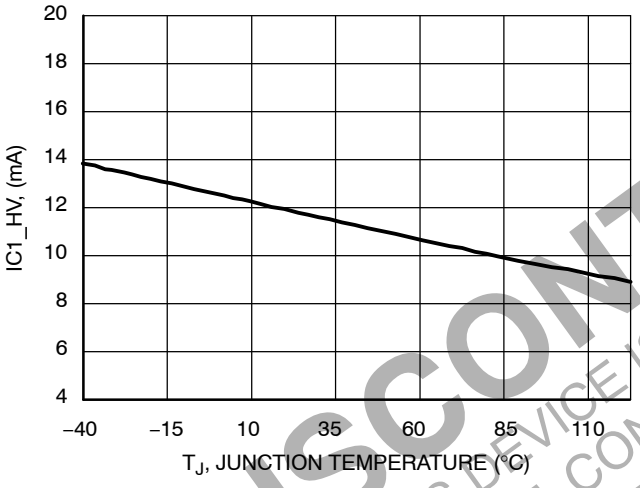


Figure 15. High−Voltage Current Source (Sunk by Pin 16) vs. Temperature (@ V_{CC} = 13.5 V)

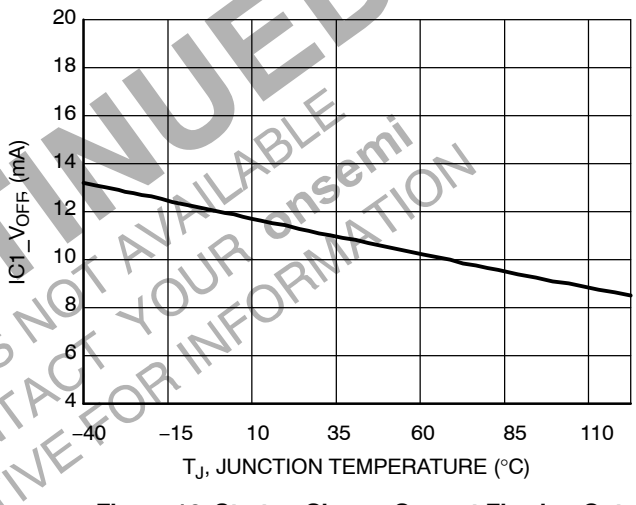


Figure 16. Startup Charge Current Flowing Out of the V_{CC} Pin vs. Temperature (@ V_{CC} = 13.5 V)

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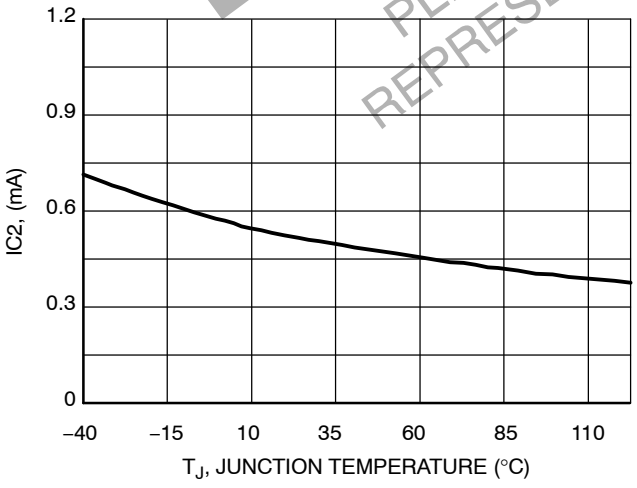


Figure 17. High−Voltage Current Source vs. Temperature (@ V_{CC} = 0 V)

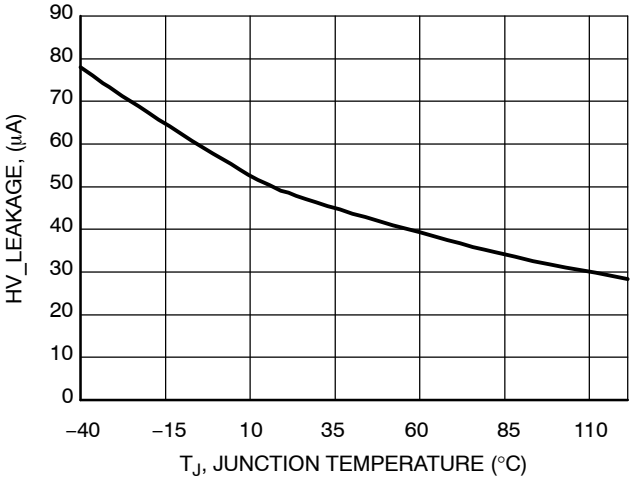


Figure 18. Pin 16 Leakage Current vs. Temperature (@ V_{PIN16} = 500 V and V_{CC} = 16 V)

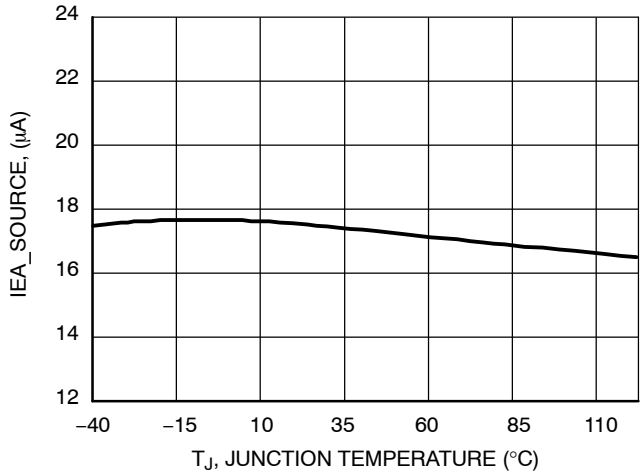


Figure 19. Source Current Capability of the Error Amplifier vs. Temperature

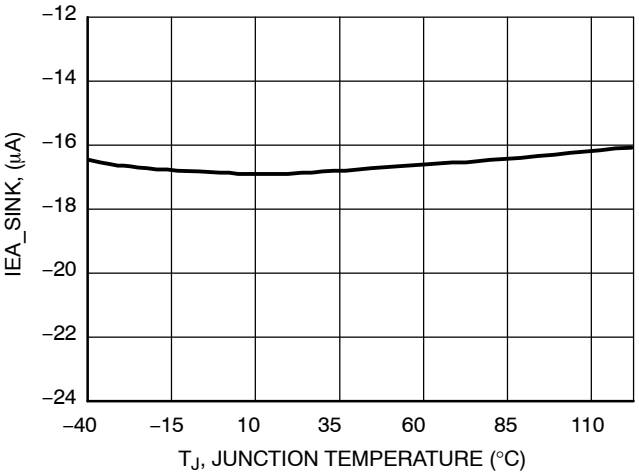


Figure 20. Sink Current Capability of the Error Amplifier vs. Temperature

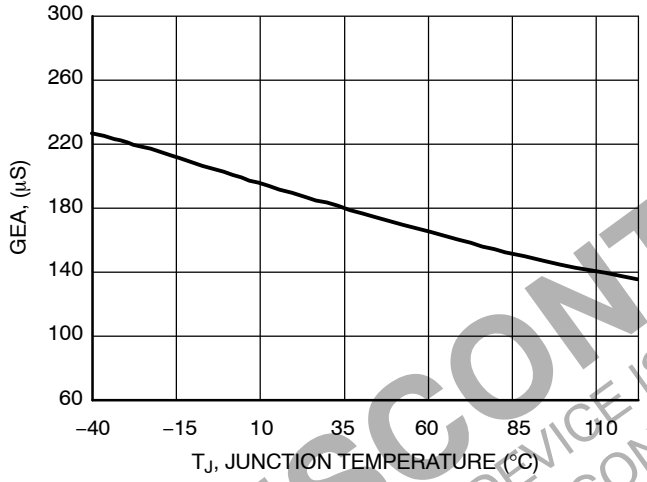


Figure 21. Error Amplifier Gain vs. Temperature

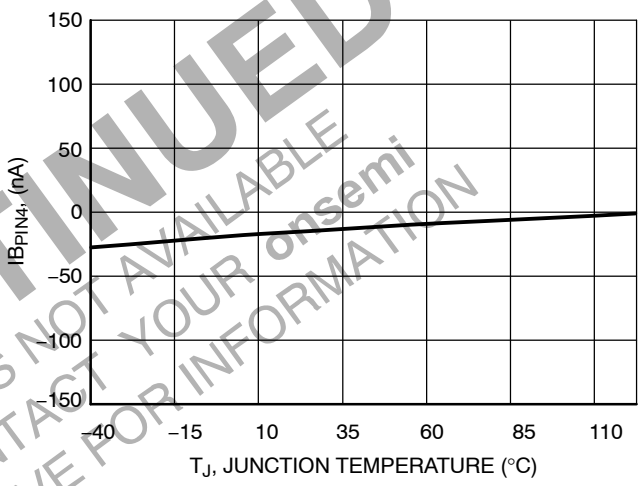


Figure 22. Feedback Pin Bias Current vs. Temperature (@ $V_{PIN4} = V_{REF}$)

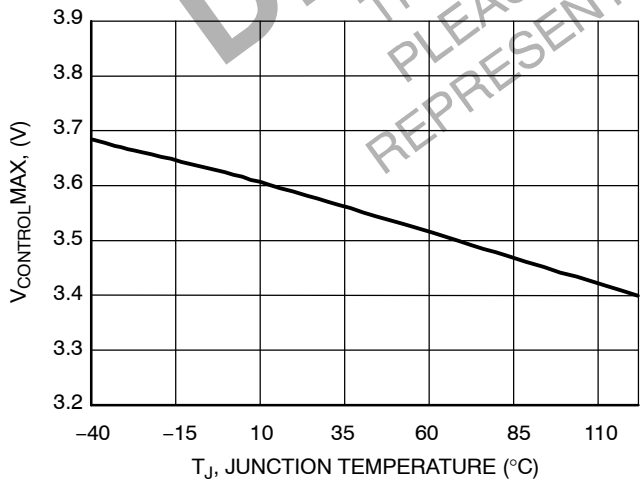


Figure 23. $V_{CONTROL}$ Maximum Voltage vs. Temperature

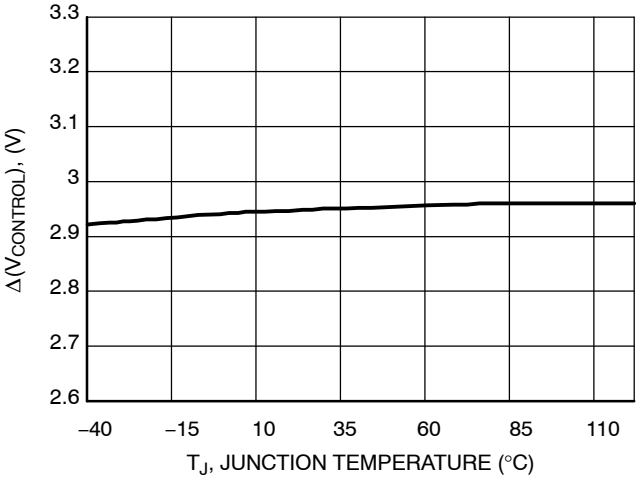


Figure 24. $V_{CONTROL}$ Maximum Swing ($\Delta V_{CONTROL}$) vs. Temperature

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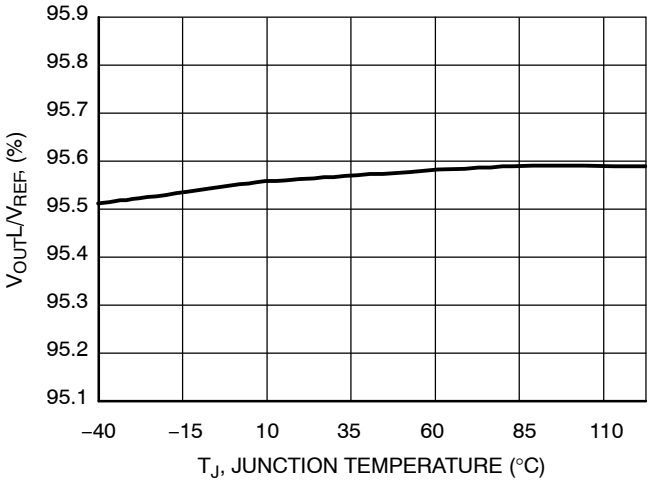


Figure 25. Ratio (V_{OUT} Low Detect Threshold) / V_{REF} vs. Temperature

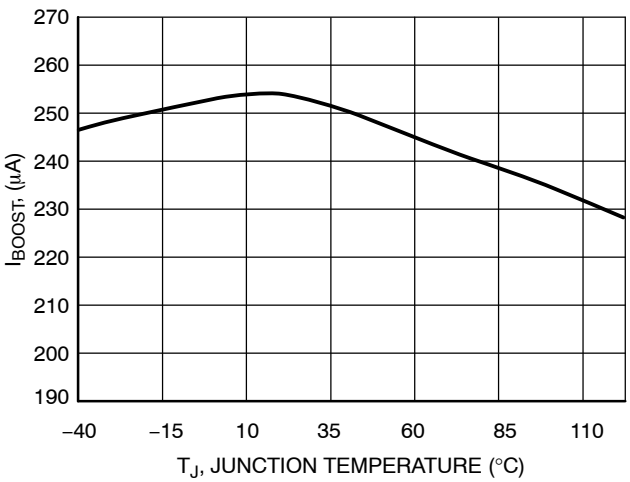


Figure 26. Pin 3 Source Current when (V_{OUT} Low Detect Threshold) is Activated vs. Temperature

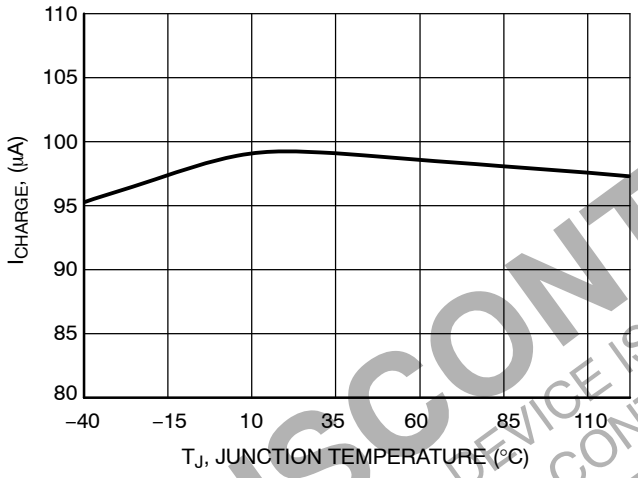


Figure 27. Oscillator Charge Current vs. Temperature

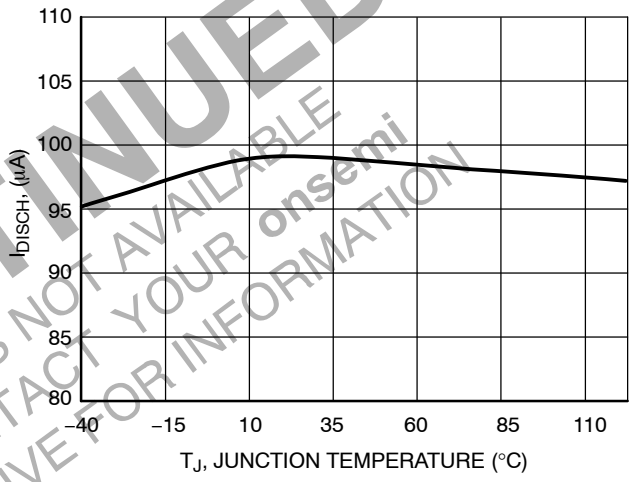


Figure 28. Oscillator Discharge Current vs. Temperature

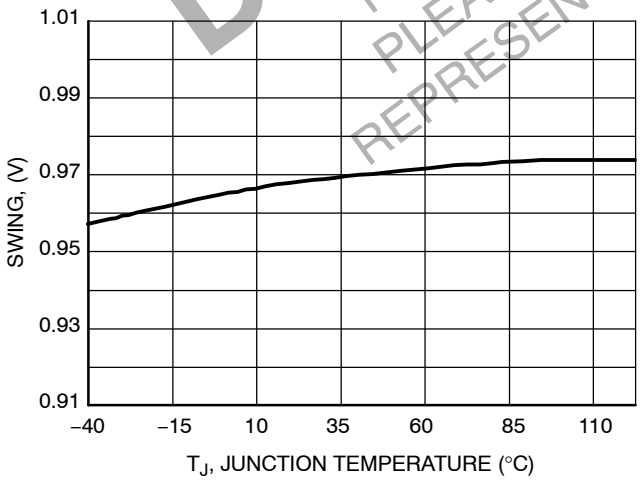


Figure 29. Oscillator Swing vs. Temperature

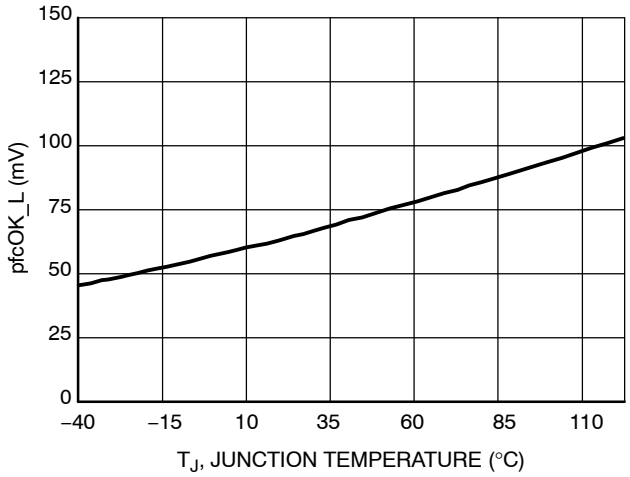


Figure 30. pfcOK Pin Low Level Voltage vs. Temperature

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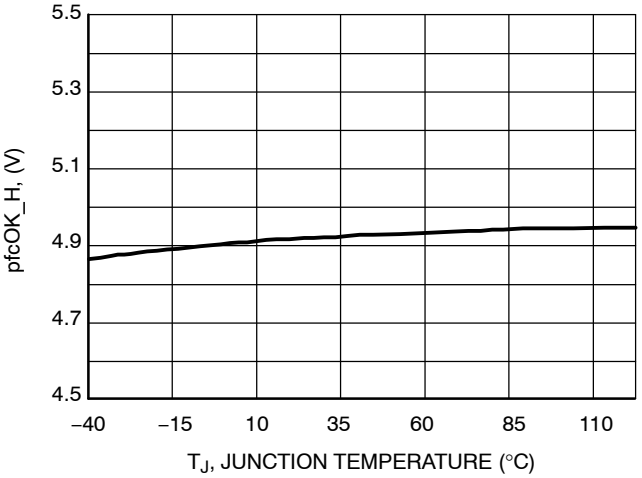


Figure 31. pfcOK Pin High Level Voltage vs. Temperature (250 μA Load)

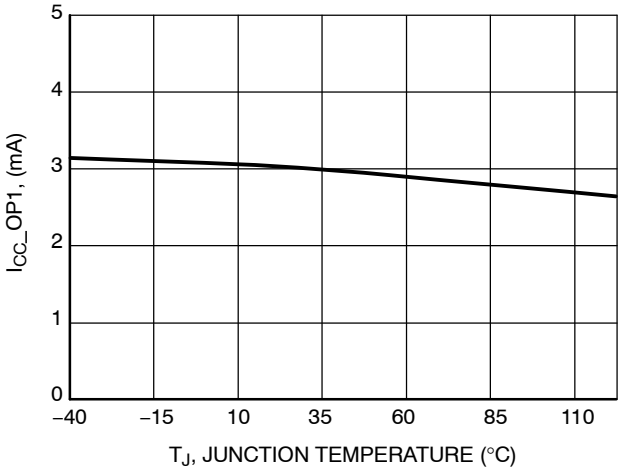


Figure 32. Operating Consumption vs. Temperature (V_{CC} = 16 V, No Load, No Switching)

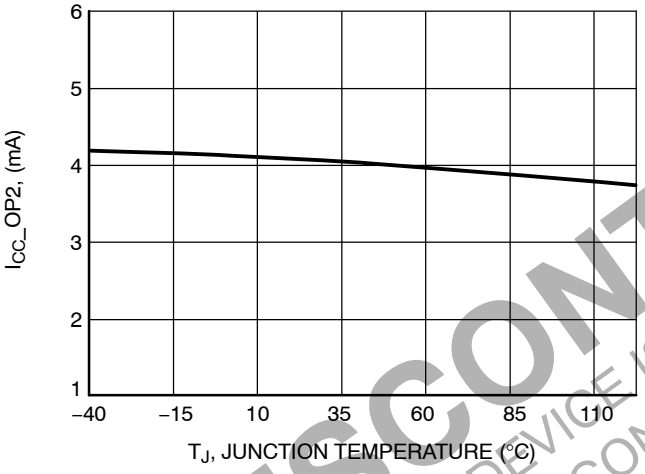


Figure 33. Operating Consumption vs. Temperature (V_{CC} = 16 V, No Load, Switching)

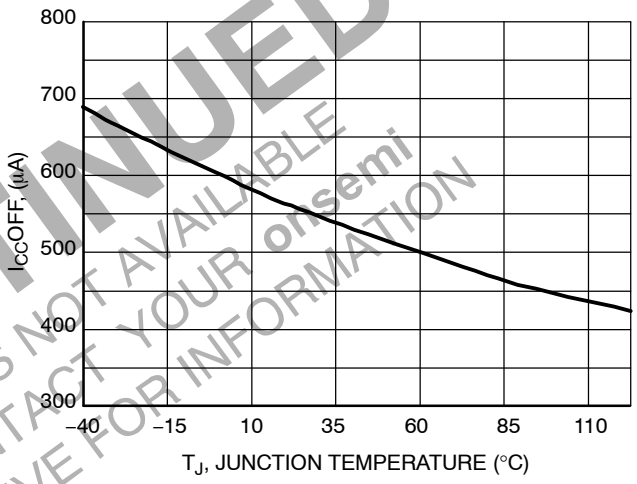


Figure 34. Off Mode Consumption vs. Temperature (V_{CC} = 16 V, Pin 2 Grounded)

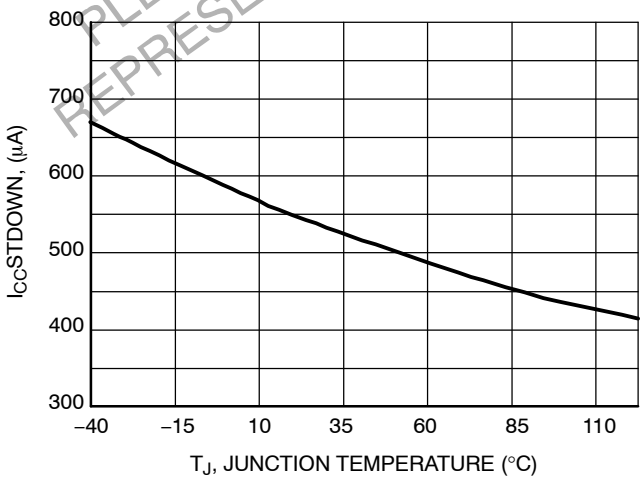


Figure 35. Shutdown Mode Consumption vs. Temperature (V_{CC} = 16 V, Pin 2 GND)

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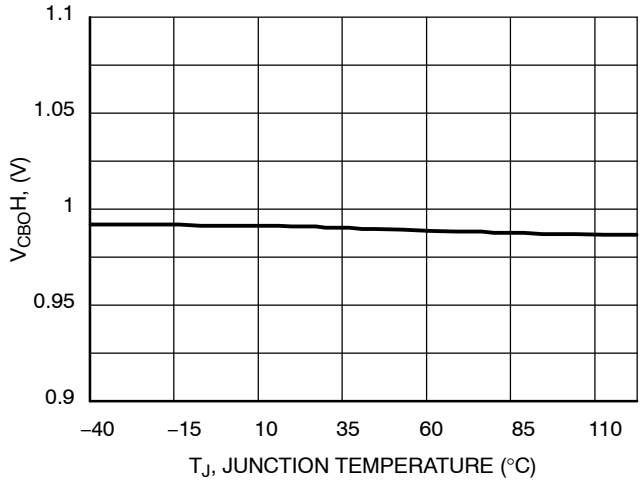


Figure 36. Brown−Out Upper Threshold vs. Temperature

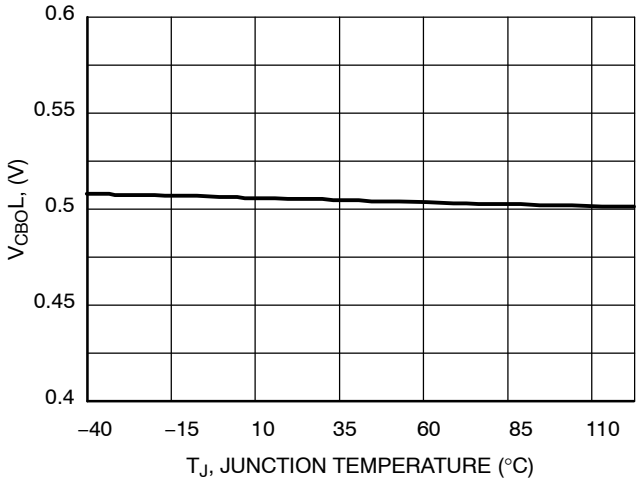


Figure 37. Brown−Out Lower Threshold vs. Temperature

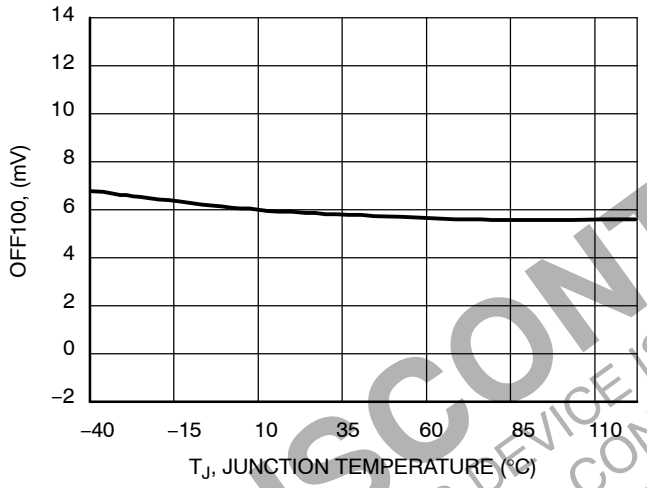


Figure 38. Current Sense Pin Voltage vs. Temperature (100 μA Being Drawn from Pin 5)

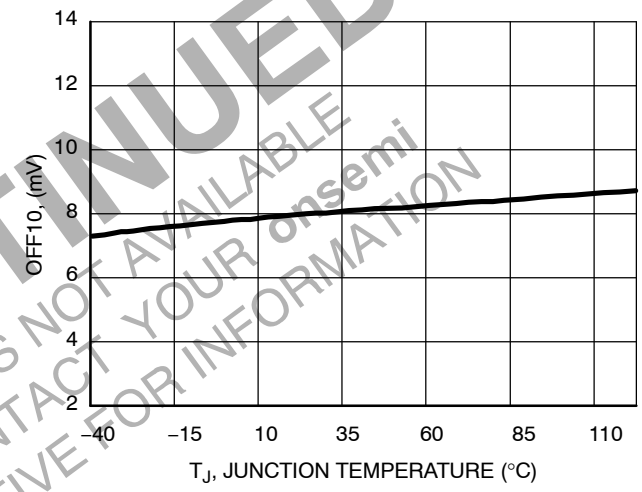


Figure 39. Current Sense Pin Voltage vs. Temperature (10 μA Being Drawn from Pin 5)

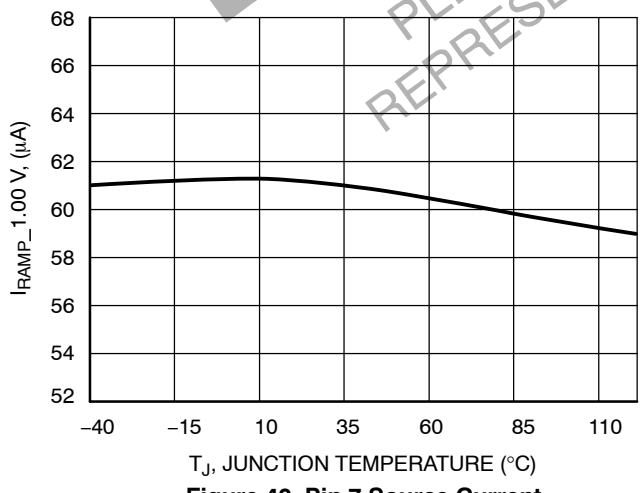


Figure 40. Pin 7 Source Current @ V_{PIN4} = 1.0 V vs. Temperature

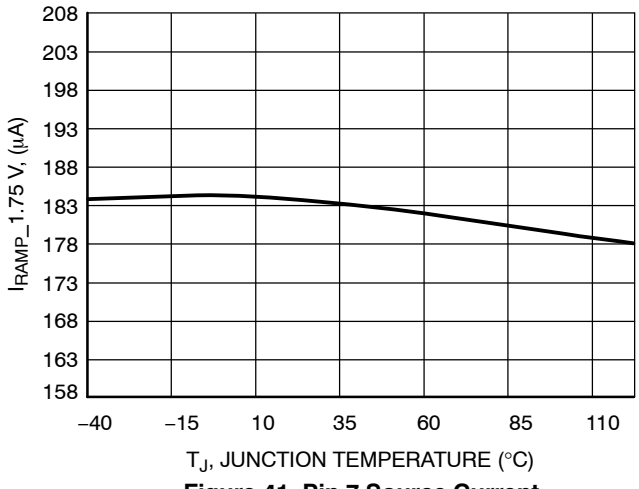


Figure 41. Pin 7 Source Current @ V_{PIN4} = 1.75 V vs. Temperature

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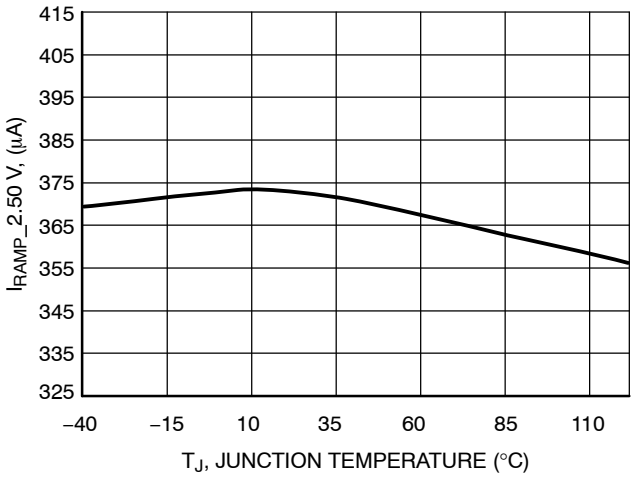


Figure 42. Pin 7 Source Current @ V_{PIN4} = 2.5 V vs. Temperature

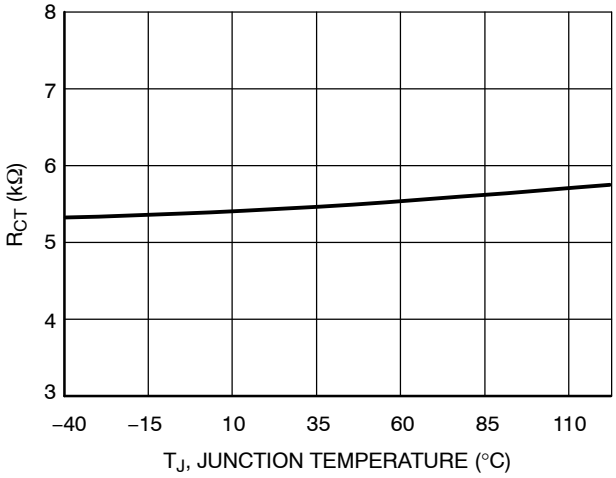


Figure 43. Ratio Pin 7 Clamp Voltage / (Pin 7 Charge Current) that is (V_{CLCRM} / I_{RAMP}) @ V_{PIN6} = 0 V and V_{PIN4} = 1.75 V

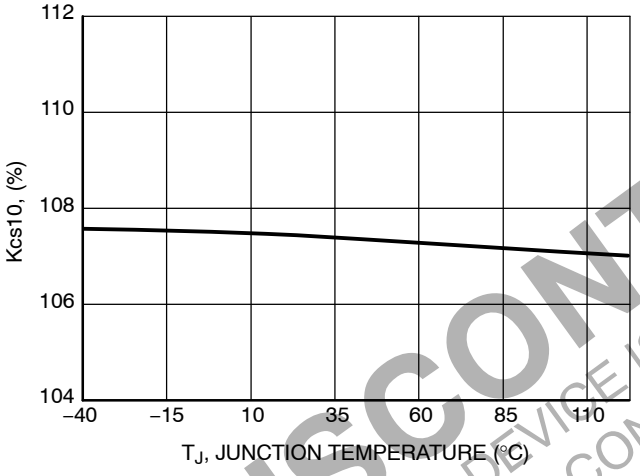


Figure 44. Ratio (I_{PIN6} / I_{PIN5}) @ I_{PIN5} = 10 μA vs. Temperature

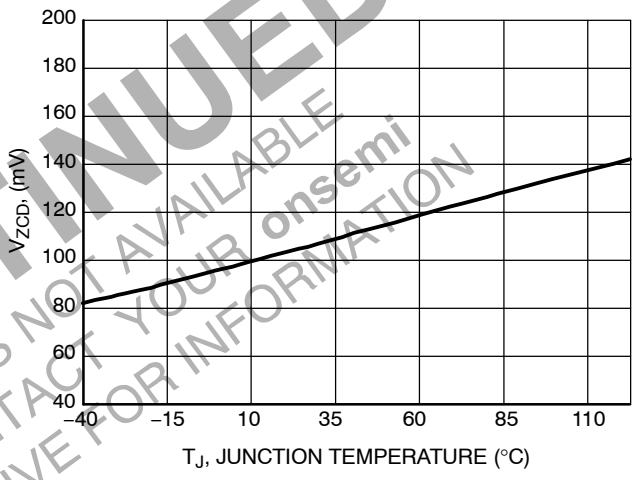


Figure 45. Pin 6 Comparator Threshold vs. Temperature

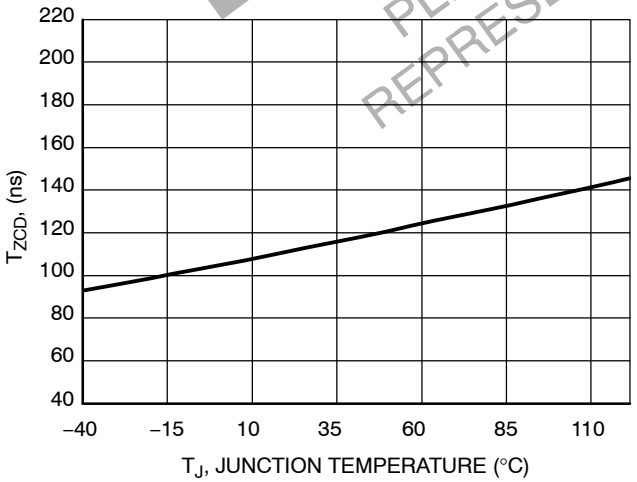


Figure 46. Delay from (ZCD Pin Low) to (DRV High) vs. Temperature

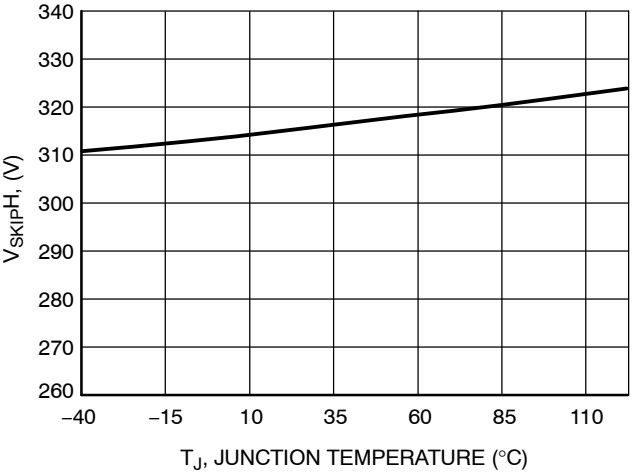


Figure 47. Skip Cycle Threshold (V_{PIN1} Falling) vs. Temperature

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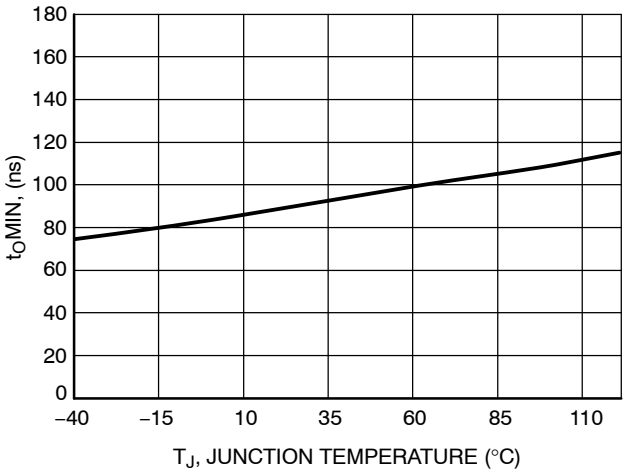


Figure 48. Minimum On−Time vs. Temperature

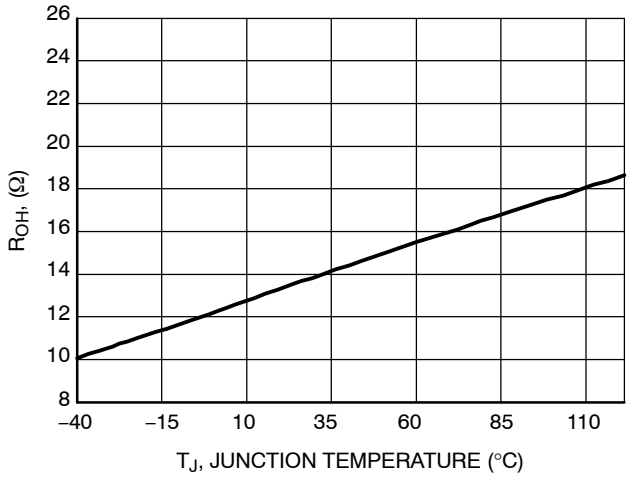


Figure 49. Gate Drive Source Resistance vs. Temperature

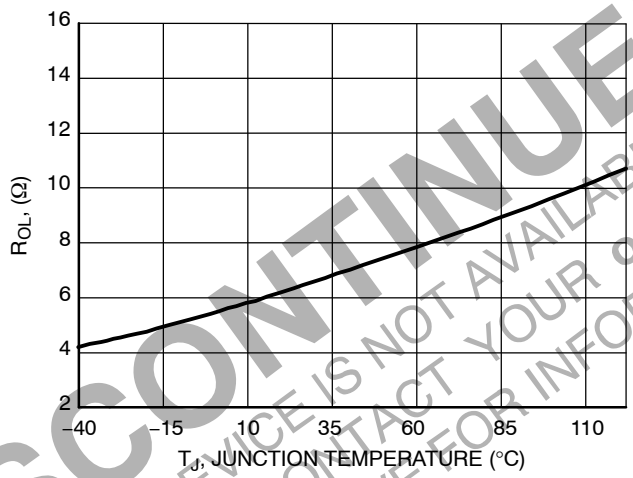
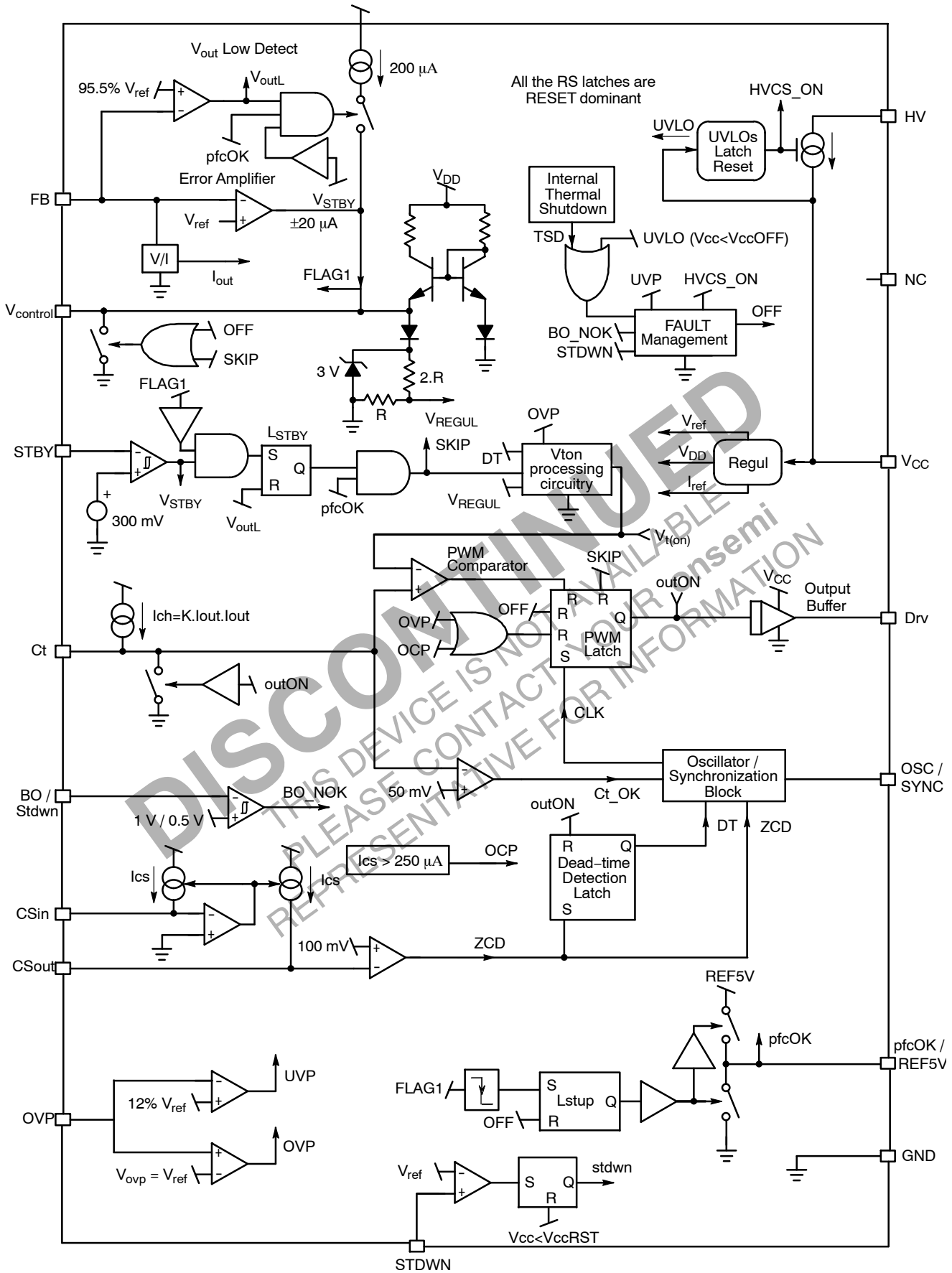


Figure 50. Gate Drive Sink Resistance vs. Temperature

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Figure 51. Block Diagram

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1605 is a PFC driver designed to operate in fixed frequency, Discontinuous Conduction Mode (DCM). In the most stressful conditions, Critical Conduction Mode (CRM) can be achieved without power factor degradation and the circuit could be viewed as a CRM controller with a frequency clamp (given by the oscillator). Finally, the NCP1605 tends to give the best of both modes without their respective drawbacks. Furthermore, the circuit incorporates protection features for a rugged operation together with some special circuitry to lower the power consumed by the PFC stage in no load conditions. More generally, the NCP1605 functions make it the ideal candidate in systems where cost−effectiveness, reliability, low standby power and high power factor are the key parameters:

- **Compactness and Flexibility:** the controller requires few external components while offering a large variety of functions. Depending on the selected coil and oscillator frequency you select, the circuit can:
  1. Mostly operate in CRM and use the oscillator as a frequency clamp.
  2. Mostly operate in fixed frequency mode and only run in CRM at high load and low line.
  3. Permanently operate in fixed frequency mode DCM.

In all cases, the circuit provides near−unity power factor.

Skip−cycle capability for low power standby: among other applications, the circuit targets power supply where the PFC stage must keep alive even in standby. A continuous flow of pulses is not compatible with no−load standby power requirements. Instead, the controller slices the switching pattern in bunch of pulses to drastically reduce the overall losses. The skip cycle operation is initiated by applying to Pin 1, a signal that goes below 300 mV in standby. Typically, this signal is drawn from the feedback of the downstream converter.

Startup Current Source and large V_{CC} range: meeting low standby power specifications represents a difficult exercise when the controller requires an external, lossy resistor connected to the bulk capacitor. The controller disables the high−voltage current source after startup which no longer hampers the consumption in no−load situations. In addition, the large V_{CC} range (10 V to 20 V after startup), highly eases the circuit biasing.

Fast Line / Load Transient Compensation: given the low bandwidth of the regulation block, the output voltage of PFC stages may exhibit excessive over and undershoots because of abrupt load or input voltage variations (e.g. at startup). If the output voltage is too far from the regulation level:

- The NCP1605 disables the drive to stop delivering power as long as the output voltage exceeds the Overvoltage Protection (OVP) level.
- The NCP1605 drastically speeds up the regulation loop when the output voltage is below 95.5% of its regulation level. This function is allowed only after the PFC stage has started up not to eliminate the soft−start effect.

PFC OK: the circuit detects when the circuit is in normal situation or if on the contrary, it is in a startup or fault condition. In the first case, Pin 12 is in high state and low otherwise. Pin 12 serves to control the downstream converter operation in response to the PFC state.

Safety Protections: the NCP1605 permanently monitors the input and output voltages, the coil current and the die temperature to protect the system from possible over−stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:

- **Maximum Current Limit and Zero Current Detection:** the circuit permanently senses the coil current and immediately turns off the power switch if it is higher than the set current limit. It also prevents any turn on of the power switch as long as some current flows through the coil, to ensure operation in DCM. This feature also protects the MOSFET from the excessive stress that could result from the large in−rush currents that occurs during the startup phases.
- **Undervoltage Protection:** the circuit turns off when it detects that the output voltage goes below 12% of the OVP level (typically). This feature protects the PFC stage from starting operation in case of too low ac line conditions or in case of a failure in the OVP monitoring network (e.g., bad connection).
- **Brown−Out Detection:** the circuit detects too low ac line conditions and stop operating in this case. This protection protects the PFC stage from the excessive stress that could damage it in such conditions.
- **Thermal Shutdown:** an internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 150°C typically. The circuit resumes operation once the temperature drops below about 100°C (50°C hysteresis).

Output Stage Totem Pole: the NCP1605 incorporates a −0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.

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NCP1605(A) Operation Modes

Like the NCP1601, the NCP1605:

- Features a current sense block that prevents the PFC stage from operating in CCM: as long as the coil current is not null, the power switch is not allowed to turn on. Hence the circuit can only operate in either Fixed Frequency DCM or CRM.
- Features the capability to exhibit near−unity power factor while operating in any type of Discontinuous Conduction Mode operation: DCM or CRM.
- Auto adapts: if there is some current flowing through the coil when the clock occurs to initiate a new current cycle, the PFC stage enters CRM. On the other hand, if the clock occurs during dead−times, one obtains a fixed frequency operation DCM. Thanks to its special oscillator/synchronization arrangement, the circuit automatically enters the appropriate mode CRM or DCM. It is worth noting that jumps between the CRM and modes cause absolutely no degradation: the input current keeps being properly shaped and there is no discontinuity in the power transfer.

Given the dead−time presence, DCM needs a higher peak inductor current compared to CRM for the same delivered power. Hence, the coil is generally designed to have CRM at the most stressful conditions while DCM limits the switching frequency at lower load. The circuit can also transition within an ac line cycle so that:

- CRM reduces the current stress around the sinusoid top.
- DCM limits the frequency around the line zero crossing.

This capability offers the best of each mode without the drawbacks. The way the circuit modulates the MOSFET on−time allows this facility.

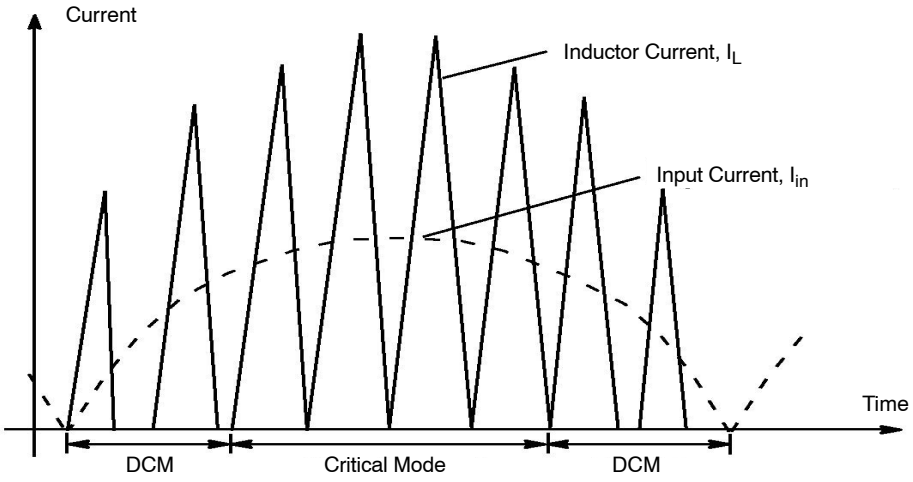


Figure 52. DCM and CRM Operation Within a Sinusoid Cycle

The NCP1605(A) can jump from DCM to CRM within a sinusoid cycle (and vice versa) without any discontinuity in the current shaping or the power transfer.

NCP1605 On−time Modulation

Let's study the ac line current absorbed by the PFC boost. The initial inductor current of each switching cycle is always zero. The coil current ramps up when the MOSFET is *on*. The slope is (V_{IN}/L) where L is the coil inductance. At the end of the on−time (t1), the coil demagnetization phase starts. The coil current ramps down until this sequence ends when it reaches zero. The duration of this phase is (t2). The system enters then the dead−time (t3) that lasts until the next clock is generated.

One can show (refer to NCP1601 data sheet) that the ac line current is given by:

$$I_{in} = V_{in}\left[\frac{t_1\,(t_1 + t_2)}{2\,T\,L}\right] \qquad \text{(eq. 1)}$$

Where T = (t1 + t2 + t3) is the switching period and V_{IN} is the ac line rectified voltage.

To the light of this equation, we immediately note that I_{IN} is proportional to V_{IN} if [t1(t1 + t2)/T] is a constant.

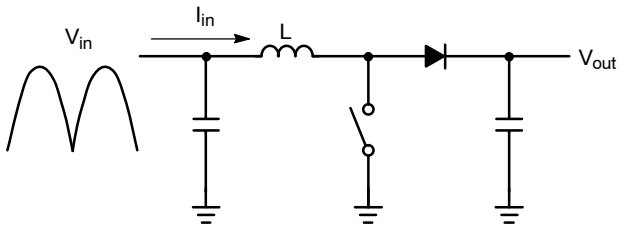


Figure 53. PFC Boost Converter

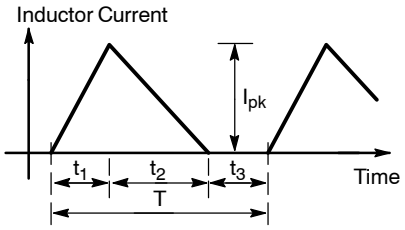


Figure 54. Inductor Current in DCM

The NCP1605 operates in voltage mode. As portrayed by Figure 55, the MOSFET on time t_1 is controlled by the signal V_{ton} generated by the regulation block and the Pin 4 ramp as follows:

$$t_1 = \frac{C_{pin7} \cdot V_{TON}}{I_{pin7}} \qquad \text{(eq. 2)}$$

The charge current that is sourced by Pin 7 [I_{pin7} = 60 μA/V^2 * (V_{Pin4})^2] is constant at a given input voltage (V_{Pin4} is proportional to the output voltage). C_{pin7} that is the capacitor connected between Pin 7 and ground is also a constant. Hence, the power factor correction is achieved when the V_{TON} ($t_1 + t_2$)/T term is constant.

The output of the regulation block ($V_{CONTROL}$) is linearly changed into a signal (V_{REGUL}) varying between 0 and 1 V. (V_{REGUL}) is the voltage that is injected into the PWM section to modulate the MOSFET duty−cycle. However, like the NCP1601, the NCP1605 inserts some circuitry that processes (V_{REGUL}) to form the signal (V_{TON}) that is used in the PWM section instead of (V_{REGUL}) (see Figure 56). (V_{TON}) is modulated in response to the dead−time sensed during the precedent current cycles, that is, for a proper shaping of the ac line current (refer to NCP1601 data sheet). This modulation leads to:

$$V_{TON} = \frac{T \cdot V_{REGUL}}{t_1 + t_2} \text{ or : } V_{TON} \cdot \frac{t_1 + t_2}{T} = V_{REGUL} \qquad \text{(eq. 3)}$$

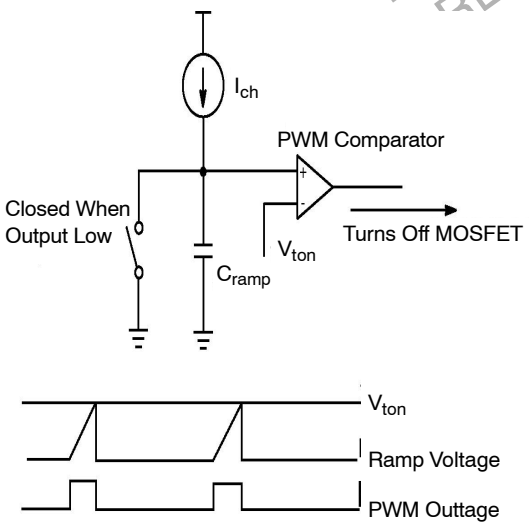


Figure 55. PWM Circuit and Timing Diagram

Given the regulation low bandwidth of the PFC systems, ($V_{CONTROL}$) and then (V_{REGUL}) are slow varying signals. Hence, the (V_{TON} * (t_1 + t_2)/T) term is substantially constant. Provided that in addition, (t1) is proportional to (V_{TON}), equation (1) leads to: (I_{in} = k * V_{in}), where k is a constant. More exactly:

$$I_{in} = k \cdot V_{in}$$
$$\text{where : } k = \text{constant} = \left[\frac{C_{pin7} \cdot V_{REGUL}}{120\,\mu \cdot L \cdot (V_{pin2})^2}\right] \qquad \text{(eq. 4)}$$

The input current is then proportional to the input voltage. Hence, the ac line current is properly shaped.

One can note that this analysis is also valid in the CRM case. This condition is just a particular case of this functioning where (t_3 = 0), which leads to (t_1 + t_2 = T) and (V_{TON} = V_{REGUL}). That is why the NCP1605 automatically adapts to the conditions and jumps from DCM and CRM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

Remark: Like in the NCP1601, the "V_{TON} processing circuit" is "informed" when there is an OVP condition, not to over−dimension V_{TON} in that conditions. Otherwise, an OVP sequence would be viewed as a dead−time phase by the circuit and V_{TON} would inappropriately increase to compensate it.

Similarly, the "V_{TON} processing circuit" is inhibited for a skip sequence not to over−dimension "V_{TON}" in this case (refer to Figure 56).

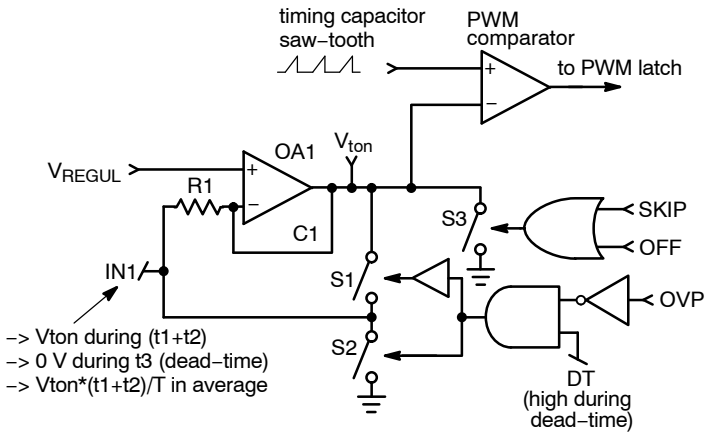


Figure 56. V_{TON} Processing Circuit

The integrator OA1 amplifies the error between V_{REGUL} and IN1 so that in average, (V_{TON}*(t1+t2)/T) equates V_{REGUL}.

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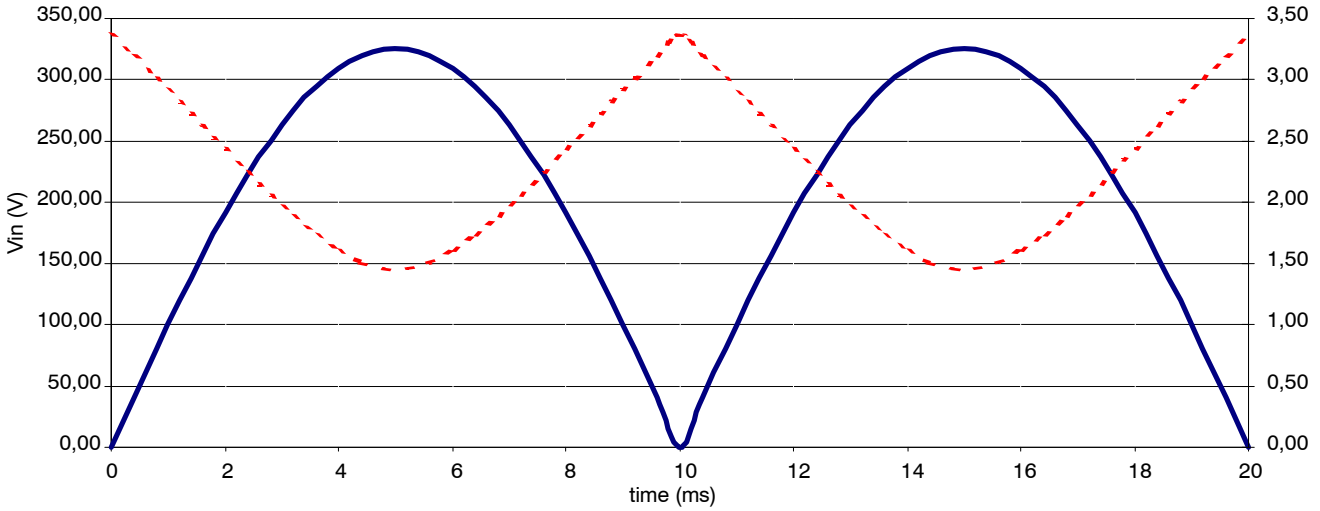


Figure 57. Input Voltage and On−time vs Time (example with F_{SW} = 100 kHz, Pin =150 W, V_{AC} = 230 V, L = 200 μH)

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Regulation Block and Low Output Voltage Detection

A transconductance error amplifier with access to the inverting input and output is provided. It features a typical transconductance gain of 200 μS and a maximum capability of ±20 μA. The output voltage of the PFC stage is typically scaled down by a resistors divider and monitored by the inverting input (feedback pin − Pin 4). The bias current is minimized (less than 500 nA) to allow the use of a high impedance feedback network. The output of the error amplifier is pinned out for external loop compensation (Pin 3). Typically a capacitor in the range of 100 nF, is applied between Pin 3 and ground, to set the regulation bandwidth below 20 Hz, as need in PFC applications.

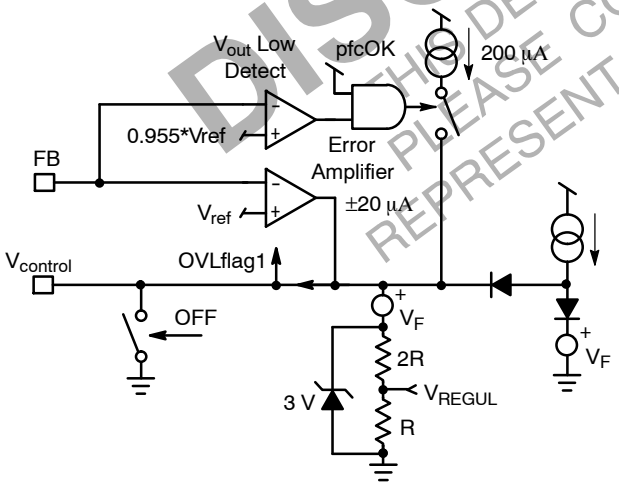


Figure 58. Regulation Block

The swing of the error amplifier output is limited within an accurate range:

- It is forced above a voltage drop (V_F) by some circuitry.
- It is clamped not to exceed 3.0 V + the same V_F voltage drop.

Hence, V_{Pin3} features a 3 V voltage swing. V_{Pin3} is then offset down by (V_F) and divided by three before it connects to the "V_{TON} processing block" and the PWM section. Finally, the output of the regulation is a signal ("V_{REGUL}" of the block diagram) that varies between 0 and 1 V.

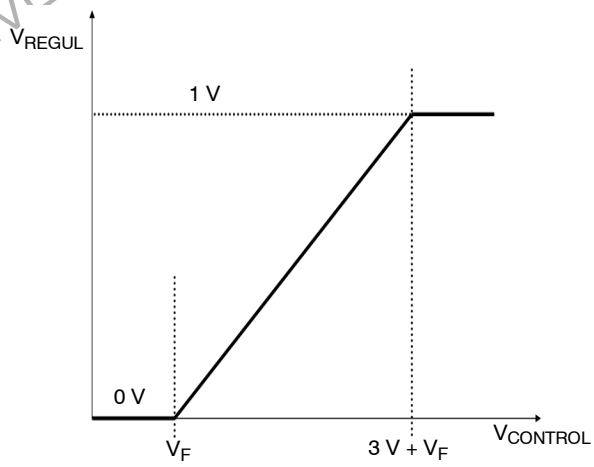


Figure 59. Correspondence between $V_{CONTROL}$ and V_{REGUL}

Provided the low bandwidth of the regulation loop, sharp variations of the load, may result in excessive over and undershoots. Overshoots are limited by the Overvoltage Protection (see OVP section). To contain the undershoots, an internal comparator monitors the feedback (V_{Pin4}) and when V_{Pin4} is lower than 95.5% of its nominal value, it connects a 200 μA current source to speed−up the charge of the compensation capacitor (Cpin3). Finally, it is like if the comparator multiplied the error amplifier gain by 10.

One must note that this circuitry for undershoots limitation, is not enabled during the startup sequence of the PFC stage but only once the converter has stabilized (that is when the

"pfcOK" signal of the block diagram, is high). This is because, at the beginning of operation, the Pin 3 capacitor must charge slowly and gradually for a soft–startup.

Remark: As shown in block diagram, the circuitry for undershoots limitation is disabled as long as Pin 3 detects standby conditions (V_{Pin3} < 300 mV). This is to suppress the risk of audible noise in standby thanks to the soft–start that softens the bursts.

On–Time Control for Maximum Power Adjustment

As aforementioned, the NCP1605 processes the error amplifier output voltage to form a signal (V_{TON}) that is used by the PWM section to control the on–time. (V_{TON}) compensates the relative weight of the dead–time sequences measured during the precedent current cycles. During the conduction time of the MOSFET, Pin 7 sources a current that is proportional to the square of the voltage applied to Pin 4 (feedback pin). Practically, as Pin 4 receives a portion of the output voltage (V_{OUT}), I_{Pin7} is proportional to the square of V_{OUT}.

The MOSFET turns off when the Pin 7 voltage exceeds V_{TON}. Hence, the MOSFET on–time (t1) is given by:

$$t_1 = \frac{C_{pin7}\, V_{TON}}{k\, V_{OUT}^2} \quad \text{where k is a constant.}$$

The coil current averaged over one switching period is:

$$< I_{COIL} >_T = I_{IN}(t) = \frac{V_{IN}\, t_1\, (t_1 + t_2)}{2\, L\, T}$$

Where $I_{IN}(t)$ and $V_{IN}(t)$ are the instantaneous input current and voltage, respectively, t_2 is the core reset time and T is the switching period. Hence, the instantaneous input power is given by the following equation:

$$P_{IN}(t) = V_{IN}(t) I_{IN}(t) = \frac{C_{pin7}\, V_{IN}^2}{2\, L\, k\, V_{OUT}^2} \cdot \frac{V_{TON}\, (t_1 + t_2)}{T}$$

As aforementioned, we have: $V_{TON}\, (t_1 + t_2)/T = V_{REGUL}$ where V_{REGUL} is the signal outputted by the regulation block. Hence, the average input power is:

$$< P_{IN} > = \frac{C_{pin7}\, V_{ac}^2}{2\, L\, k\, V_{OUT}^2}\, V_{REGUL}$$

The maximum value of V_{REGUL} being 1 V, the maximum power that can be delivered is:

$$< P_{IN} >_{MAX} = \frac{C_{pin7}\, V_{ac}^2}{2\, L\, k\, V_{OUT}^2}\, 1\ V$$

To the light of the last equations, one can note that the PFC power capability is inversely proportional to the square of the output voltage. One sees that if the power demand is too high to keep the regulation, (V_{REGUL}=1V) and the power delivery depends on the output voltage level that stabilizes to the following value:

$$V_{OUT} = \sqrt{\frac{C_{pin7}\, 1\ V}{2\, L\, k\, \eta\, P_{OUT}}}\, V_{ac}$$

Where:

- P_{OUT} is the output power.
- And η is the efficiency.

Hence, one obtains the Follower Boost characteristics. The "Follower Boost" is an operation mode where the pre–converter output voltage stabilizes at a level that varies linearly versus the ac line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage (refer to the MC33260 data sheet for more information, at:
http://www.onsemi.com/pub/Collateral/MC33260–D.PDF).

Remark: the timing capacitor applied to Pin 7 is discharged and maintained grounded when the drive is low. Furthermore, the circuit compares the Pin 7 voltage to an internal reference 50 mV and prevents the PWM latch from being set as long as V_{Pin7} is higher than this low threshold. This is to guarantee that the timing capacitor is properly discharged before starting a new cycle.

Current Sense and Zero Current Detection

The NCP1605 is designed to monitor a negative voltage proportional to the coil current. Practically, a current sense resistor (R_{CS}) is inserted in the return path to generate a negative voltage proportional to the coil current (V_{CS}). The circuit uses V_{CS} for two functions: the limitation of the maximum coil current and the detection of the core reset (coil demagnetization). To do so, the circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage null (refer to Figure 60). By inserting a resistor R_{OCP} between the CS pin and R_{CS}, we adjust the CS pin current as follows:

$$-\,[R_{CS}\, I_{COIL}] + [R_{OCP}\, I_{pin5}] = V_{pin5} \approx 0$$

Which leads to:

$$I_{pin5} = \frac{R_{CS}}{R_{OCP}}\, I_{COIL}$$

In other words, the Pin 5 current is proportional to the coil current.

I_{Pin5} is utilized as follows:

- If I_{Pin5} exceeds 250 μA, an overcurrent is detected and the PWM latch is reset. Hence, the maximum coil current is:

$$(I_{COIL})_{max} = \frac{R_{OCP}}{R_{CS}}\, 250\ \mu A$$

  The propagation delay (Ipin5 higher than 250 μA) to (drive output low) is in the range of 100 ns, typically.
- The Pin 5 current is internally copied and sourced by Pin 6. Place a resistor (R_{Pin6}) between Pin 6 and ground to build a voltage proportional to the coil current. The circuit detects the core reset when V_{Pin6} drops below 100 mV, typically. The Pin 6 voltage equating:

$$V_{pin6} = \frac{R_{pin6} \cdot R_{cs}}{R_{cs}} \cdot I_{COIL}\ ,$$

  the coil current threshold for zero current detection is:

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$$(I_{COIL})_{zcd} = \frac{R_{OCP}}{R_{pin6} \cdot R_{CS}}\ 100\ mV = \frac{100\ mV}{R_{pin6} \cdot 250\ \mu A} \cdot (I_{COIL})_{MAX} = \frac{400\ \Omega}{R_{pin6}} \cdot (I_{COIL})_{MAX}$$

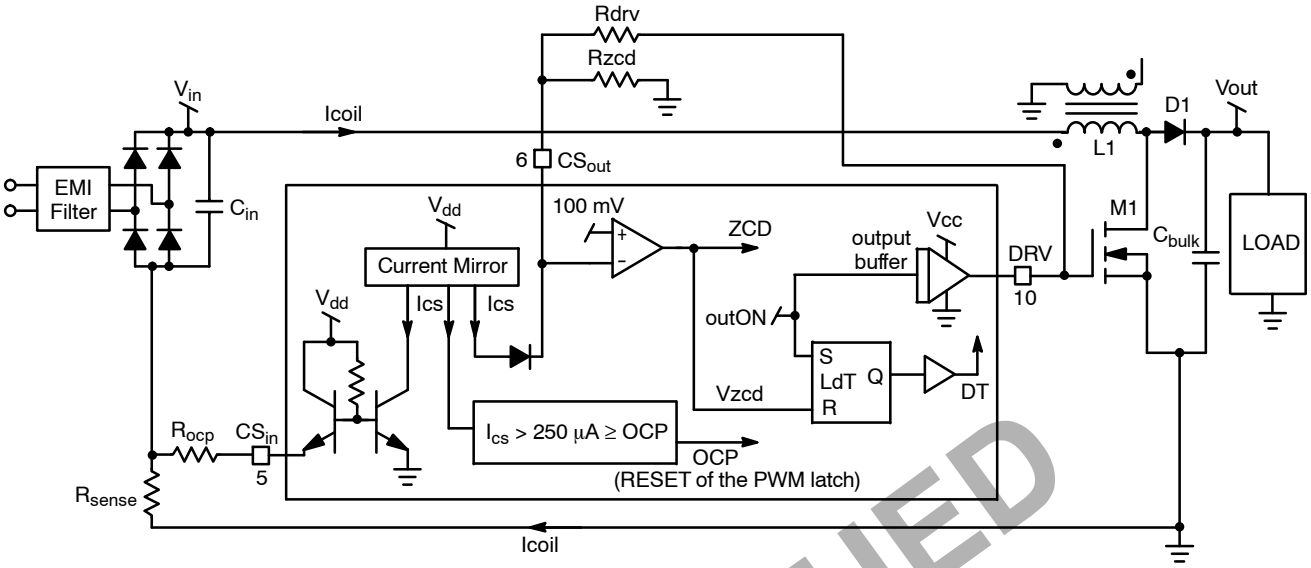


Figure 60. Current Sense Block

The CS block performs the overcurrent protection and the zero current detection.

The propagation delay (V_{Pin6} lower than 100 mV) to (drive output high) is in the range of 300 ns, typically.

The Zero Current Detection:

- Is used to detect the dead−time sequences (“DT” high) and hence, to process (V_{TON}) from the error amplifier output ($V_{CONTROL}$). In other words, this is an input of the on−time modulation block.
- Prevents the MOSFET from turning on as long as the “DT” and “ZCD” signals are low. This is the case as long as some current flows through the coil. This delaying action on the output stage tends to make the MOSFET turn on at the valley. To further optimize the valley switching, one can apply the voltage of an auxiliary winding to Pin 6 (CS_{OUT}). The voltage is compared to an internal 100 mV reference, so that ZCD turns high only if (V_{Pin6} < 100 mV).

Remarks:

- A resistor can be placed between Pin 6 and ground to increase the ZCD precision.
- It is worth highlighting that the circuit permanently senses the coil current and that it prevents any turn on of the power switch as long as the core is not reset. This feature protects the MOSFET from the possible excessive stress it could suffer from, if it was allowed to turn on while a huge current flows through the coil. In particular, this scheme effectively protects the PFC stage during the startup phase when huge in−rush currents charge the output capacitor.
- In addition this detection method does not require any auxiliary winding. A simple coil can then be used in the PFC stage.

It is recommended to:

1. Keep R_{OCP} equal to or lower than 5 kΩ
2. Choose R_{ZCD} as high as possible but not bigger than (3 x R_{OCP}). This is to avoid that the Pin 6 leakage prevents a proper zero current detection. For instance, if R_{OCP} is 2.2 kΩ, R_{ZCD} should not exceed 6.6 kΩ.

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3. Place a resistor R_{DRV} between the drive pin and Pin 6 to ease the circuit detection by creating some over−riding at the turn on instant. R_{DRV} should be selected in the range of 3 times R_{ZCD}. For instance, if R_{ZCD} is 6.2 kΩ, a 22 kΩ resistor can be used for R_{DRV}.

Overvoltage Protection

While PFC circuits often use one single pin for both the Overvoltage Protection (OVP) and the feedback, the NCP1605 dedicates one specific pin for the undervoltage and overvoltage protections. The NCP1605 configuration allows the implementation of two separate feedback networks (see Figure 62):

– One for regulation applied to Pin 4.
– Another one for the OVP function.

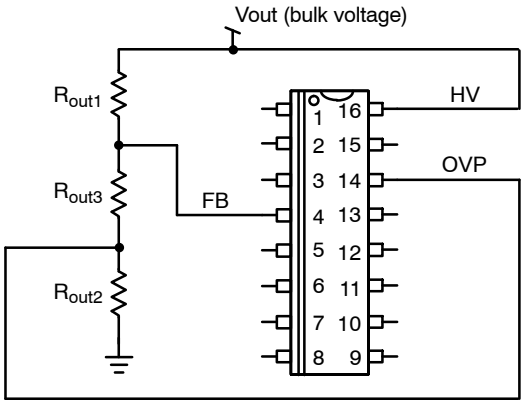


Figure 61. Configuration with One Feedback Network for Both OVP and Regulation

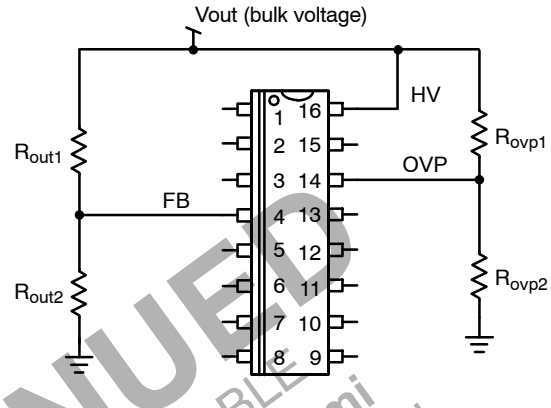


Figure 62. Configuration with Two Separate Feedback Networks

The double feedback configuration offers some up−graded safety level as it protects the PFC stage even if there is a failure of one of the two feedback arrangements.

However, if wished, one single feedback arrangement is possible as portrayed by Figure 61. The regulation and OVP blocks having the same reference voltage, the resistance ratio Rout2 over Rout3 adjusts the OVP threshold. More specifically,

The bulk regulation voltage is:

$$V_{out} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2} + R_{out3}} \cdot V_{ref}$$

The OVP level is:

$$V_{ovp} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2}} \cdot V_{ref}$$

The ratio OVP level over regulation level is:

$$\frac{V_{ovp}}{V_{out}} = 1 + \frac{R_{out3}}{R_{out2}}$$

For instance, (V_{OVP} = 105% * V_{out}) leads to the following constraint: (R_{out3} = 5% * R_{out2}).

As soon and as long as the circuit detects that the output voltage exceeds the OVP level, the power switch is turned off to stop the power delivery.

Remark: Like in the NCP1601, the "V_{TON} processing circuit" is "informed" when there is an OVP condition, not to over−dimension V_{TON} in that conditions. Otherwise, an OVP sequence would be viewed as a dead−time phase by the circuit and V_{TON} would inappropriately increase to compensate it (refer to Figure 56).

PfcOK / REF5V Signal

The NCP1605 can communicate with the downstream converter. The signal "pfcOK/REF5V is high (5 V) when the PFC stage is in normal operation (its output voltage is stabilized at the nominal level) and low otherwise.

More specifically, "pfcOK/REF5V" is low:

- During the PFC stage startup, that is, as long as the output voltage has not yet stabilized at the right level. The startup phase is detected by the latch "L_{STUP}" of the block diagram. "L_{STUP}" is set during each "off" phase so that its output ("STUP") is high when the circuit enters an active phase. The latch is reset when the error amplifier stops charging its output capacitor, that is, when the output voltage of the PFC stage has reached its desired regulation level. At that moment, "STUP" falls down to indicate the end of the startup phase.
- In case of a condition preventing the circuit from operating properly, i.e., during the V_{CC} charge by the high voltage startup current source, in a Brown−out case or when one of the following major faults turns off the circuit:

– Incorrect feeding of the circuit ("UVLO" high when V_{CC}<V_{CC}OFF, V_{CC}OFF equating 9 V typically).
– Excessive die temperature detected by the thermal shutdown.
– Undervoltage Protection
– Latched off of the circuit (when the "STDWN" pin, V_{Pin13}, exceeds 2.5 V).

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And “pfcOK/REF5V” is high when the PFC output voltage is properly and safely regulated. “pfcOK/REF5V” should be used to allow operation of the downstream converter.

Standby Management

The NCP1605 automatically skips switching cycles when the power demand drops below a given level. This is accomplished by monitoring the Pin 1 voltage that must receive a voltage below 300 mV in light load conditions. Practically, a portion of the feedback signal of the downstream converter (or some other signal able to indicate that the power demand is low) should be applied to Pin 1.

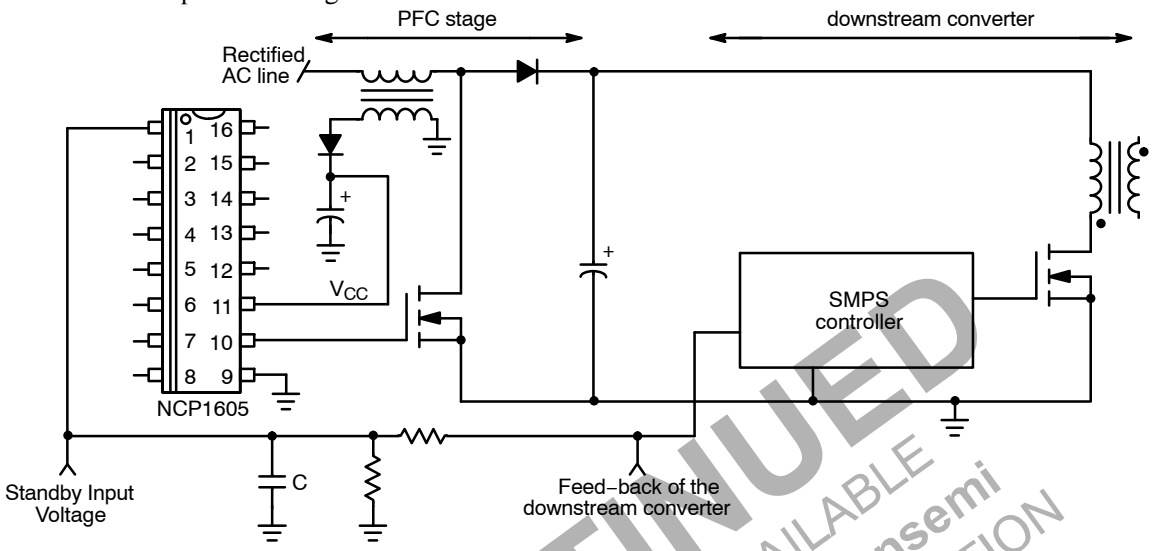


Figure 63. Signal for Standby Detection

In normal operation, the circuit controls the ***continuous*** absorption of the line current necessary for matching the load power demand. When the voltage applied to Pin 1 goes below 300 mV:

- The output pulses are blanked and Pin 3 (“$V_{CONTROL}$”) is grounded.
- The output of the PFC stage being not fed any more, it drops. When the output voltage goes below 95.5% of the regulation level, the circuit resumes operation until “FLAG1” becomes low (what means that the output voltage has exceeded the regulation level).
- At that moment, if V_{Pin1} is still below 300 mV, a new skipping phase starts.

In other words, instead of continuously providing the output with a small amount of power, the circuit operates from time to time at a higher power level. As an example and to make it simple, instead of continuously supplying 1% of P_{MAX}, the circuit can provide the load with 10% of P_{MAX} for 10% of the time. The IC enters the so−called skip cycle mode, also named controlled burst operation. This burst operation is much more efficient compared to a continuous power flow as it drastically reduces the number of pulsations and therefore the switching losses associated to them.

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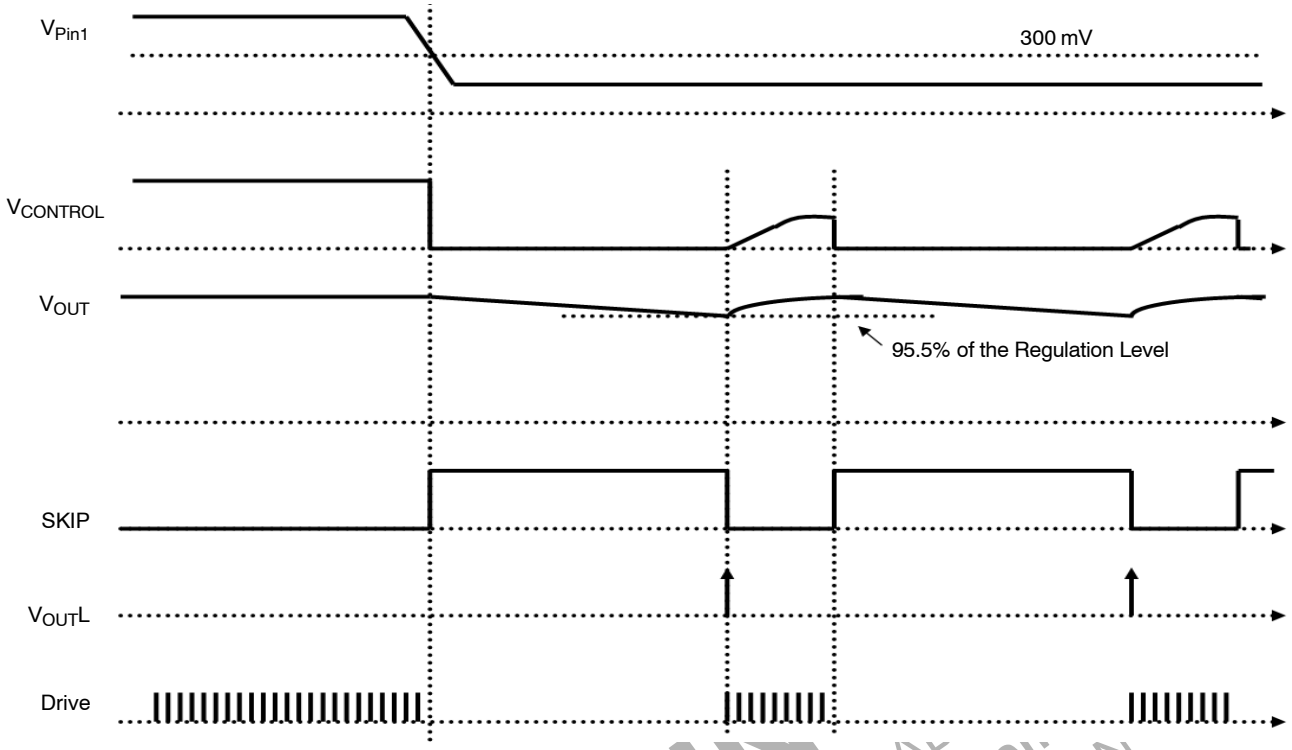


Figure 64. Standby Management

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Remark:

- Skip cycle is not allowed during the PFC startup phase to avoid that it interferes with the soft−start. That is why, skip cycle is enabled only when “pfcOK” is high.
- Each working phase of the burst mode starts smoothly as Pin 3 is grounded at the beginning of it. This soft−start capability is effective to avoid the audible noise that could possibly result from such a burst operation.
- The circuit leaves the standby mode when the output voltage goes below 95.5% of its regulation level **and** V_{Pin1} is above 330 mV (300 mV + 30 mV hysteresis).

Oscillator / Synchronization Section

The oscillator generates the clock signal to set the PWM latch and turn the MOSFET on. The oscillator frequency is set by the capacitor that is applied to Pin 8. Typically, 820 pF force about 60 kHz. The maximum allowable oscillator frequency is 250 kHz. The clock frequency can also be driven by an external synchronization signal.

This block contains two main parts (refer to Figure 66):

- The arrangement that consists of charging/discharging current sources, a switch and a comparator. When used in oscillator mode, a capacitor is connected between Pin 8 and ground. A current source (100 μA) charges the Pin 8 capacitor until its voltage exceeds VoscH. At that moment, the comparator (“COMP_OSC”) turns high and activates the discharge current source (200 μA). As a consequence, Pin 8 actually sinks 100 μA that discharge the oscillator capacitor to VoscL. At that moment, the comparator turns low and initiates a new charge phase. If the circuit is to be externally triggered, the synchronization signal must cross VoscL and VoscH to properly turn on and off the “COMP_OSC” comparator. Also the synchronization signal must be low impedance enough not to be distorted by the Pin 8 source and sink currents.
- The “storing circuitry” that contains a latch and some gates. The raising edge of the “COMP_OSC” output sets the “CLOCK Generation” latch to turn high the “CLK” signal. If the timing capacitor of Pin 7 is properly discharged (V_{Pin4} <50 mV leading to “C_TOK” high), the PWM block is ready for a new cycle and “CLK” can force the signal “V_{SET}” in high state. As a consequence, the PWM latch sets. In addition, “V_{SET}” resets the “CLOCK Generation” latch to make it ready for the next oscillator cycle. The two inverters of Figure 66, simply generate some delay to ensure that “V_{SET}” keeps high long enough to set the PWM latch and reset the “CLOCK Generation” latch (longer delay than that produced by the two gates, may actually be necessary).

The oscillator / Synchronization block is designed to set the switching frequency.

However, the coil current can possibly be non zero at the end of a clock period and the circuit would enter Continuous Conduction Mode (CCM) if the MOSFET turned on in that moment. In order to prevent CCM, the “storing circuitry” of the oscillator / synchronization block, memorizes the “COMP_OSC” rising edge (thanks to the “CLOCK Generation” latch) and delays the next MOSFET conduction time until the coil current has totally vanished (that is until the signal “DT” is high − “DT” is generated by the current sense block so that it is high during the dead−time and low otherwise). In other words, CRM operation is obtained (refer to Figure 65).

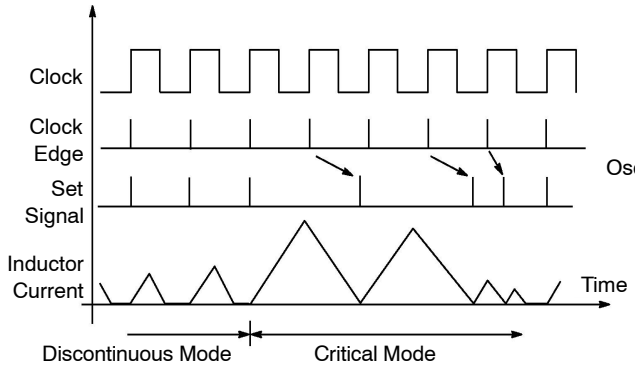


Figure 65. Oscillator Timing Diagram

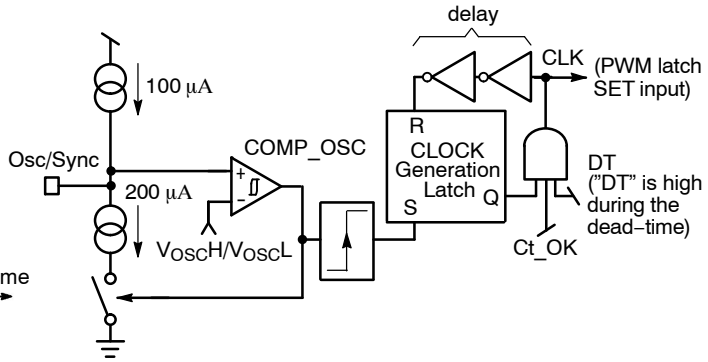
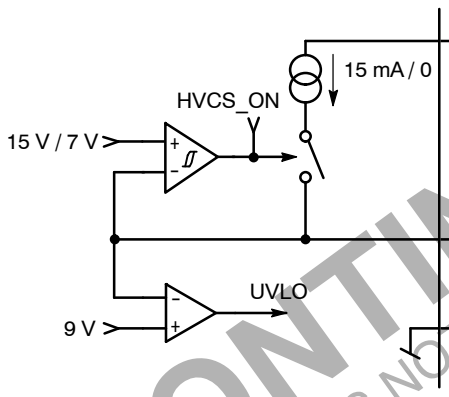


Figure 66. Oscillator / Synchronization Block



(When high, "UVLO" indicates that the circuit is not properly fed and it sets the Fault latch to turn off the circuit)

Figure 67. The Current Source brings V_{CC} above 15 V and then Turns Off

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Startup Sequence / V_{CC} Management

At the moment when the PFC stage is plugged to the mains outlet, the internal current source starts charging the V_{CC} capacitor. More generally, the startup current source is enabled whenever V_{CC} drops below V_{CC}STUP (7 V, typically). When V_{CC} exceeds the V_{CC}ON level (typically 15 V for the NCP1605 and NCP1605B, 10.5 V for the NCP1605A), the current source turns off and the circuit starts pulsing.

The energy stored by the V_{CC} capacitor serves to feed the controller and some auxiliary supply must take over before V_{CC} drops below V_{CC}OFF (9 V, typically), that is, the level below which the circuit stops pulsing.

Hence, the circuit starts operating when the V_{CC} voltage exceeds V_{CC}ON and stops pulsing when V_{CC} drops below V_{CC}OFF. The hysteresis (6 V for the NCP1605 and NCP1605B, 1.5 V for the NCP1605A) prevents erratic operation as the V_{CC} crosses the V_{CC}ON threshold.

Figure 67 shows the internal arrangement of this structure (the V_{CC} turn on threshold of Figure 67 is that of the NCP1605/B). One can note that the startup current source is *on* during the V_{CC} charging phase and *off* for the rest of the time. Hence, it spends no power during the PFC stage operation and in particular, in light load conditions. That is why the NCP1605 helps meet the most stringent standby requirements.

Remarks:

- Some circuitry (not represented in Figure 67) limits the HV pin current to IC2 (below 1 mA) if the V_{CC} voltage is below V_{CC}INHIBIT. This protects the circuit when the V_{CC} pin is accidentally grounded. The full current capability (around 15 mA) is obtained when V_{CC} exceeds V_{CC}INHIBIT.
- The circuit is also kept off when the startup current source is on to make a clear distinction between the V_{CC} charge phase and the operating sequence (refer to "HVCS_ON" signal on block diagram).

Brown−Out Detection

The brown−out pin receives a portion of the input voltage (V_{IN}). As V_{IN} is a rectified sinusoid, a capacitor must integrate the ac line ripple so that a voltage proportional to the average value of (V_{IN}) is applied to the brown−out pin.

The brown−out block detects too low input voltage conditions. A hysteresis comparator monitors the Pin 2 voltage. Before operation, the PFC stage is off and the input bridge acts as a peak detector. Hence, the voltage applied to Pin 2 is:

$$V_{pin2} = \sqrt{2}\,Vac\,\frac{R_{bo2}}{R_{bo1} + R_{bo2}}.$$

After the PFC stage has started operation, the input voltage becomes a rectified sinusoid and the voltage applied to Pin 2 is:

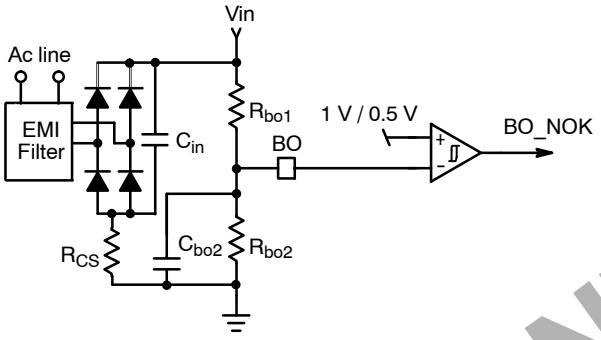


Figure 68. Brown−Out Block

$$V_{pin2} = \frac{2\sqrt{2}\,Vac}{\pi}\,\frac{R_{bo2}}{R_{bo1} + R_{bo2}},$$

i.e., about 64% of the previous value. Therefore, the same line magnitude leads to a V_{Pin2} voltage that is 36% lower when the PFC is working than when it is off (refer to Figure 69). That is why the NCP1605 features a 50% hysteresis ($V_{BO}L$ = 50% $V_{BO}H$).

When the circuit starts operation, the input voltage equates the ac line peak.

Hence, the initial threshold of the Brown−Out comparator, must be the upper one (V_{BO} = $V_{BO}H$ = 1 V when the NCP1605 leaves the off mode).

When a brown−out condition is detected, the signal "BO_NOK" turns off the circuit (refer to block diagram).

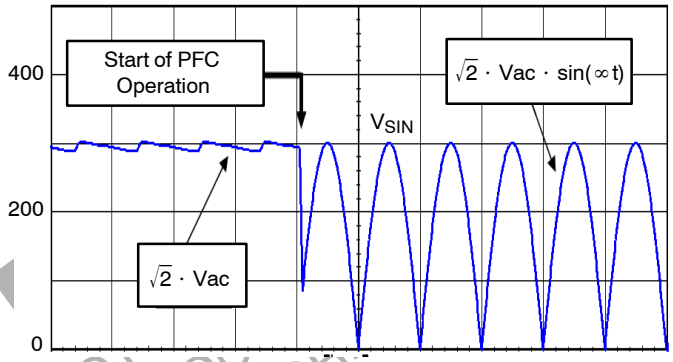


Figure 69. Typical Input Voltage of a PFC Stage

Thermal Shutdown (TSD)

An internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 150°C typically. The output stage is then enabled once the temperature drops below about 100°C (50°C hysteresis).

The temperature shutdown keeps active as long as the circuit is not reset, that is, as long as V_{CC} keeps higher than V_{CC}RESET. The reset action forces the TSD threshold to be the upper one (150°C). This ensures that any cold startup will be done with the right TSD level.

Output Drive Section

The output stage contains a totem pole optimized to minimize the cross conduction current during high frequency operation. The gate drive is kept in a sinking mode whenever the Undervoltage Lockout is active or more generally whenever the circuit is off (i.e., when the "Fault Latch" of the block diagram is high or when the HV current source is on). Its high current capability (−500 mA/+800 mA) allows it to effectively drive high gate charge power MOSFET.

Reference Section

The circuit features an accurate internal reference voltage (V_{REF}). V_{REF} is optimized to be ±3% accurate over the temperature range (the typical value is 2.5 V). V_{REF} is the voltage reference used for the regulation and the overvoltage protection. The circuit also incorporates a precise current reference (I_{REF}) that allows the Overcurrent Limitation to feature a ±6% accuracy over the temperature range.

OFF Mode

As previously mentioned, the circuit turns off in the following cases:

- When the high voltage, startup current source charges the V_{CC} capacitor.
- When one of the following major faults is detected:
- Incorrect feeding of the circuit ("UVLO" high when V_{CC}<V_{CC}OFF, V_{CC}OFF equating 9 V typically).
- Excessive die temperature detected by the thermal shutdown.
- Brown−Out condition.
- Undervoltage Protection.
- V_{Pin13} higher than 2.5 V ("STDWN" of the block diagram turns high).

Generally speaking, the circuit turns off when the conditions are not proper for good operation. In this mode, the controller stops operating. The major part of the circuit sleeps and its consumption is minimized (< 500 μA).

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More specifically, when the circuit is in OFF state:

- The drive output is kept low
- All the blocks are off except:
  1. The UVLO circuitry that keeps monitoring the V_{CC} voltage and controlling the startup current source accordingly.
  2. The TSD (thermal shutdown)
  3. The "STDWN" latch that stores its output state.
  4. The Undervoltage Protection ("UVP").
  5. The brown−out circuitry. One must note that the comparator is reset during the latched−off phase so that its threshold is the upper one (1 V) when the circuit enters the active phase (refer to next "V_{CC} sequences" section).
  6. The high voltage, startup current source when the circuit is in startup phase (that is when V_{CC} is lower than V_{CC}STUP).
- The Pin 3 capacitor is discharged and kept grounded along the OFF time, to initialize it for the next operating sequence, where it must be slowly and gradually charged to offer some soft−start.
- The "pfcOK" pin is grounded.
- The output of the "V_{TON} processing block" is grounded

V_{CC} Sequences

The following table summarizes the state of the circuit in accordance to the V_{CC} level.

V_{CC} Conditions	"OFF" is Low (no condition forces the circuit off)	"OFF" is High (due to some protection like the thermal shutdown)
V_{CC} exceeds V_{CC}ON ⇒ the circuit enters the working phase	The startup current source is disabled The circuit is fully active	The startup current source is disabled The circuit is in OFF state
V_{CC} drops below V_{CC}OFF ⇒ the circuit enters the latched−off phase	The circuit is in OFF state The brown−out block resets during the latched−off phase so that its comparator threshold is forced to be the upper one (1 V)	The circuit is in OFF state The brown−out block resets during the latched−off phase so that its comparator threshold is forced to be the upper one (1 V)
V_{CC} goes below V_{CC}STUP ⇒ the circuit enters the startup phase	The high voltage, startup current source turns on to charge V_{CC}. The drive output and the "pfcOK" are in low state (the circuit is off) All the circuit blocks are reset except: The thermal shutdown (TSD) and the brown−out block that keep operating The "STDWN" latch.	The high voltage, startup current source turns on to charge V_{CC}. The drive output and the "pfcOK" are in low state (the circuit is off) All the circuit blocks are reset except: The thermal shutdown (TSD) and the brown−out block that keep operating The "STDWN" latch.
V_{CC} goes below V_{CC}RESET ⇒ the circuit resets	The high voltage, startup current source is on. The whole circuitry is reset including the "TSD" and the "STDWN" latch. After reset, the TSD threshold is 150°C and the output of the "STDWN latch" is low.	The high voltage, startup current source is on. The whole circuitry is reset including the "TSD" and the "STDWN" latch. After reset, the TSD threshold is 150°C and the output of the "STDWN latch" is low.

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The figures on the following pages portray the circuit behavior during a startup phase:

- In case of normal conditions (Figure 70).
- As a function of the brown−out pin voltage (Figure 71).

Remarks:

The $V_{CONTROL}$ signal does not necessarily reach its clamp level (3.7 V) depending of the load and of the system time constants. In particular, if the circuit starts operation in light load and if the bulk capacitor is not too large, the output voltage V_{OUT} generally exceeds the regulation level while $V_{CONTROL}$ keeps below its upper limit.

The output voltage exhibits a 100 or 120 Hz ripple (at twice the line frequency). This ripple is also present in the $V_{CONTROL}$ voltage even if it is attenuated due to the regulation low bandwidth. Like that of V_{OUT}, this ripple is not represented in Figure 70, for the sake of the clarity.

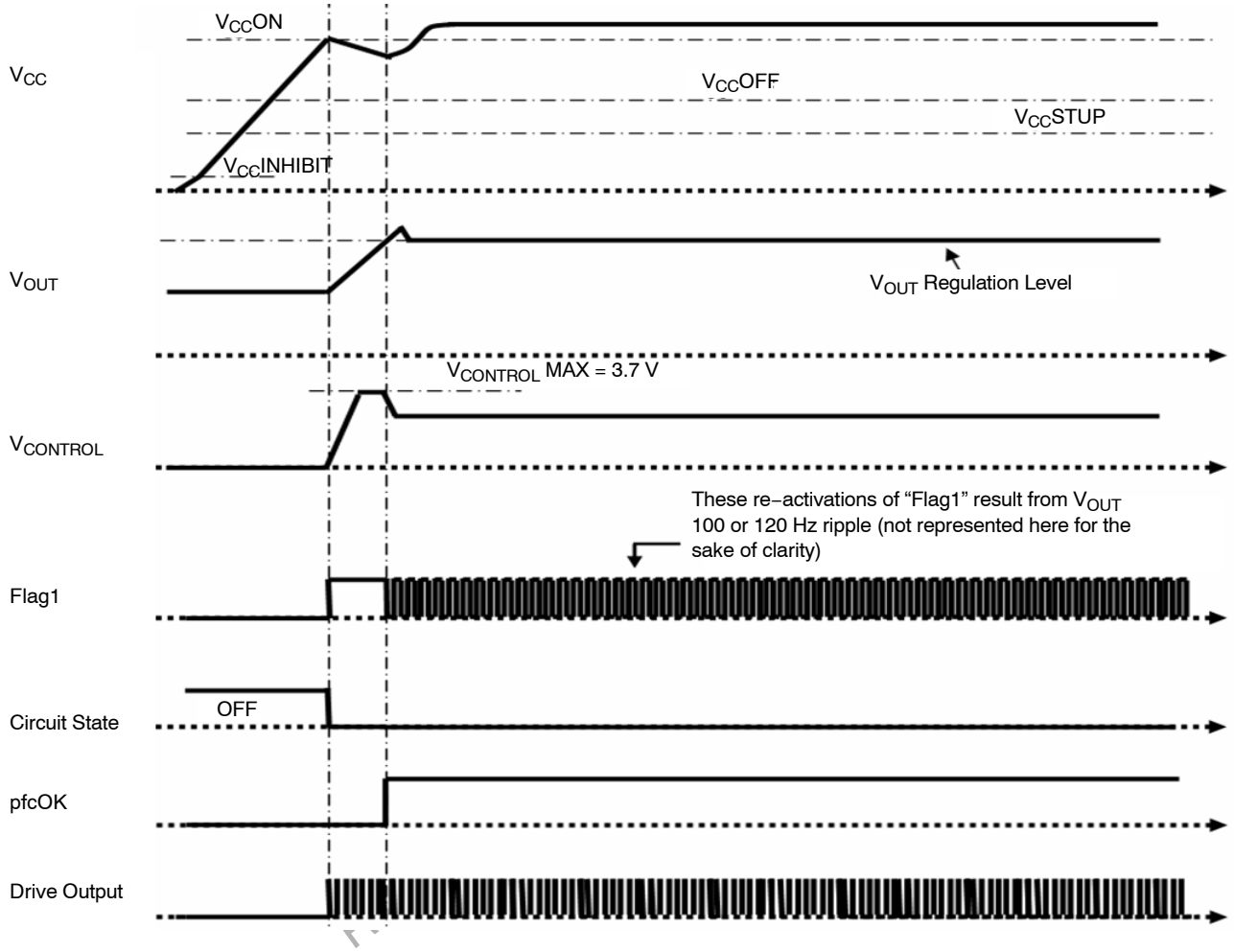


Figure 70. Startup Phase in Normal Conditions

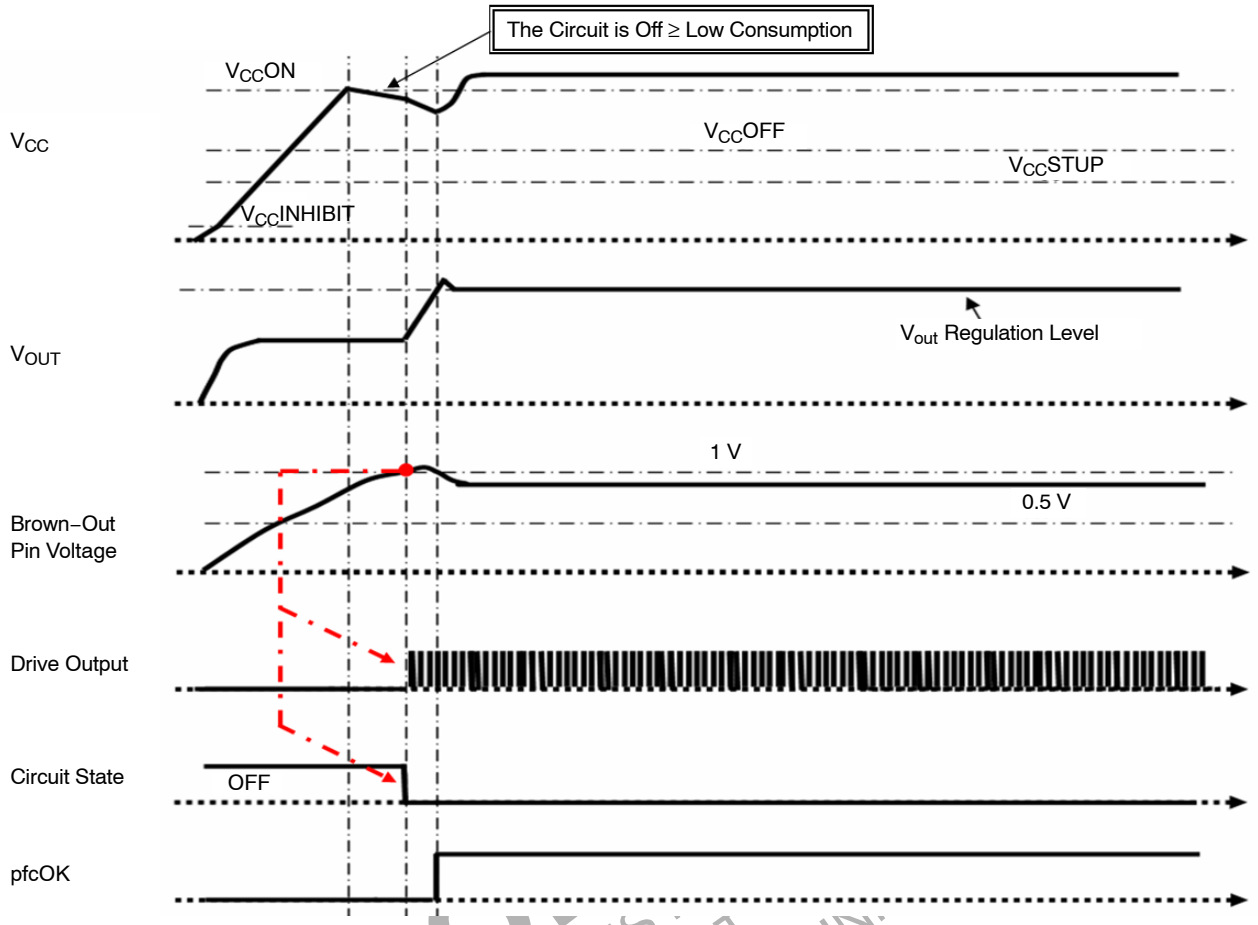


Figure 71. Startup and Brown Out Conditions

When the high voltage, startup current source is on, the brown−out is active and its threshold is the upper one (V_{BO} = V_{BO}H = 1 V).

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Fault Management Block

When any of the following faults is detected: brown−out (“BO_NOK”), Undervoltage (“UVP”), shutdown (“STDWN”), Die Overtemperature (“TSD”), the circuit immediately turns off and recovers operation as soon as the fault disappears.

In case of UVLO (V_{CC} too low to allow operation), the circuit keeps off until the end of the next V_{CC} charge phase by the HV startup current source.

The following block diagram details the function.

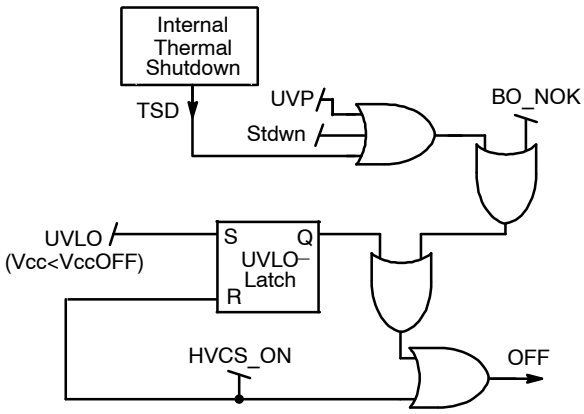


Figure 72. Fault Management Block

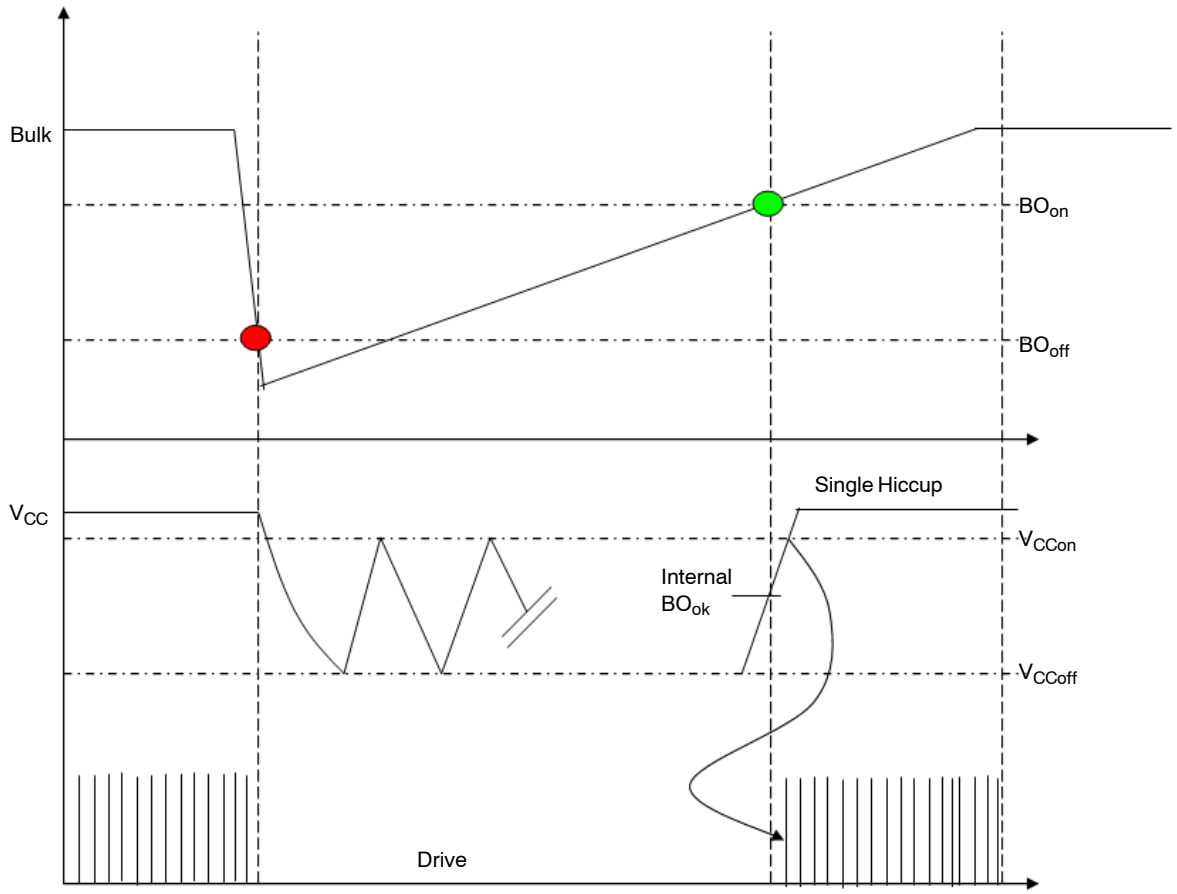


Figure 73.

The above figure shows how the circuit recovers after a brown−out event.

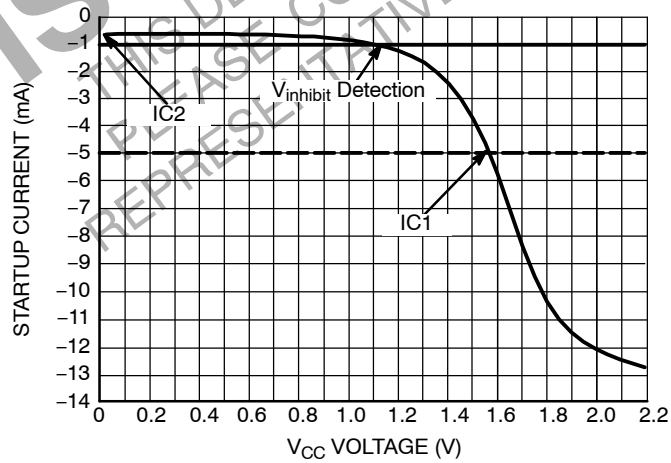


Figure 74. Startup Current vs. V_{CC} Voltage

VCC_inhibit is defined as the point at which IC2 current reaches 1 mA at this point VCC is logged as VCC_inhibit. At 5 mA the current becomes the IC2 startup current.

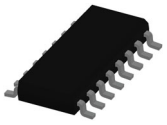
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REVISION HISTORY

Revision	Description of Changes	Date
13	Document Discontinued.	5/18/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

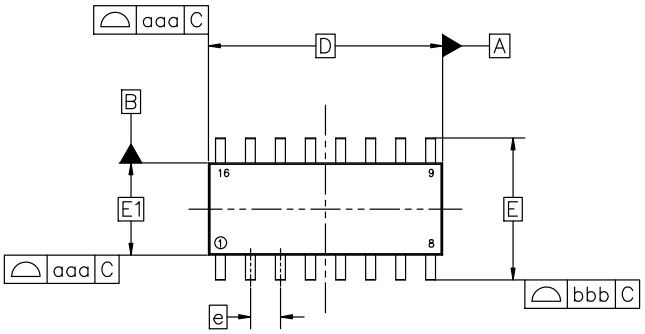
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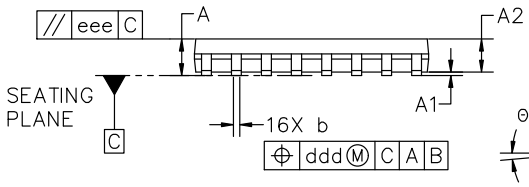
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

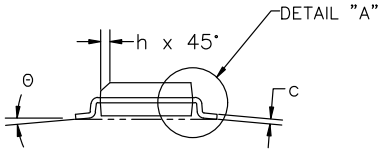
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



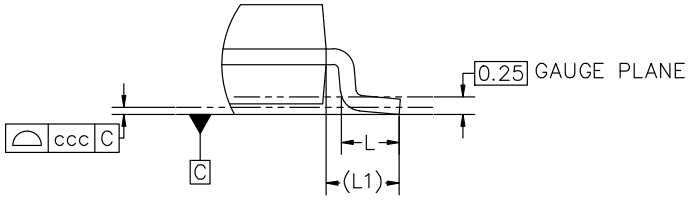
TOP VIEW



SIDE VIEW

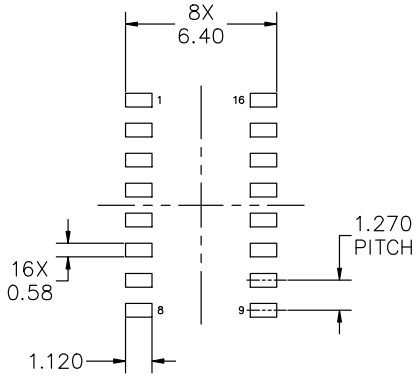


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



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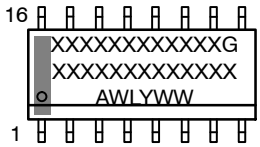
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SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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