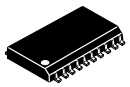
# Octal Bus Buffer

## With 5V−Tolerant Inputs

# MC74LVX244



SOIC−20
DW SUFFIX
CASE 751D



TSSOP−20
DT SUFFIX
CASE 948E

The MC74LVX244 is an advanced high speed CMOS non−inverting 3−state octal bus buffer and has two active low output enables. It is also designed to work with 3−state memory address drivers, etc. The inputs tolerate voltages up to 6.5 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed: $t_{PD}$ = 4.7 ns (Typ) at $V_{CC}$ = 3.3 V
- Low Power Dissipation: $I_{CC}$ = 4 μA (Max) at $T_A$ = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP}$ = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  Human Body Model > 2000 V
- These Devices are Pb−Free and are RoHS Compliant

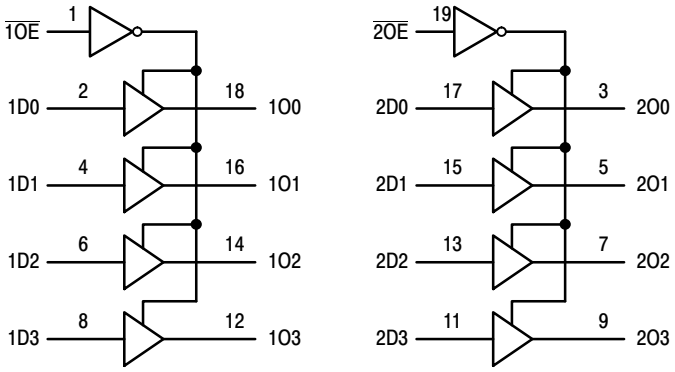



**Figure 1. Logic Diagram**

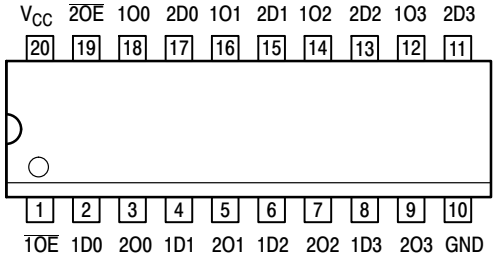
### PIN NAMES

| Pins | Function |
|---|---|
| $\overline{n}$OE<br>1Dn, 2Dn<br>1On, 2On | Output Enable Inputs<br>Data Inputs<br>3−State Outputs |

### FUNCTION TABLE

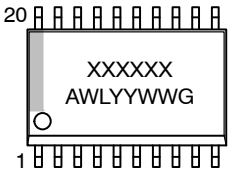
| INPUTS | | OUTPUTS |
|---|---|---|
| $\overline{1OE}$, $\overline{2OE}$ | 1Dn, 2Dn | 1On, 2On |
| L<br>L<br>H | L<br>H<br>X | L<br>H<br>Z |

### PIN ASSIGNMENT

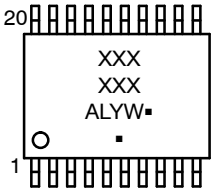



**20−Lead** (Top View)

### MARKING DIAGRAMS




**SOIC−20**




**TSSOP−20**

| | |
|---|---|
| XXXXXX | = Specific Device Code |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | –0.5 to +6.5 | V |
| $V_{in}$ | DC Input Voltage | | –0.5 to +6.5 | V |
| $V_{out}$ | DC Output Voltage | | –0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | Input Diode Current | | –20 | mA |
| $I_{OK}$ | Output Diode Current | | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ±75 | mA |
| $P_D$ | Power Dissipation | SOIC<br>TSSOP | 1302<br>833 | mW |
| $T_{stg}$ | Storage Temperature | | –65 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | 2.0 | 3.6 | V |
| $V_{in}$ | DC Input Voltage | 0 | 5.5 | V |
| $V_{out}$ | DC Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | –40 | +85 | °C |
| $\Delta t/\Delta V$ | Input Rise and Fall Time | 0 | 100 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $T_A$ = 25°C | | | $T_A$ = –40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | High–Level Input Voltage | | 2.0<br>3.0<br>3.6 | 1.5<br>2.0<br>2.4 | | | 1.5<br>2.0<br>2.4 | | V |
| $V_{IL}$ | Low–Level Input Voltage | | 2.0<br>3.0<br>3.6 | | | 0.5<br>0.8<br>0.8 | | 0.5<br>0.8<br>0.8 | V |
| $V_{OH}$ | High–Level Output Voltage<br>($V_{in}$ = $V_{IH}$ or $V_{IL}$) | $I_{OH}$ = –50 μA<br>$I_{OH}$ = –50 μA<br>$I_{OH}$ = –4 mA | 2.0<br>3.0<br>3.0 | 1.9<br>2.9<br>2.58 | 2.0<br>3.0 | | 1.9<br>2.9<br>2.48 | | V |
| $V_{OL}$ | Low–Level Output Voltage<br>($V_{in}$ = $V_{IH}$ or $V_{IL}$) | $I_{OL}$ = 50 μA<br>$I_{OL}$ = 50 μA<br>$I_{OL}$ = 4 mA | 2.0<br>3.0<br>3.0 | | 0.0<br>0.0 | 0.1<br>0.1<br>0.36 | | 0.1<br>0.1<br>0.44 | V |
| $I_{in}$ | Input Leakage Current | $V_{in}$ = 5.5V or GND | 3.6 | | | ±0.1 | | ±1.0 | μA |
| $I_{OZ}$ | Maximum 3–State Leakage Current | $V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 3.6 | | | ±0.2<br>5 | | ±2.5 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{in}$ = $V_{CC}$ or GND | 3.6 | | | 4.0 | | 40.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Test Conditions | $T_A = 25°C$ Min | Typ | Max | $T_A = -40$ to $85°C$ Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Input to Output | $V_{CC}$ = 2.7 V $C_L$ = 15 pF | | 6.1 | 11.4 | 1.0 | 13.5 | ns |
| | | $V_{CC}$ = 2.7 V $C_L$ = 50 pF | | 8.6 | 14.9 | 1.0 | 17.0 | |
| | | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF | | 4.7 | 7.1 | 1.0 | 8.5 | |
| | | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 50 pF | | 7.2 | 10.6 | 1.0 | 12.0 | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time to High and Low Level | $V_{CC}$ = 2.7 V $R_L$ = 1 kΩ $C_L$ = 15 pF | | 7.1 | 13.8 | 1.0 | 16.5 | ns |
| | | $V_{CC}$ = 2.7 V $R_L$ = 1 kΩ $C_L$ = 50 pF | | 9.6 | 17.3 | 1.0 | 20.0 | |
| | | $V_{CC}$ = 3.3 ± 0.3 V $R_L$ = 1 kΩ $C_L$ = 15 pF | | 5.5 | 8.8 | 1.0 | 10.5 | |
| | | $V_{CC}$ = 3.3 ± 0.3 V $R_L$ = 1 kΩ $C_L$ = 50 pF | | 8.0 | 12.3 | 1.0 | 14.0 | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time From High and Low Level | $V_{CC}$ = 2.7 V $R_L$ = 1 kΩ $C_L$ = 50 pF | | 11.6 | 16.0 | 1.0 | 19.0 | ns |
| | | $V_{CC}$ = 3.3 ± 0.3 V $R_L$ = 1 kΩ $C_L$ = 50 pF | | 9.7 | 11.4 | 1.0 | 13.0 | |
| $t_{OSHL}$ $t_{OSLH}$ | Output−to−Output Skew (Note 1) | $V_{CC}$ = 2.7 V $C_L$ = 50 pF | | | 1.5 | | 1.5 | ns |
| | | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 50 pF | | | 1.5 | | 1.5 | |

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW ($t_{OSHL}$) or LOW−to−HIGH ($t_{OSLH}$); parameter guaranteed by design.

## CAPACITIVE CHARACTERISTICS

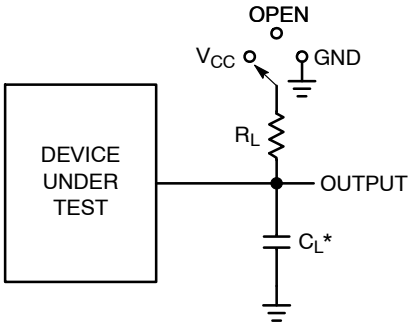
| Symbol | Parameter | $T_A = 25°C$ Min | Typ | Max | $T_A = -40$ to $85°C$ Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| Cin | Input Capacitance | | 4 | 10 | | 10 | pF |
| $C_{out}$ | Maximum Three−State Output Capacitance | | 6 | | | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 2) | | 19 | | | | pF |

2. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

| Symbol | Characteristic | $T_A = 25°C$ Typ | Max | Unit |
|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 0.5 | 0.8 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | −0.5 | −0.8 | V |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

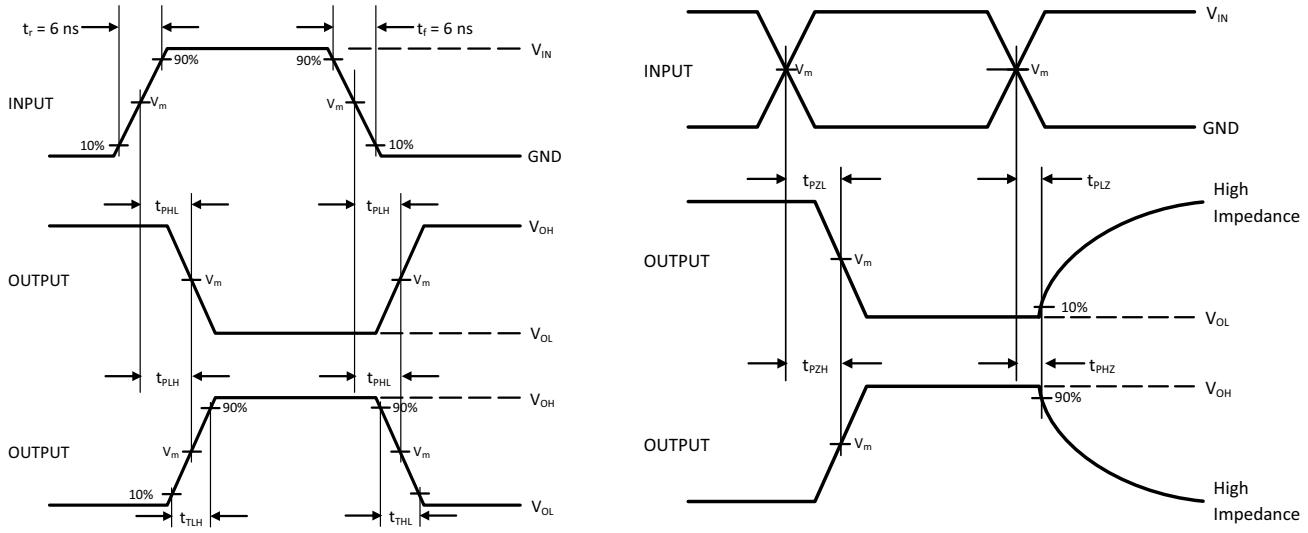

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*$C_L$ Includes probe and jig capacitance

| Test | Switch Position | $C_L$ | $R_L$ |
|---|---|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open | See AC Charac-teristics Table | 1 kΩ |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{CC}$ | | |
| $t_{PHZ}$ / $t_{PZH}$ | GND | | |

**Figure 2. Test Circuit**




| Device | $V_{IN}$, V | $V_m$, V |
|---|---|---|
| MC74LVX244 | $V_{CC}$ | 50% x $V_{CC}$ |

**Figure 3. Switching Waveforms**

## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MC74LVX244DWR2G | LVX244 | SOIC−20 (Pb−Free) | 1000 / Tape & Reel |
| MC74LVX244DTG | LVX 244 | TSSOP−20 (Pb−Free) | 50 Units / Rail |
| MC74LVX244DTR2G | LVX 244 | TSSOP−20 (Pb−Free) | 2500 / Tape & Reel |

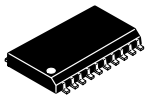
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



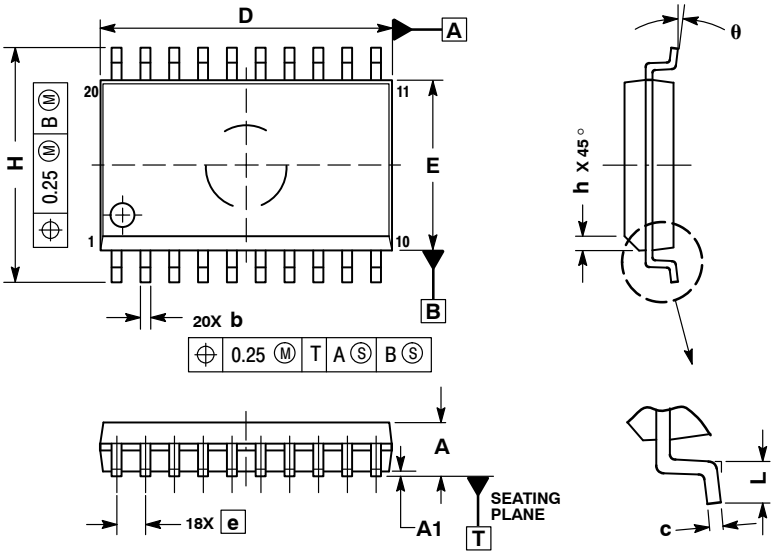
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**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



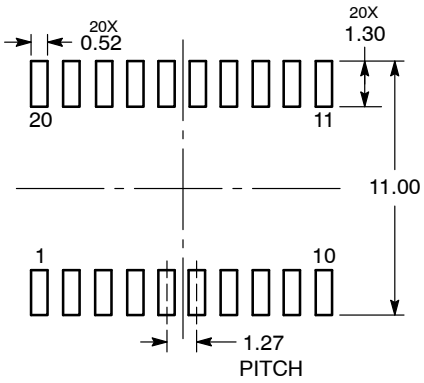
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

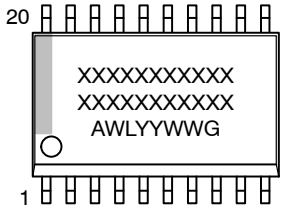
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
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