ESD Protection Diode

Low Capacitance ESD Protection Diode for High Speed Data Line

ESD7002, SZESD7002

The ESD7002 surge protection device is designed to protect high speed data lines from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0 and HDMI.

Features

- Low Capacitance (0.3 pF Typical, I/O to GND)
- Diode capacitance matching
- Protection for the Following IEC Standards:
  IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

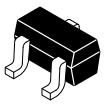
- USB2.0/3.0
- LVDS
- HDMI
- High Speed Differential Pairs

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

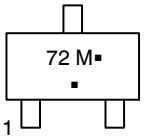
Rating	Symbol	Value	Unit
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T_L	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Contact (ESD) IEC 61000-4-2 Air (ESD) ISO 10605 Contact (330 pF / 330 Ω) ISO 10605 Contact (330 pF / 2 kΩ) ISO 10605 Contact (150 pF / 2 kΩ)	ESD	±8 ±0.4 ±8 ±15 ±8 ±15 ±24	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM

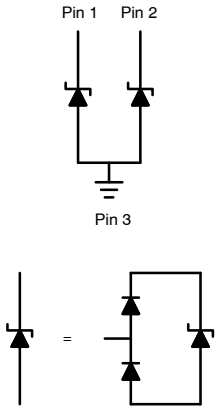


SC-70
CASE 419
STYLE 4



72 = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

Device	Package	Shipping†
ESD7002WTT1G	SC-70 (Pb-Free)	3000 / Tape & Reel
SZESD7002WTT1G*		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

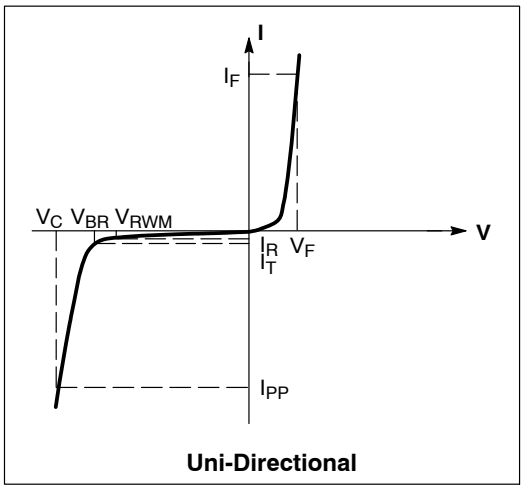
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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni-Directional

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			16	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	16.5	23		V
Reverse Leakage Current	I_R	V_{RWM} = 5 V, I/O Pin to GND			1	μA
Clamping Voltage (Note 1)	V_C	IEC61000-4-2, ±8 kV Contact	See Figures 3 and 4			
Clamping Voltage TLP (Note 2)	V_C	I_{TLP} = 8 A I_{TLP} = 16 A I_{TLP} = −8 A I_{TLP} = −16 A		31.2 33.9 −5.5 −10.8		V
Clamping Voltage 8/20 s Waveform (See Figures 5, 6)	V_C	I_{PP} = 1 A		28.7		V
Junction Capacitance Match	ΔC_J	V_R = 0 V, f = 1 MHz between I/O1 to GND and I/O 2 to GND		5	10	%
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins		0.2	0.4	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.3	0.5	pF
3dB Bandwidth	f_{BW}	R_L = 50 Ω		5		GHz
Insertion Loss	I_L	f = 1 GHz f = 5 GHz		0.06 0.5		dB
Return Loss	R_L	f = 1 GHz f = 5 GHz		25.9 9.0		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 13 and 14 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

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TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

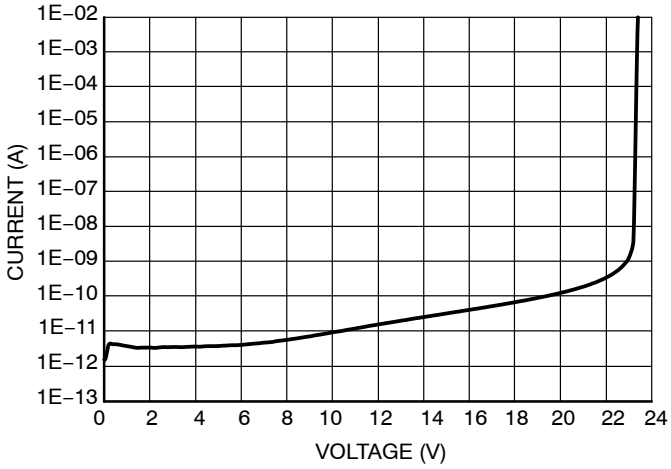


Figure 1. Typical IV Characteristic Curve

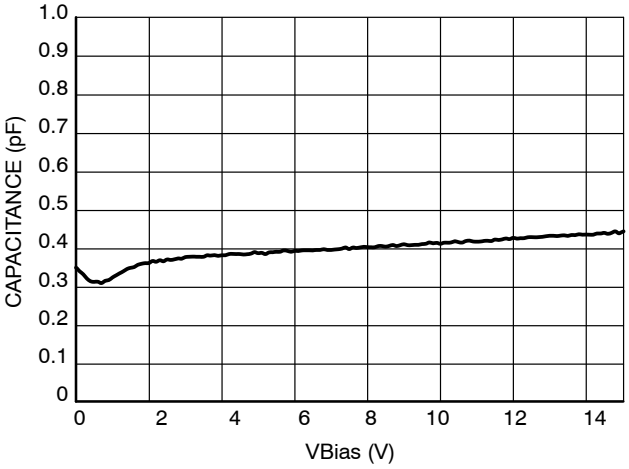


Figure 2. Typical CV Characteristic Curve

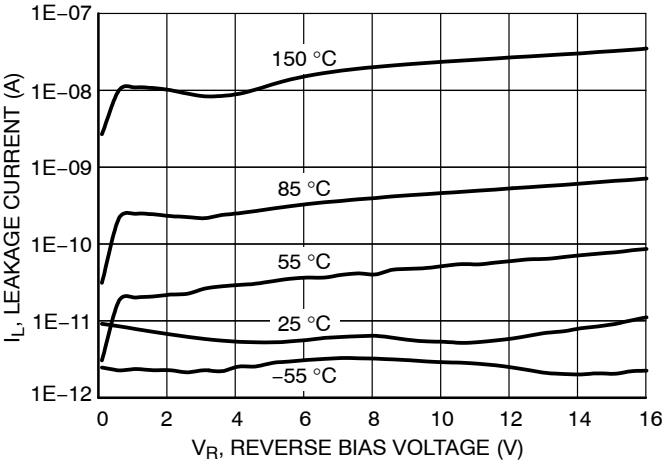


Figure 3. I_R vs. Temperature

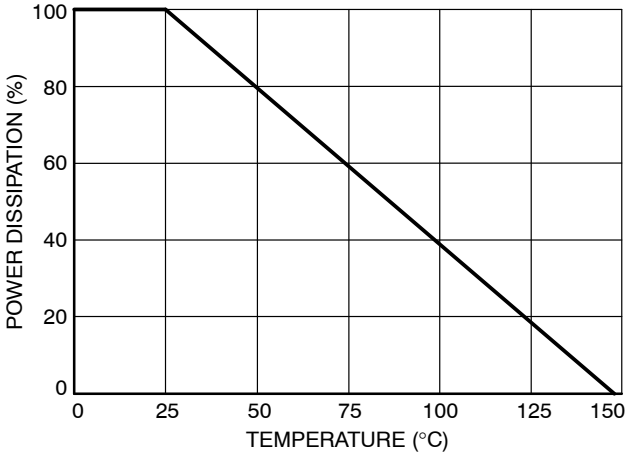


Figure 4. Steady State Power Derating

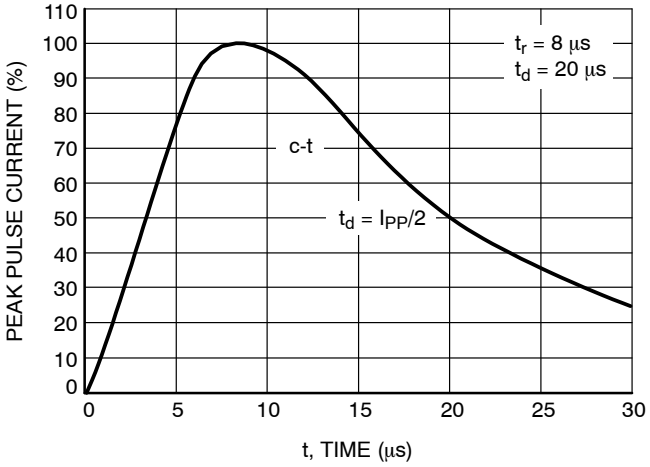


Figure 5. Pulse Waveform (8/20 μs)

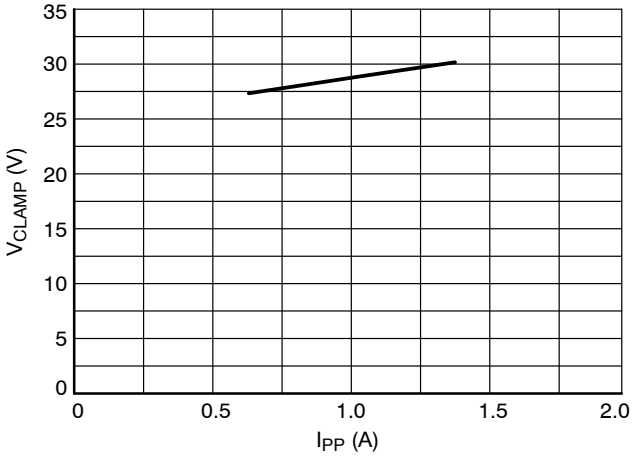


Figure 6. Clamping Voltage vs. Peak Pulse Current (8/20 μs)

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TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

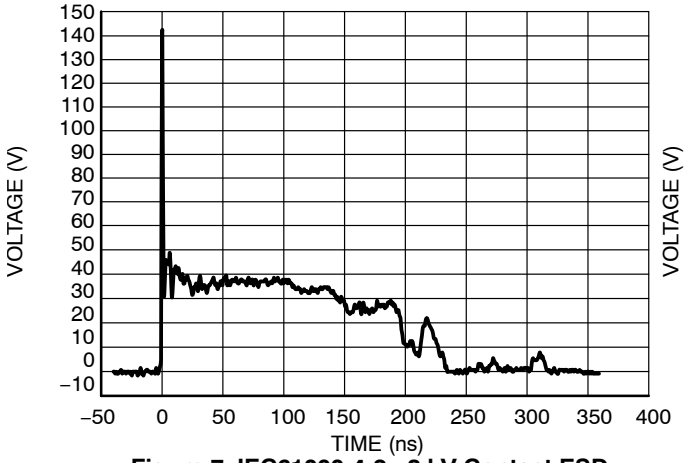


Figure 7. IEC61000-4-2 +8 kV Contact ESD Clamping Voltage

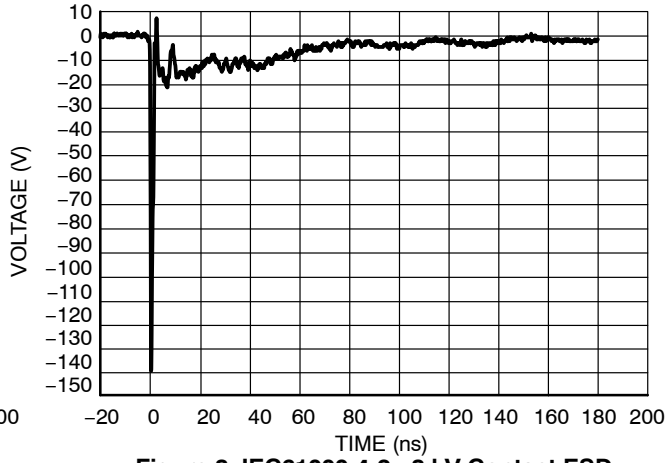


Figure 8. IEC61000-4-2 −8 kV Contact ESD Clamping Voltage

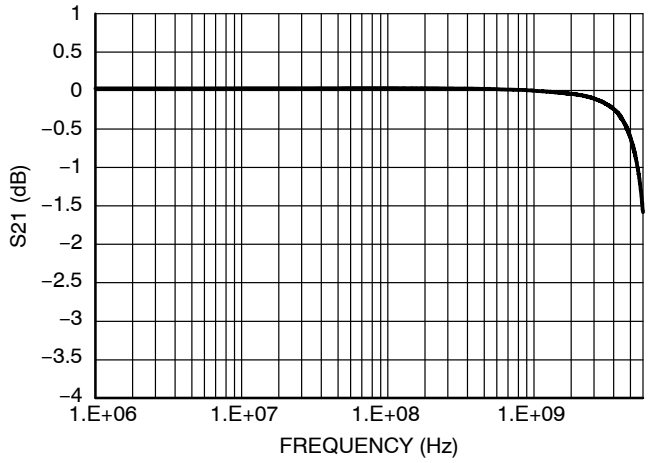


Figure 9. Typical Insertion Loss

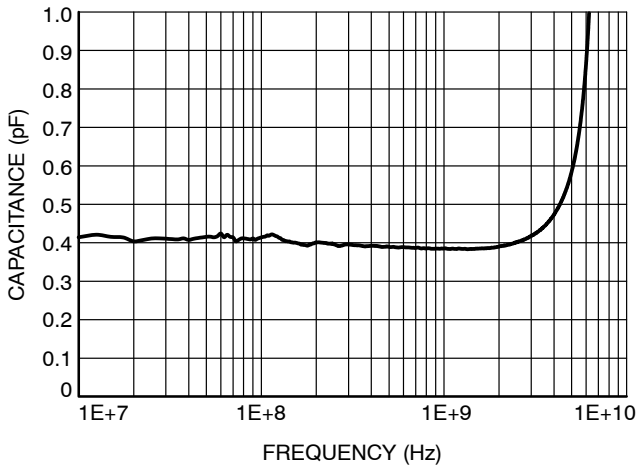


Figure 10. Typical Capacitance vs. Frequency

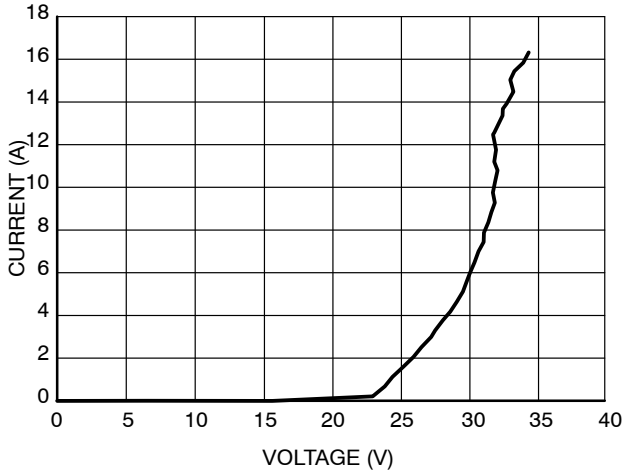


Figure 11. Positive TLP IV Curve

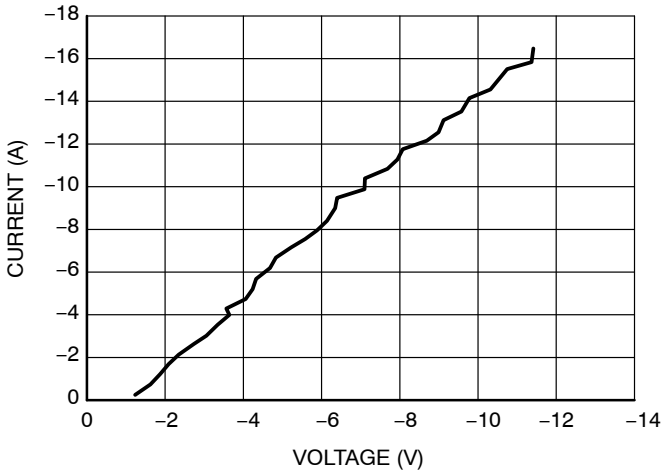


Figure 12. Negative TLP IV Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns.

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IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

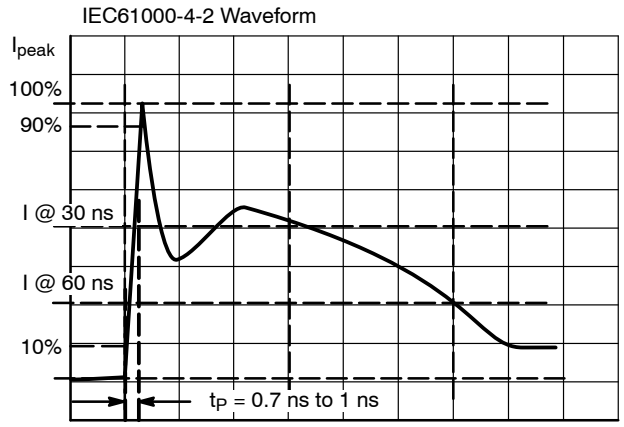


Figure 13. IEC61000-4-2 Spec

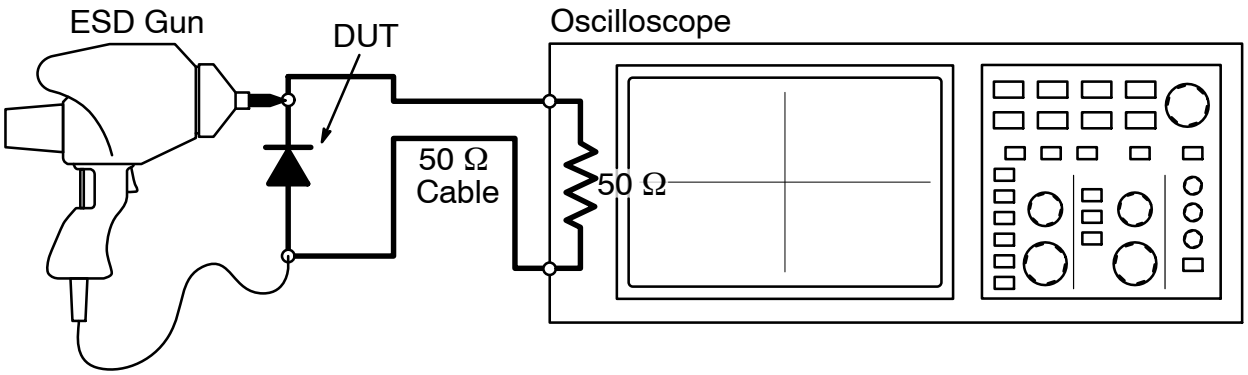


Figure 14. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

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Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 15. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 16 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

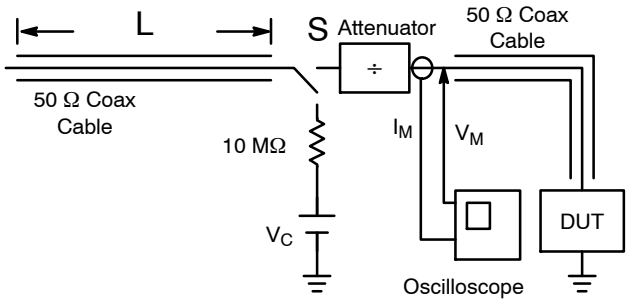


Figure 15. Simplified Schematic of a Typical TLP System

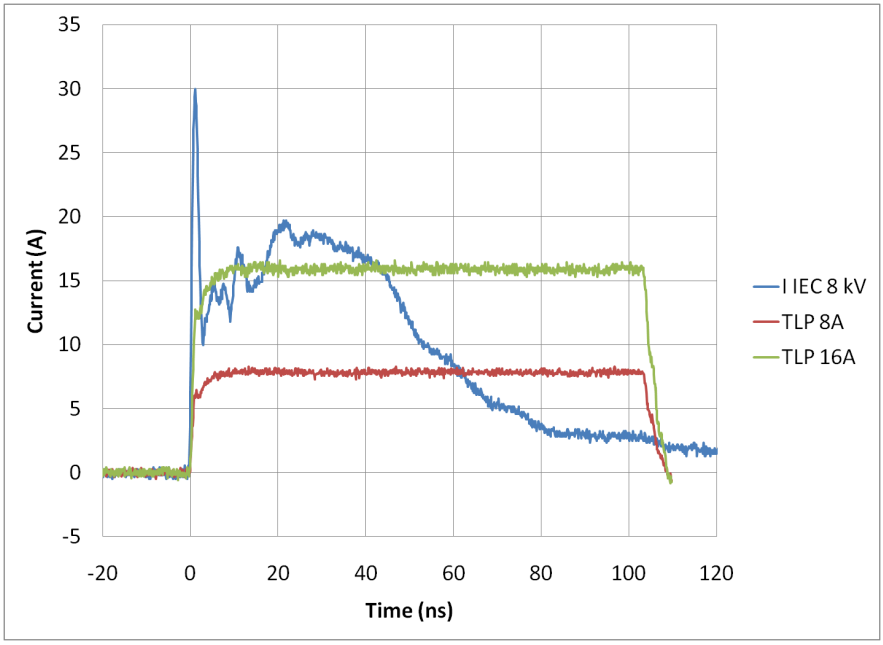


Figure 16. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

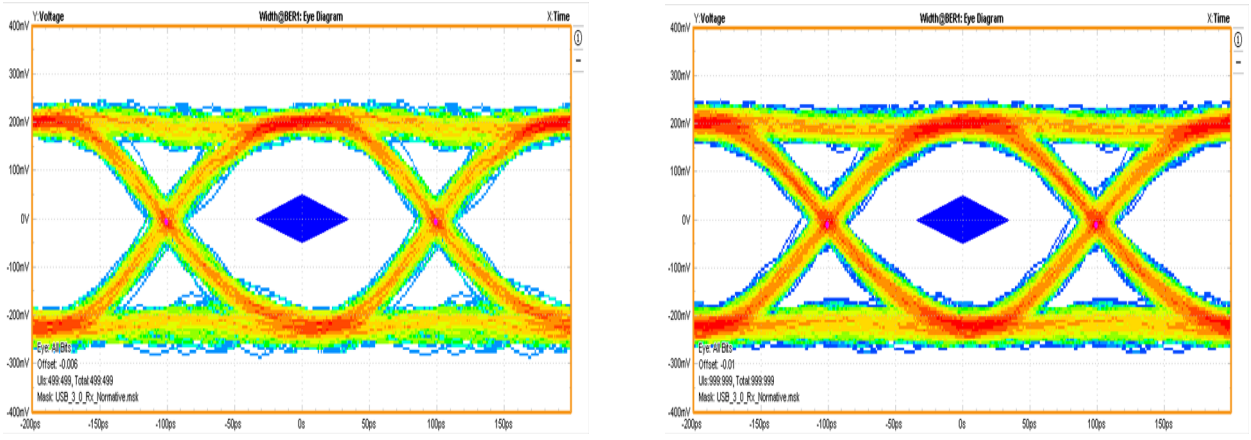


Figure 17. USB3.0 Eye Diagram with and without ESD7002 at 5 Gb/s

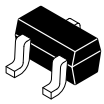
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REVISION HISTORY

Revision	Description of Changes	Date
6	Replace the max ratings table, add new page 2 data, edits to the EC table, rearrange characteristics curves and add three more, move the order info table	5/8/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

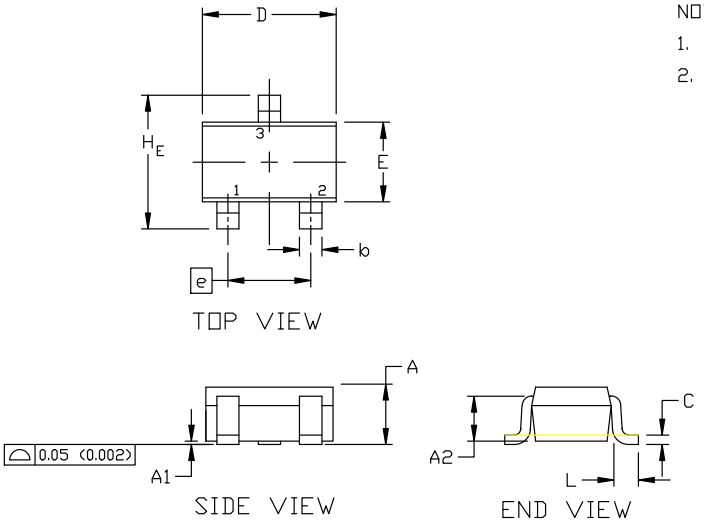
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SCALE 4:1

SC−70 (SOT−323)
CASE 419
ISSUE R

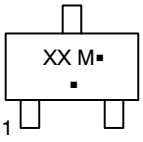
DATE 11 OCT 2022



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

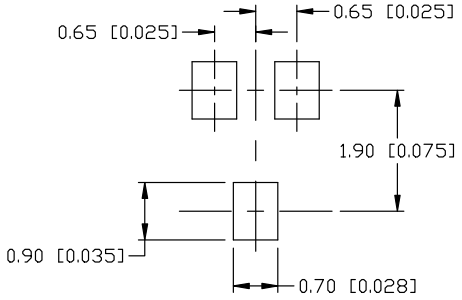
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

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