Dual Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

EMG2DXV5, EMG5DXV5

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT−553 package which is designed for low power surface mount applications.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Moisture Sensitivity Level: 1
- Available in 8 mm, 7 inch Tape and Reel
- Lead−Free Solder Plating
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Rating	Value	Unit
V_{CBO}	Collector-Base Voltage	50	Vdc
V_{CEO}	Collector-Emitter Voltage	50	Vdc
I_C	Collector Current	100	mAdc

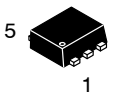
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

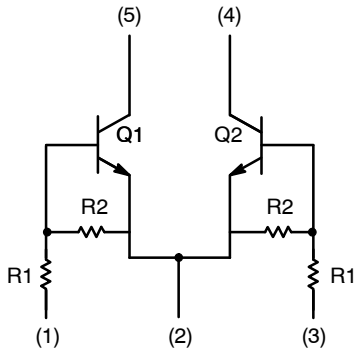
Symbol	Characteristic	Max	Unit
P_D	Total Device Dissipation T_A = 25°C Derate above 25°C	230 (Note 1) 338 (Note 2) 1.8 (Note 1) 2.7 (Note 2)	mW °C/W
$R_{\theta JA}$	Thermal Resistance – Junction-to-Ambient	540 (Note 1) 370 (Note 2)	°C/W
$R_{\theta JL}$	Thermal Resistance – Junction-to-Lead	264 (Note 1) 287 (Note 2)	°C/W
T_J, T_{stg}	Junction and Storage Temperature Range	−55 to +150	°C

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 x 1.0 inch Pad

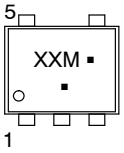
NPN SILICON BIAS RESISTOR TRANSISTORS



SOT−553
CASE 463B



MARKING DIAGRAM



XX = UF (EMG5)
UP (EMG2)
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

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DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1 (K)	R2 (K)
EMG2DXV5	SOT−553	UP	47	47
EMG5DXV5	SOT−553	UF	10	47

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Q1 & Q2)					
I_{CBO}	Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	–	–	100	nAdc
I_{CEO}	Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	–	–	500	nAdc
I_{EBO}	Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0) EMG2DXV5 EMG5DXV5	– –	– –	0.1 0.2	mAdc
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	50	–	–	Vdc
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)	50	–	–	Vdc
ON CHARACTERISTICS (Q1 & Q2) (Note 3)					
h_{FE}	DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA) EMG2DXV5 EMG5DXV5	80 80	140 140	– –	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (IC = 10 mA, I_B = 0.3 mA)	–	–	0.25	Vdc
V_{OL}	Output Voltage (on) (V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ) EMG2DXV5 (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ) EMG5DXV5	 – –	 – –	 0.2 0.2	Vdc
V_{OH}	Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	4.9	–	–	Vdc
R_1	Input Resistor EMG2DXV5 EMG5DXV5	32.9 7.0	47 10	61.1 13	kΩ
R_1/R_2	Resistor Ratio EMG2DXV5 EMG5DXV5	0.8 0.17	1.0 0.21	1.2 0.25	

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

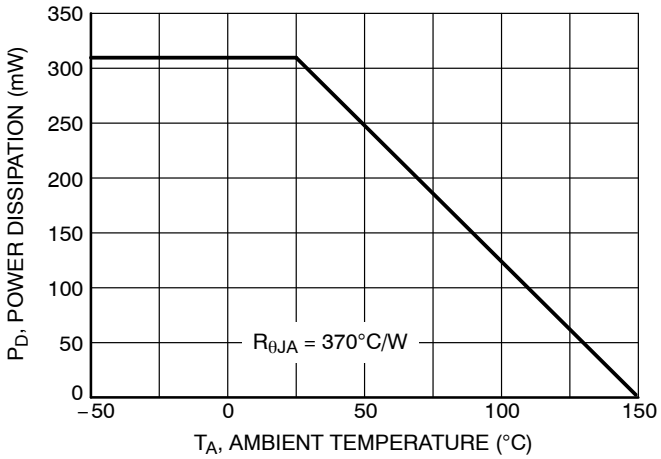


Figure 1. Derating Curve

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TYPICAL ELECTRICAL CHARACTERISTICS — EMG2DXV5

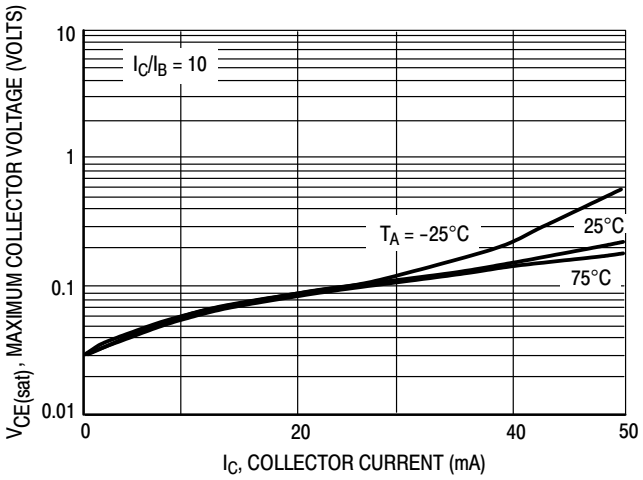


Figure 2. $V_{CE(sat)}$ versus I_C

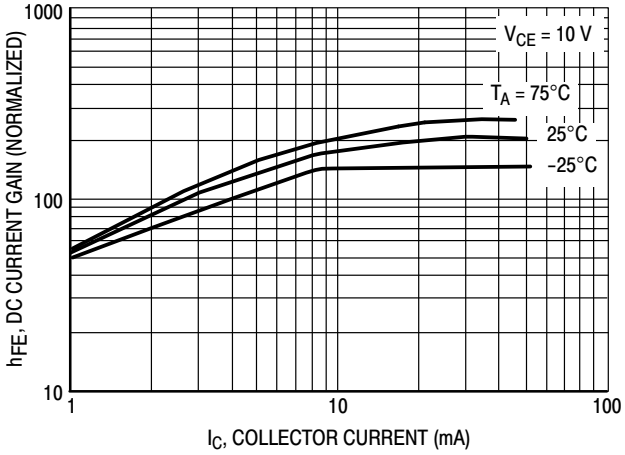


Figure 3. DC Current Gain

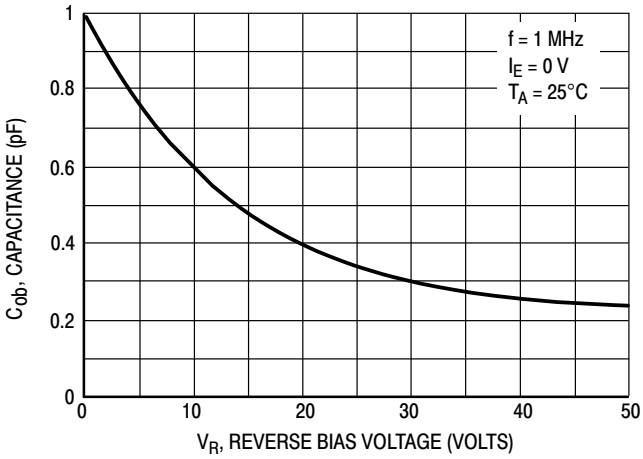


Figure 4. Output Capacitance

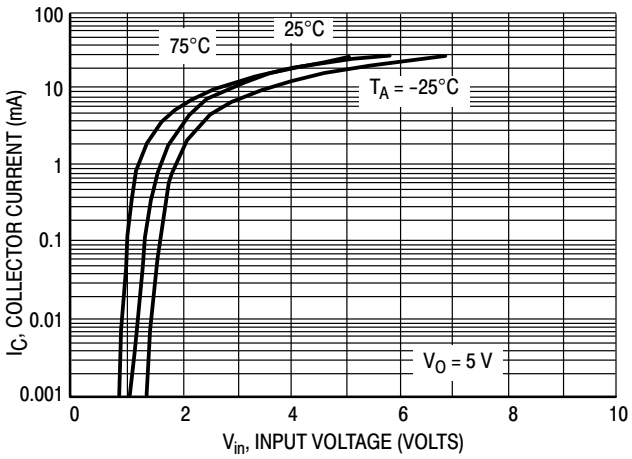


Figure 5. Output Current versus Input Voltage

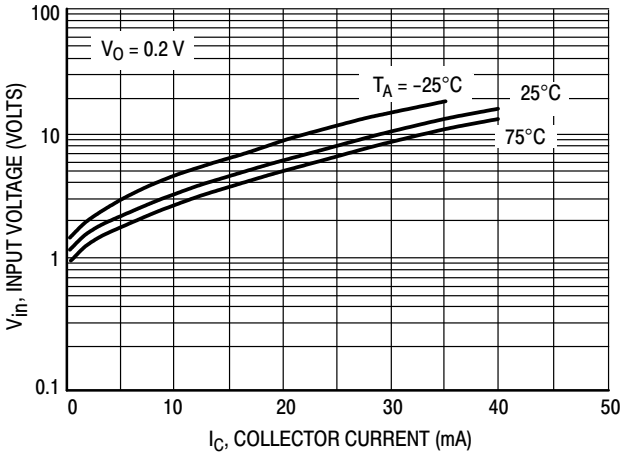


Figure 6. Input Voltage versus Output Current

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TYPICAL ELECTRICAL CHARACTERISTICS – EMG5DXV5 (continued)

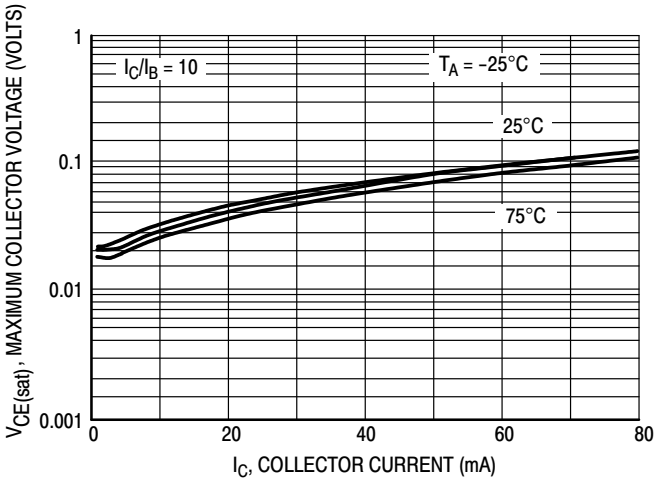


Figure 7. $V_{CE(sat)}$ versus I_C

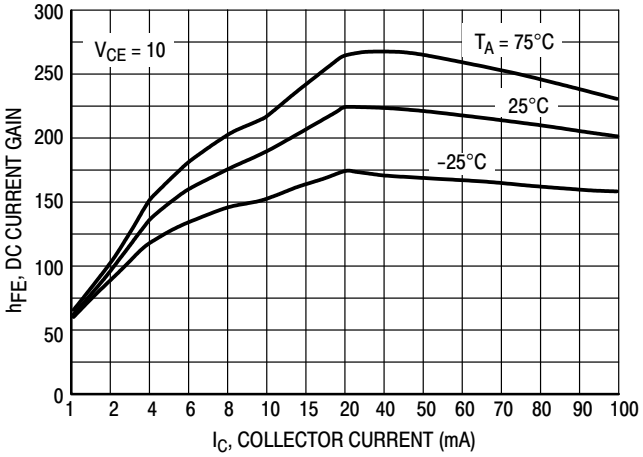


Figure 8. DC Current Gain

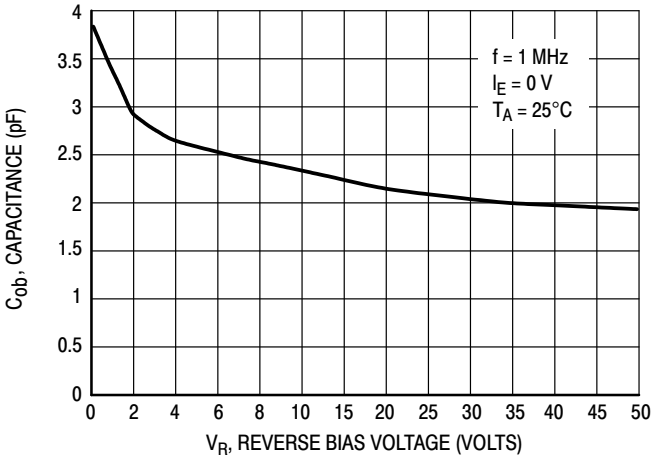


Figure 9. Output Capacitance

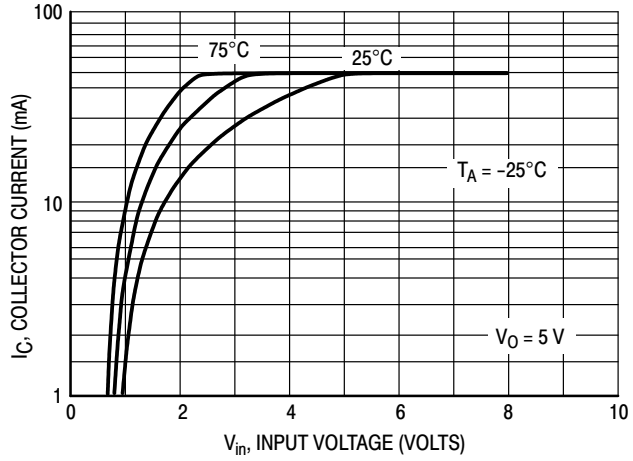


Figure 10. Output Current versus Input Voltage

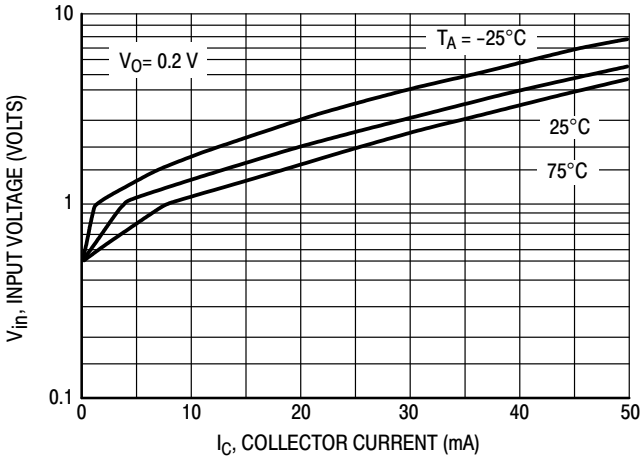


Figure 11. Input Voltage versus Output Current

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TYPICAL APPLICATIONS FOR NPN BRTS

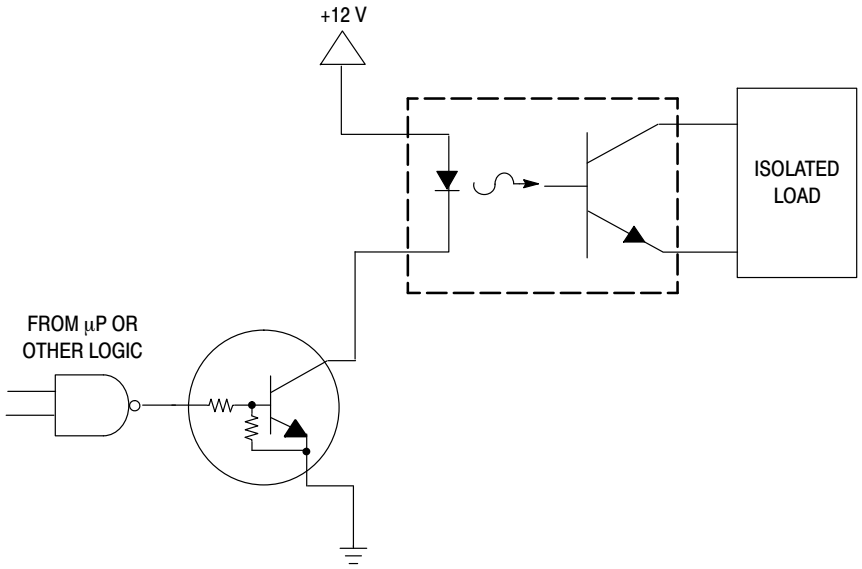


Figure 12. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

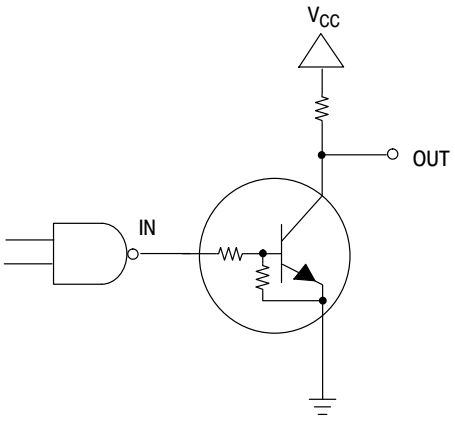


Figure 13. Open Collector Inverter: Inverts the Input Signal

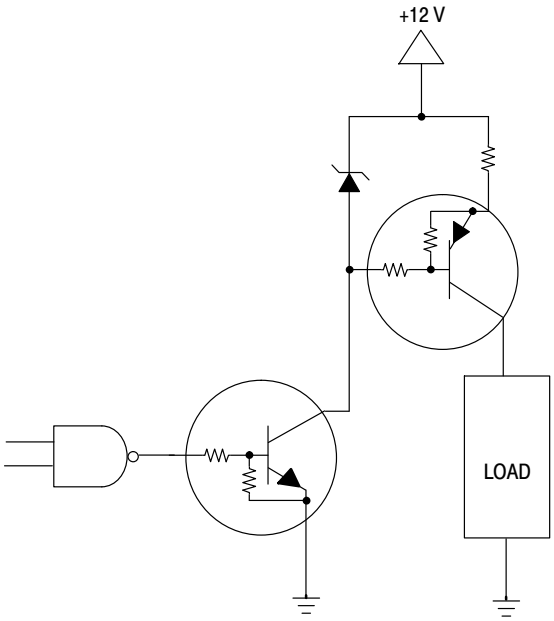


Figure 14. Inexpensive, Unregulated Current Source

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DEVICE ORDERING INFORMATION

Device	Package	Shipping†
EMG2DXV5T1G	SOT−553 (Pb−Free)	4,000 / Tape & Reel

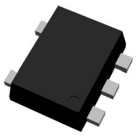
DISCONTINUED (Note 4)

EMG2DXV5T5G	SOT−553 (Pb−Free)	8,000 / Tape & Reel
EMG5DXV5T1G	SOT−553 (Pb−Free)	4,000 / Tape & Reel
EMG5DXV5T5G	SOT−553 (Pb−Free)	8,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

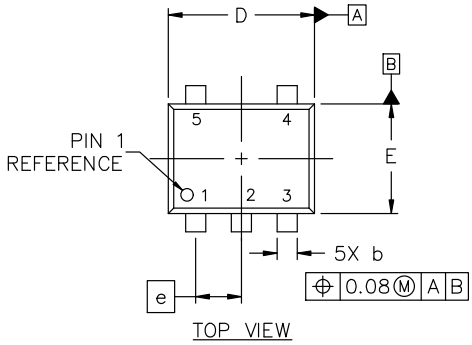
4. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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SOT−553−5 1.60x1.20x0.55, 0.50P
CASE 463B
ISSUE D

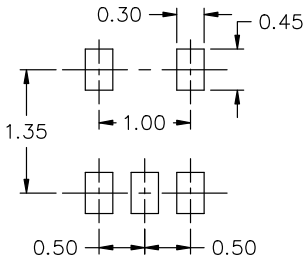
DATE 21 FEB 2024



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.55	1.60	1.65
E	1.15	1.20	1.25
e	0.50 BSC		
H	1.55	1.60	1.65
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR 1
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

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DESCRIPTION:	**SOT−553−5 1.60x1.20x0.55, 0.50P**	**PAGE 1 OF 1**

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