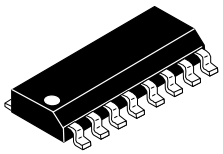
# 3-Channel Constant-Current RGB LED Driver with Individual PWM Dimming

# CAT4109, CAV4109



SOIC−16
V SUFFIX
CASE 751BG

## Description

The CAT4109/CAV4109 is a 3−channel constant−current LED driver, requiring no inductor. LED channel currents up to 175 mA are programmed independently via separate external resistors. Low output voltage operation of 0.4 V at 175 mA allows for more power efficient designs across wider supply voltage range. The three LED pins are compatible with high voltage up to 25 V supporting applications with long strings of LEDs.

Three independent control inputs PWM1, PWM2, PWM3, control respectively LED1, LED2, LED3 channels. The device also includes an output enable (OE) control pin to disable all three channels independently of the PWMx input states.

Thermal shutdown protection is incorporated in the device to disable the LED outputs whenever the die temperature exceeds 150°C.

The device is available in a 16−lead SOIC package.

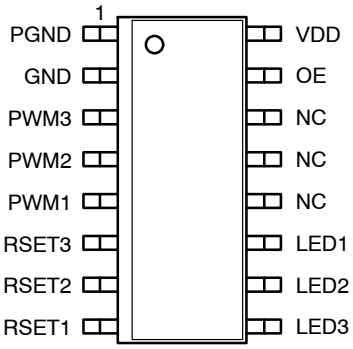
## Features

- 3 Independent Current Sinks up to 175 mA rated 25 V
- LED Current Set by External Low Power Control Resistors
- Individual PWM Control per Channel
- Low Dropout Current Source (0.4 V at 175 mA)
- Output Enable Input for Dimming
- “Zero” Current Shutdown Mode
- 3 V to 5.5 V Logic Supply
- Thermal Shutdown Protection
- 16−lead SOIC Package
- CAV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

## Application

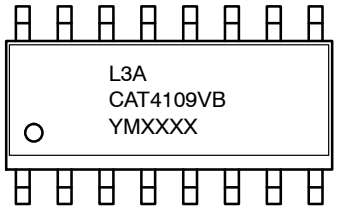
- Multi−color LED, Architectural Lighting
- LED Signs and Displays
- LCD Backlight

## PIN CONNECTIONS




(Top View)

## MARKING DIAGRAM




L = Assembly Location
3 = PB Free
A = Product Revision (Fixed as “A”)
CAT4109V = Device Code
B = Leave Blank
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXXX = Last Four Digits of Assembly Lot Number

## ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| CAT4109V−GT2 (Note 1) | SOIC−16 (Pb−Free) | 3,000/ Tape & Reel |
| CAV4109V−GT2 (Note 1) | SOIC−16 (Pb−Free) | 3,000/ Tape & Reel |

1. Lead Finish Pb−Free

© Semiconductor Components Industries, LLC, 2015

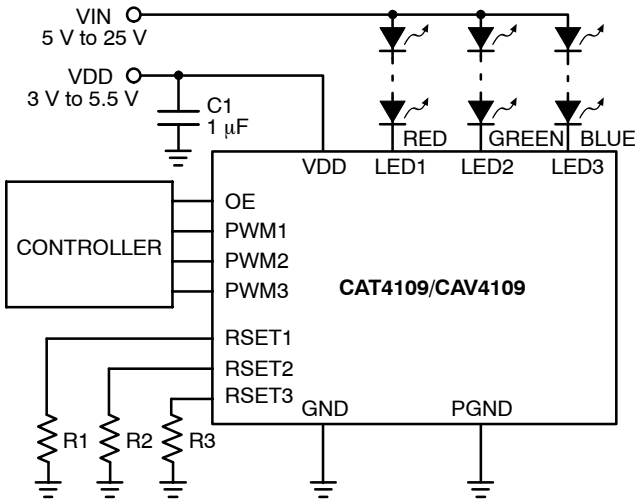



**Figure 1. Typical Application Circuit**

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter | Rating | Units |
|---|---|---|
| VDD Voltage | 6 | V |
| Input Voltage Range (OE, PWM1, PWM2, PWM3) | −0.3 V to 6 V | V |
| LED1, LED2, LED3 Voltage | 25 | V |
| DC Output Current on LED1 to LED3 | 200 | mA |
| Storage Temperature Range | −55 to +160 | °C |
| Junction Temperature Range | −40 to +150 | °C |
| Lead Soldering Temperature (10 sec.) | 300 | °C |
| **ESD RATING** | | |
| Human Body Model (Note 2)<br>LV pins (non LEDn pins # 3, 4, 5, 6, 7, 8, 15 and 16)<br>HV pins( LEDn pins #9, 10 and 11) | <br>1500<br>500 | V |
| Machine Model (Note 3)<br>LV pins (non LEDn pins # 3, 4, 5, 6, 7, 8, 15 and 16)<br>HV pins ( LEDn pins #9, 10 and 11) | <br>200<br>175 | V |
| Charged Device Model (Note 4) | 1000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JESD22−A114C
3. JESD625−A
4. JESD22−C101E

**Table 2. RECOMMENDED OPERATING CONDITIONS**

| Parameter | | Range | Units |
|---|---|---|---|
| VDD | | 3.0 to 5.5 | V |
| Voltage applied to LED1 to LED3, outputs off | | up to 25 | V |
| Voltage applied to LED1 to LED3, outputs on | | up to 6 (Note 5) | V |
| Output Current on LED1 to LED3 | | 2 to 175 | mA |
| Ambient Temperature Range | CAT4109<br>CAV4109 | −40 to +85<br>−40 to +105 | °C<br>°C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Keeping LEDx pin voltage below 6 V in operation is recommended to minimize thermal dissipation in the package.



Share Feedback
Your Opinion Matters

**Table 3. ELECTRICAL OPERATING CHARACTERISTICS** (Min and Max values are over recommended operating conditions unless specified otherwise. Typical values are at $V_{DD}$ = 5.0 V, $T_{AMB}$ = 25°C.)

| Symbol | Name | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $I_{DD1}$ | Supply Current Outputs Off | $V_{LED}$ = 5 V, $R_{SET}$ = 24.9 kΩ | | 2 | 5 | mA |
| $I_{DD2}$ | Supply Current Outputs Off | $V_{LED}$ = 5 V, $R_{SET}$ = 5.23 kΩ | | 4 | 10 | mA |
| $I_{DD3}$ | Supply Current Outputs On | $V_{LED}$ = 0.5 V, $R_{SET}$ = 24.9 kΩ | | 2 | 5 | mA |
| $I_{DD4}$ | Supply Current Outputs On | $V_{LED}$ = 0.5 V, $R_{SET}$ = 5.23 kΩ | | 4 | 10 | mA |
| $I_{SHDN}$ | Shutdown Current | $V_{OE}$ = 0 V | | | 1 | μA |
| $I_{LKG}$ | LED Output Leakage | $V_{LED}$ = 5 V, Outputs Off | −1 | | 1 | μA |
| $R_{OE}$ | OE Pull−down Resistance | | 140 | 190 | 250 | kΩ |
| $V_{OE_IH}$<br>$V_{OE_IL}$ | OE Logic High Level<br>OE Logic Low Level | | 1.3 | | <br>0.4 | V |
| $V_{PWM_IH}$<br>$V_{PWM_IL}$ | PWMx Logic High Level<br>PWMx Logic Low Level | | 0.7 x $V_{DD}$ | | <br>0.3 x $V_{DD}$ | V |
| $I_{IL}$ | Logic Input Leakage Current (PWMx) | $V_{PWMx}$ = $V_{DD}$ or GND | −5 | 0 | 5 | μA |
| $V_{RSETx}$ | RSETx Regulated Voltage | | 1.17 | 1.2 | 1.23 | V |
| $T_{SD}$ | Thermal Shutdown | | | 150 | | °C |
| $T_{HYS}$ | Thermal Hysteresis | | | 20 | | °C |
| $I_{LED}/I_{RSET}$ | RSET to LED Current Gain Ratio | 100 mA LED Current | | 400 | | |
| $V_{UVLO}$ | Undervoltage Lockout (UVLO) Threshold | | | 1.8 | | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 4. RECOMMENDED TIMING** (Min and Max values are over recommended operating conditions unless specified otherwise. Typical values are at $V_{DD}$ = 5.0 V, $T_{AMB}$ = 25°C.)

| Symbol | Name | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PS}$ | Turn−On time, OE rising to $I_{LED}$ from Shutdown | $I_{LED}$ = 100 mA | | 1.4 | | μs |
| $t_{P1}$ | Turn−On time, OE or PWMx rising to $I_{LED}$ | $I_{LED}$ = 100 mA | | 600 | | ns |
| $t_{P2}$ | Turn−Off time, OE or PWMx falling to $I_{LED}$ | $I_{LED}$ = 100 mA | | 300 | | ns |
| $t_R$ | LED rise time | $I_{LED}$ = 100 mA | | 300 | | ns |
| $t_F$ | LED fall time | $I_{LED}$ = 100 mA | | 300 | | ns |
| $t_{LO}$ | OE low time | | 1 | | | μs |
| $t_{HI}$ | OE high time | | 5 | | | μs |
| $t_{PWRDWN}$ | OE low time to shutdown delay | | | 4 | 8 | ms |



Share Feedback
Your Opinion Matters

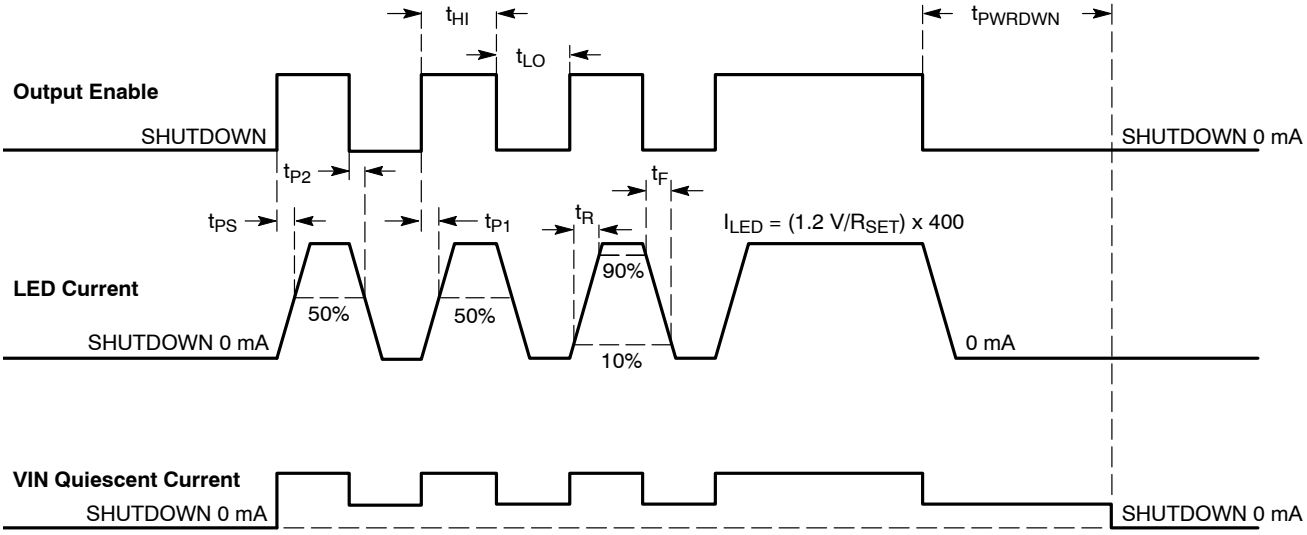



**Figure 2. CAT4109/CAV4109 OE Timing**

### OE Operation

The Output Enable (OE) pin has two primary functions. When the OE input goes from high to low, all three LED channels are turned off. If OE remains low for longer than $t_{PWRDWN}$, the device enters shutdown mode drawing "zero current" from the supply.

The OE input can be used to adjust the contrast of the RGB LED by applying an external PWM signal. The device has a very fast turn−on time (from OE rising to LED on) allowing "instant on" when dimming LEDs.

When applying PWM signals to the three PWMx inputs and using the OE pin for dimming, the OE PWM frequency should be much lower to preserve the color mixing.

Accurate linear dimming on OE is compatible with PWM frequencies from 100 Hz to 5 kHz for PWM duty cycle down to 1%. PWM frequencies up to 50 kHz can be supported for duty cycles greater than 10%.

When performing a combination of low frequencies and small duty cycles, the device may enter shutdown mode. This has no effect on the dimming accuracy, because the turn−on time $t_{PS}$ is very short, in the range of 1 μs.

To ensure that PWM pulses are recognized, pulse width low time $t_{LO}$ should be longer than 1 μs. The driver enters a "zero current" shutdown mode after a 4 ms delay (typical) when OE is held low.



Share Feedback
Your Opinion Matters

## TYPICAL PERFORMANCE CHARACTERISTICS

($V_{IN}$ = 5 V, $V_{DD}$ = 5 V, C1 = 1 μF, $T_{AMB}$ = 25°C unless otherwise specified.)

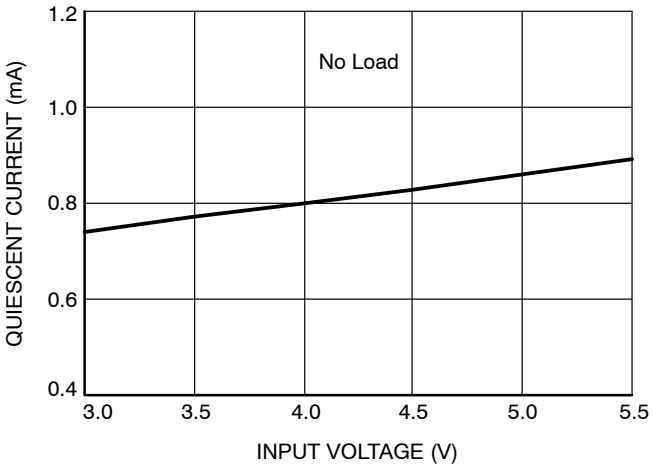



**Figure 3. Quiescent Current vs. Input Voltage ($I_{LED}$ = 0 mA)**

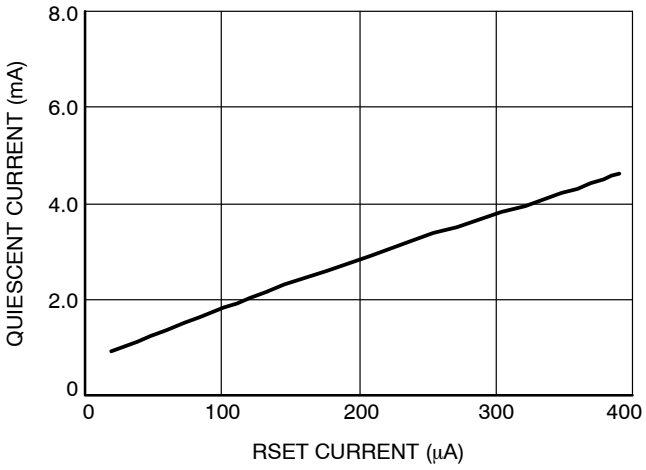



**Figure 4. Quiescent Current vs. RSET Current**

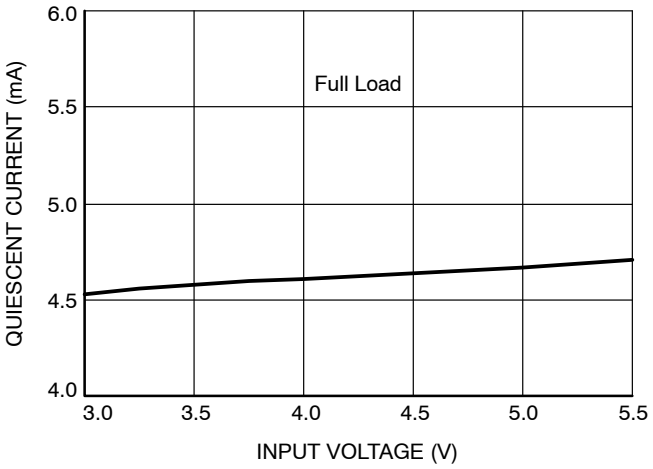



**Figure 5. Quiescent Current vs. Input Voltage ($I_{LED}$ = 175 mA)**

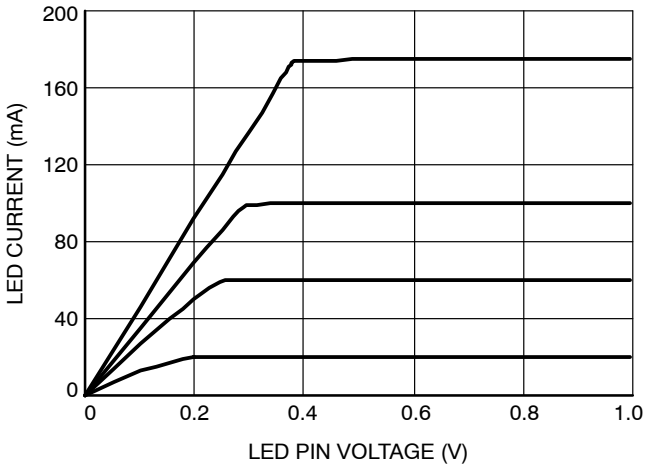



**Figure 6. LED Current vs. LED Pin Voltage**

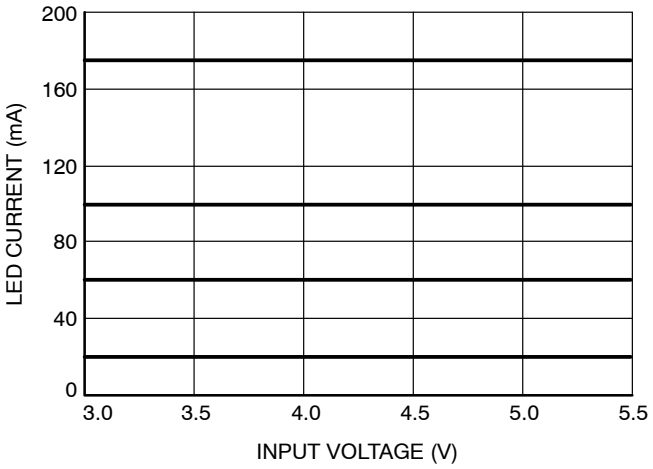



**Figure 7. LED Current Change vs. Input Voltage**

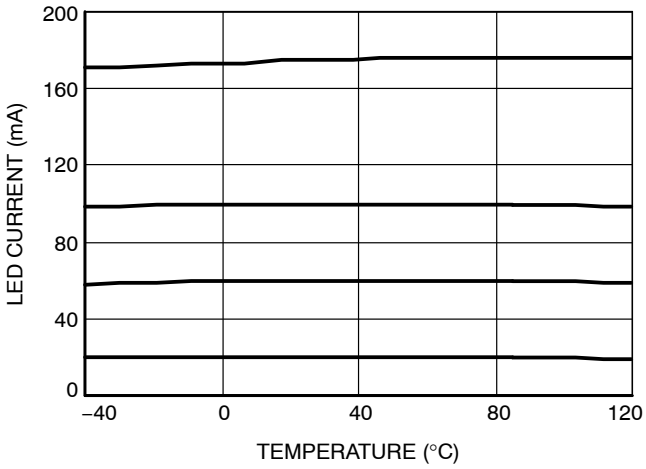



**Figure 8. LED Current Change vs. Temperature**



Share Feedback
Your Opinion Matters

## TYPICAL PERFORMANCE CHARACTERISTICS

($V_{IN}$ = 5 V, $V_{DD}$ = 5 V, C1 = 1 μF, $T_{AMB}$ = 25°C unless otherwise specified.)

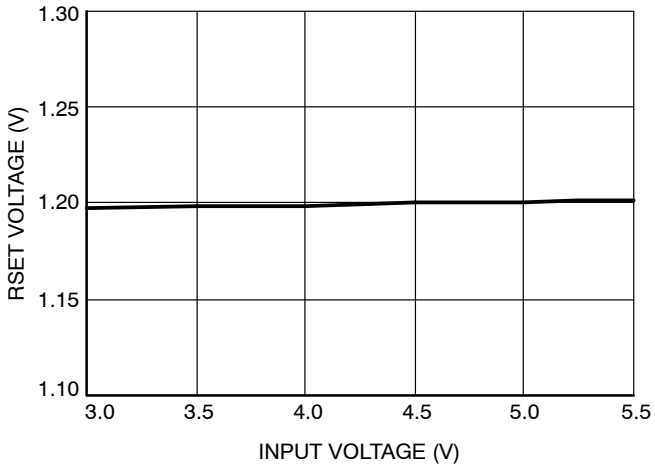



**Figure 9. RSET Pin Voltage vs. Input Voltage**

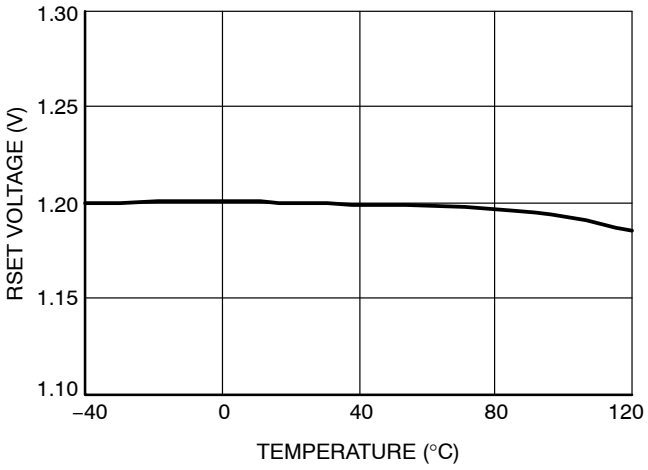



**Figure 10. RSET Pin Voltage vs. Temperature**

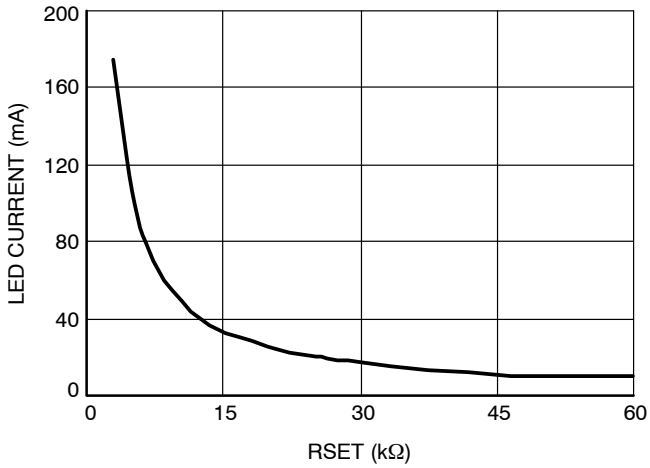



**Figure 11. LED Current vs. RSET Resistor**

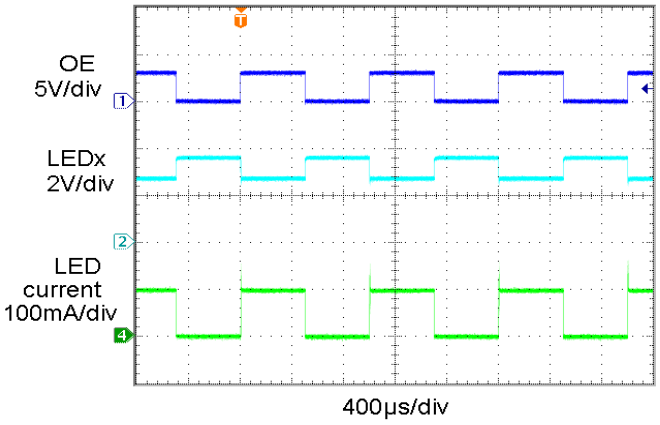



**Figure 12. OE Transient Response at 1 kHz**

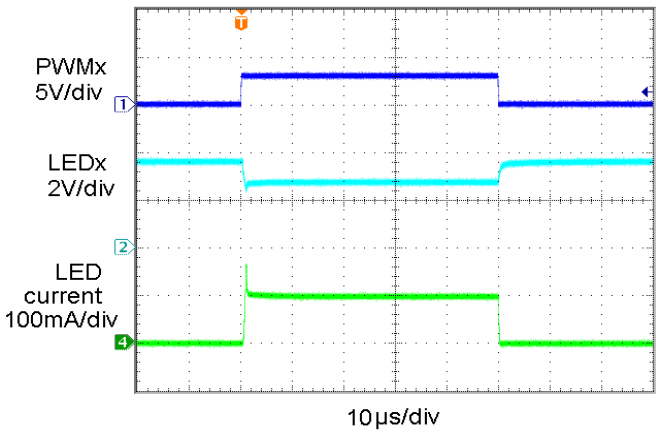



**Figure 13. PWMx Transient Response**



Share Feedback
Your Opinion Matters

**Table 5. PIN DESCRIPTIONS**

| Name | Pin Number | Function |
|---|---|---|
| PGND | 1 | Power Ground. |
| GND | 2 | Ground Reference. |
| PWM3 | 3 | PWM control input for LED3 |
| PWM2 | 4 | PWM control input for LED2 |
| PWM1 | 5 | PWM control input for LED1 |
| RSET3 | 6 | LED current set pin for LED3 |
| RSET2 | 7 | LED current set pin for LED2 |
| RSET1 | 8 | LED current set pin for LED1 |
| LED3 | 9 | LED channel 3 cathode terminal |
| LED2 | 10 | LED channel 2 cathode terminal |
| LED1 | 11 | LED channel 1 cathode terminal |
| NC | 12 | Not connected inside package |
| NC | 13 | Not connected inside package |
| NC | 14 | Not connected inside package |
| OE | 15 | Output Enable input pin |
| VDD | 16 | Device Supply pin |

## Pin Function

**PGND** is the power ground reference pin for the device. This pin must be connected to the GND pin and to the ground plane on the PCB.

**GND** is the ground reference pin for the entire device. This pin must be connected to the ground plane on the PCB.

**PWM1** to **PWM3** are the control inputs respectively for LED1, LED2 and LED3 channels. When PWMx are low, the associated LED channels are turned off. When PWMx are high, the corresponding channels are turned on, assuming the OE input is also high. PWMx pins can not be left open and must be set either to logic high or low.

**RSET1 to RSET3** are the LED current set inputs. The current pulled out of these pins will be mirrored in the corresponding LED channel with a gain of 400.

**LED1 to LED3** are the LED current sink inputs. These pins are connected to the bottom cathodes of the LED strings. The current sinks bias the LEDs with a current equal to 400 times the corresponding RSETx pin current. For the LED sink to operate correctly the voltage on the LED pin must be above 0.4 V. Each LED channel can withstand voltages up to 25 V.

**OE** is the output enable input. When high, all LED channels are enabled according to the state of their corresponding PWMx control inputs. When low, all LED channels are turned off. This pin can be used to turn all the LEDs off independently of the state of the PWMx inputs. If the OE stays low for a duration longer than $t_{PWRDWN}$, the device enters shutdown mode.

**VDD** is the positive supply pin voltage for the entire device. A small 1 μF bypass ceramic capacitor is recommended between VDD pin and ground near the device.



Share Feedback
Your Opinion Matters

## BLOCK Diagram

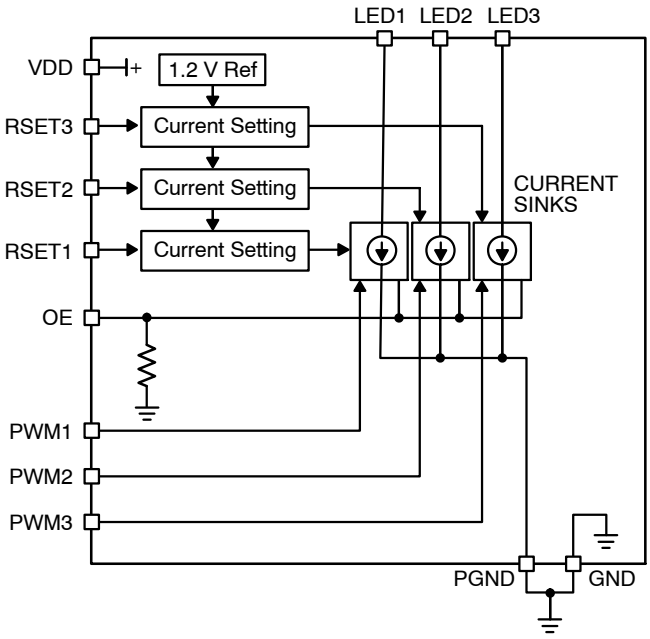



**Figure 14. CAT4109/CAV4109 Functional Block Diagram**

### Basic Operation

The CAT4109/CAV4109 uses 3 independent current sinks to accurately regulate the current in each LED channel to 400 times the current sink from the corresponding RSET pin. Each of the resistors tied to the RSET1, RSET2, RSET3 pins set the current respectively in the LED1, LED2, and LED3 channels. Table 6 shows standard resistor values for RSET and the corresponding LED current.

**Table 6. RSET RESISTOR SETTINGS**

| LED Current [mA] | RSET [kΩ] |
|---|---|
| 20 | 24.9 |
| 60 | 8.45 |
| 100 | 5.23 |
| 175 | 3.01 |

Tight current regulation for all channels is possible over a wide range of input and LED voltages due to independent current sensing circuitry on each channel. The LED channels have a low dropout of 0.4 V or less for all current ranges and supply voltages. This helps improve heat dissipation and efficiency.

Upon power−up, an under−voltage lockout circuit sets all outputs to off. Once the VDD supply voltage is greater than the under−voltage lockout threshold, the device channel can be turned on. The on/off state of each channel LED1, LED2 and LED3 is independently controlled respectively by PWM1, PWM2, PWM3. When a PWMx is high, the associated LEDx channel is turned on.



Share Feedback
Your Opinion Matters

## Application Information

### Power Dissipation

The power dissipation ($P_D$) of the CAT4109/CAV4109 can be calculated as follows:

$$P_D = (V_{DD} \times I_{DD}) + \Sigma(V_{LEDN} \times I_{LEDN})$$

where $V_{LEDN}$ is the voltage at the LED pin, and $I_{LEDN}$ is the associated LED current. Combinations of high $V_{LED}$ voltage or high ambient temperature can cause the CAT4109/CAV4109 to enter thermal shutdown. In applications where $V_{LEDN}$ is high, a resistor can be inserted in series with the LED string to lower $P_D$.

Thermal dissipation of the junction heat consists primarily of two paths in series. The first path is the junction to the case ($\theta_{JC}$) thermal resistance which is defined by the package style, and the second path is the case to ambient ($\theta_{CA}$) thermal resistance, which is dependent on board layout. The overall junction to ambient ($\theta_{JA}$) thermal resistance is equal to:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

For a given package style and board layout, the operating junction temperature $T_J$ is a function of the power dissipation $P_D$, and the ambient temperature, resulting in the following equation:

$$T_J = T_{AMB} + P_D (\theta_{JC} + \theta_{CA}) = T_{AMB} + P_D \theta_{JA}$$

When mounted on a double−sided printed circuit board with two square inches of copper allocated for “heat spreading”, the resulting $\theta_{JA}$ is about 74°C/W.

For example, at 60°C ambient temperature, the maximum power dissipation is calculated as follow:

$$P_{Dmax} = \frac{(T_{Jmax} - T_{AMB})}{\theta_{JA}} = \frac{(150 - 60)}{74} = 1.2\ W$$

### Recommended Layout

Bypass capacitor C1 should be placed as close to the IC as possible. RSET resistors should be directly connected to the GND pin of the device. For better thermal dissipation, multiple via can be used to connect the GND pad to a large ground plane. It is also recommended to use large pads and traces on the PCB wherever possible to spread out the heat. The LEDs for this layout are driven from a separate supply (VLED+), but they can also be driven from the same supply connected to VDD.

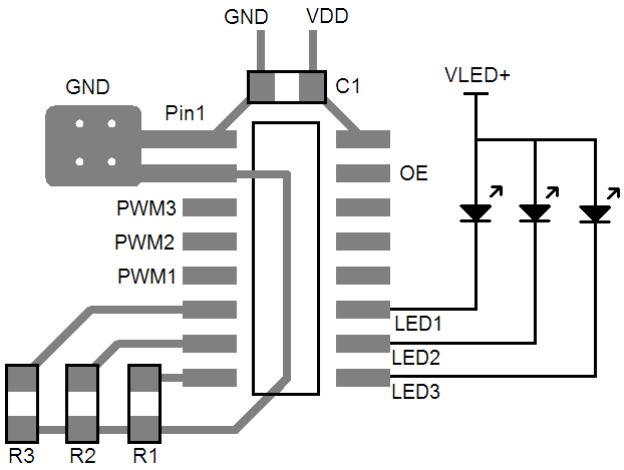


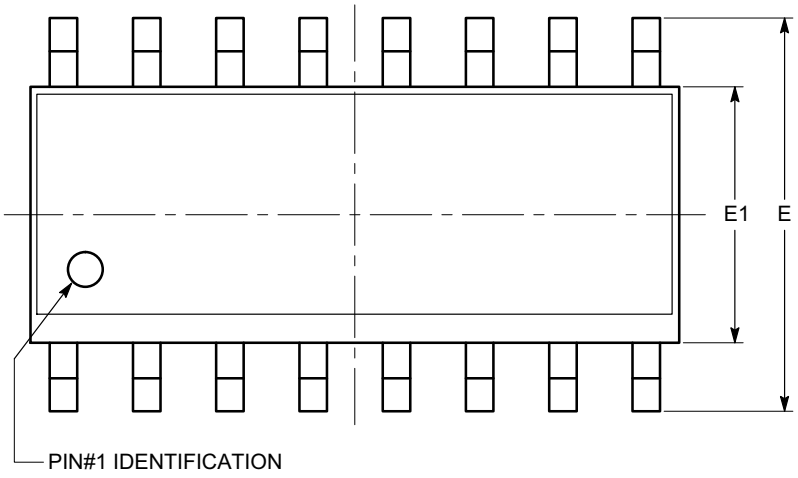

**Figure 15. Recommended Layout**



Share Feedback
Your Opinion Matters

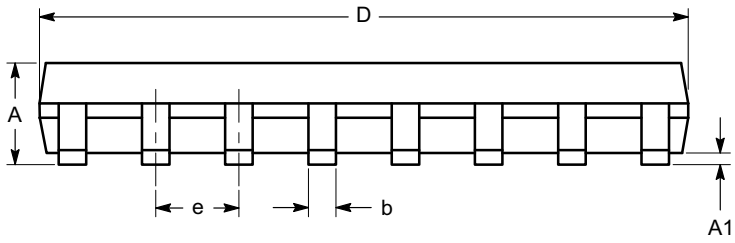
**SOIC−16, 150 mils**
CASE 751BG
ISSUE O

DATE 19 DEC 2008

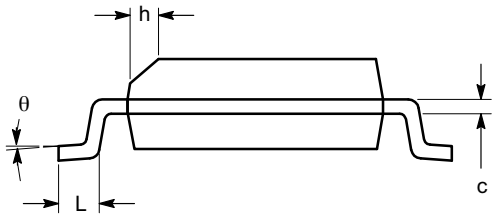



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 9.80 | 9.90 | 10.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |




**SIDE VIEW**




**END VIEW**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98AON34275E** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **SOIC−16, 150 mils** | | **PAGE 1 OF 1** |

**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales