CAN/CAN-FD Bus Protector

Low Capacitance ESD Protection Diode for CAN/CAN-FD Bus

ESDONCAN1, SESDONCAN1

The S/ESDONCAN1 has been designed to protect the CAN transceiver from ESD and other harmful transient voltage events. This device provides bidirectional protection for each data line with a single compact SOT-23 package, giving the system designer a low cost option for improving system reliability and meeting stringent EMI requirements.

Features

- 150 W Peak Power Dissipation per Line (8 x 20 μsec Waveform)
- Diode Capacitance Matching
- Low Reverse Leakage Current (< 100 nA)
- Low Capacitance High-Speed FlexRay Data Rates
- IEC Compatibility: – IEC 61000-4-2 (ESD): Level 4
  – IEC 61000-4-4 (EFT): 50 A – 5/50 ns
  – IEC 61000-4-5 (Lighting) 3.0 A (8/20 μs)
- ISO 7637-1, Nonrepetitive EMI Surge Pulse 2, 8.0 A (1/50 μs)
- ISO 7637-3, (EFT) EMI Surge Pulses, 50 A (5/50 ns)
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

Typical Applications

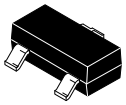
- Industrial
  - Smart Distribution Systems (SDS)
  - DeviceNet
- Automotive
  - Controlled Area Network – CAN 2.1 / CAN FD
  - Low and High Speed CAN

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

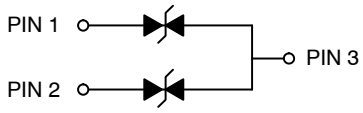
Symbol	Rating	Max	Unit
PPK	Peak Power Dissipation, 8x20 μs Double Exponential Waveform (Note 1)	150	W
T_J, T_{stg}	Junction and Storage Temperature Range	–55 to +150	°C
T_L	Lead Solder Temperature (10 s)	260	°C
ESD	Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Contact IEC 61000-4-2 Air ISO 10605 Contact (330 pF / 330 Ω) ISO 10605 Contact (330 pF / 2 kΩ) ISO 10605 Contact (150 pF / 2 kΩ)	±8 ±0.4 ±23 ±21 ±30 ±30 ±30	kV
I_{PP}	Maximum Peak Pulse Current, 8/20 μs Waveforms (Figure 4)	3.0	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Non-repetitive current pulse per Figure 1.

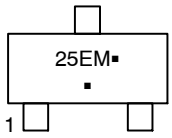
SOT-23
DUAL BIDIRECTIONAL VOLTAGE SUPPRESSOR
150 W PEAK POWER



SOT-23
CASE 318
STYLE 27



MARKING DIAGRAM



25E = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
ESDONCAN1LT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
SESDONCAN1LT1G*		
ESDONCAN1LT3G		10000 / Tape & Reel
SESDONCAN1LT3G*		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

* S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

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ELECTRICAL CHARACTERISTICS

(T_A = 25 °C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of data sheet parameters.

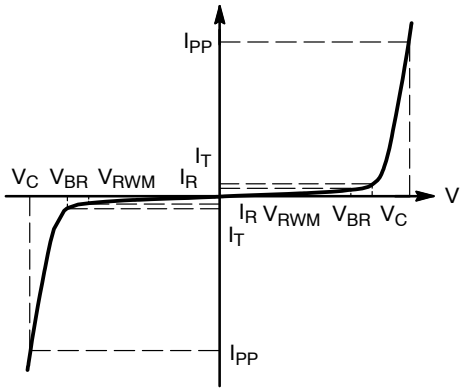


Figure 1. Bi-Directional

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	(Note 2)	24			V
V_{BR}	Breakdown Voltage	I_T = 1 mA (Note 3)	26.2		32	V
I_R	Reverse Leakage Current	V_{RWM} = 24 V		15	100	nA
V_C	Clamping Voltage TLP (See Figures 12−13) (Note 3)	ITLP = 4 A ITLP = 8 A ITLP = 16 A ITLP = 20 A		42 44 57 67		V
V_C	Clamping Voltage 8/20 s Waveform (See Figures 6−7)	IPP = 1 A IPP = 3 A		33.4 44	36.6 50	V
C_J	Capacitance	V_R = 0 V, f = 1 MHz (Line to GND)			10	pF
ΔC	Diode Capacitance Matching	V_R = 0 V, 5 MHz (Note 5)		0.26	2	%
I_L	Insertion Loss	f = 1 GHz		12.3		dB
		f = 5 GHz		1		dB
R_L	Return Loss	f = 1 GHz		1.54		dB
		,f = 5 GHz		17		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
3. V_{BR} is measured at pulse test current I_T.
4. Pulse waveform per Figure 1.
5. ΔC is the percentage difference between C_J of lines 1 and 2 measured according to the test conditions given in the electrical characteristics table.

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TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

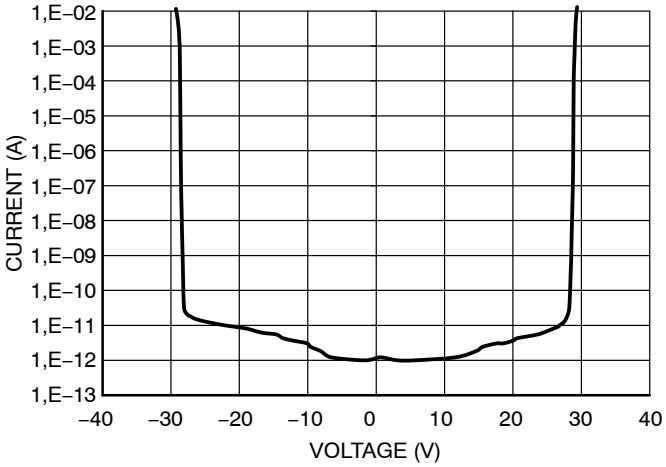


Figure 2. IV Characteristics

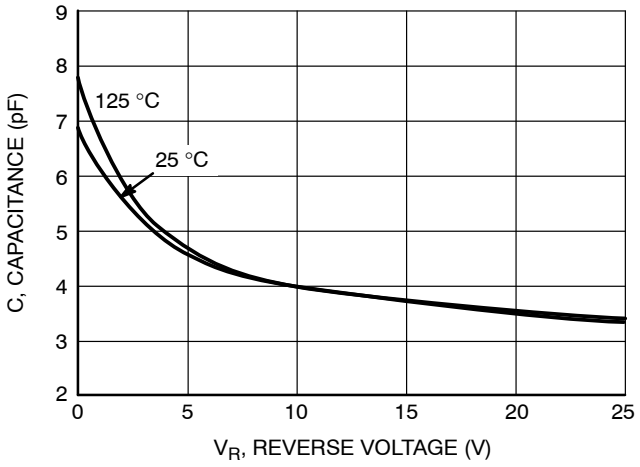


Figure 3. CV Characteristics

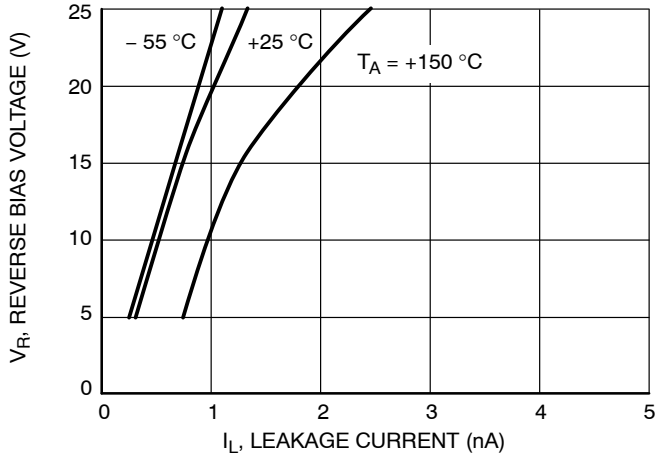


Figure 4. I_R vs. Temperature Characteristics

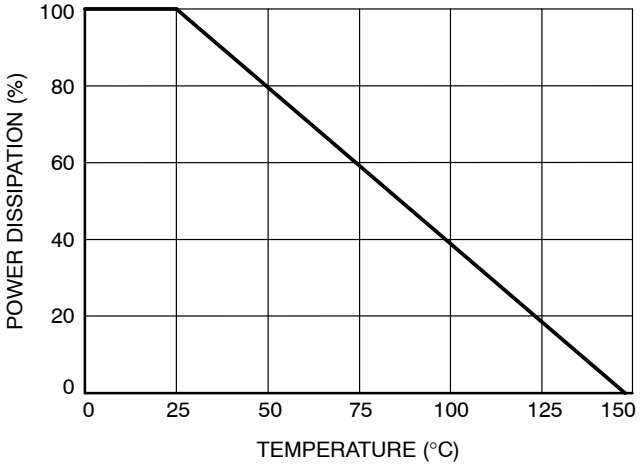


Figure 5. Steady State Power Derating

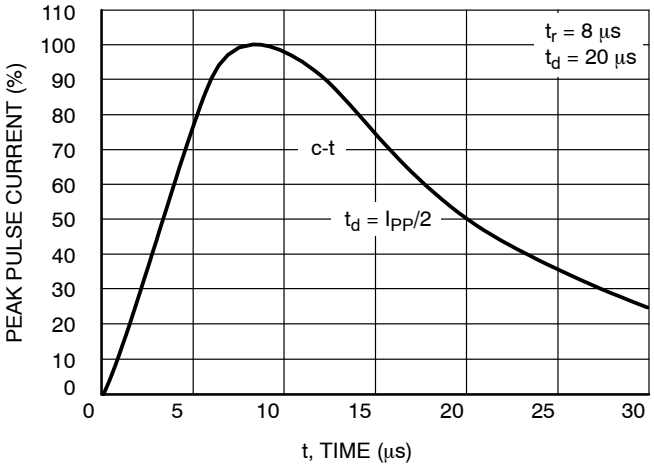


Figure 6. Pulse Waveform (8/20 μs)

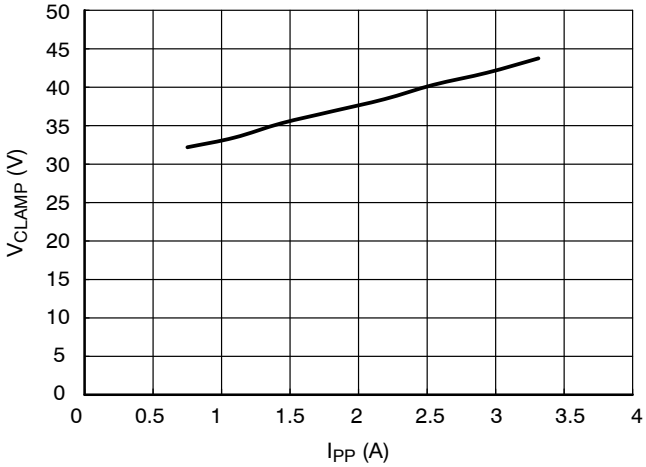


Figure 7. Clamping Voltage vs. Peak Pulse Current (8/20 μs)

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TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

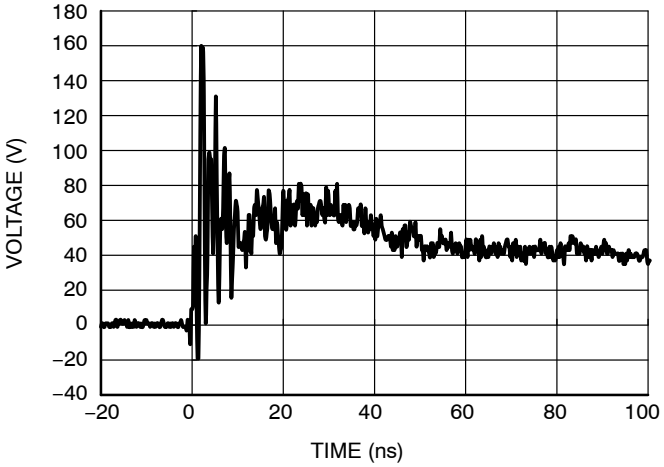


Figure 8. IEC61000-4-2 +8 kV Contact

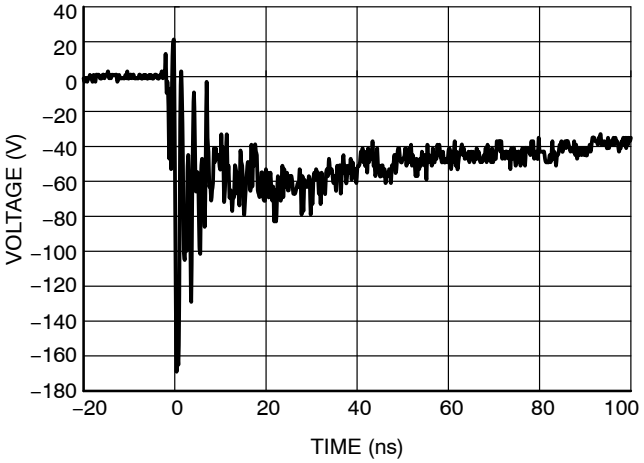


Figure 9. IEC61000-4-2 −8 kV Contact

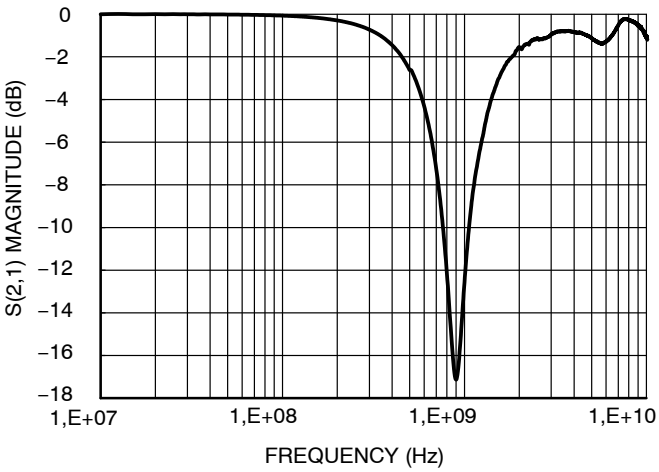


Figure 10. Typical Insertion Loss

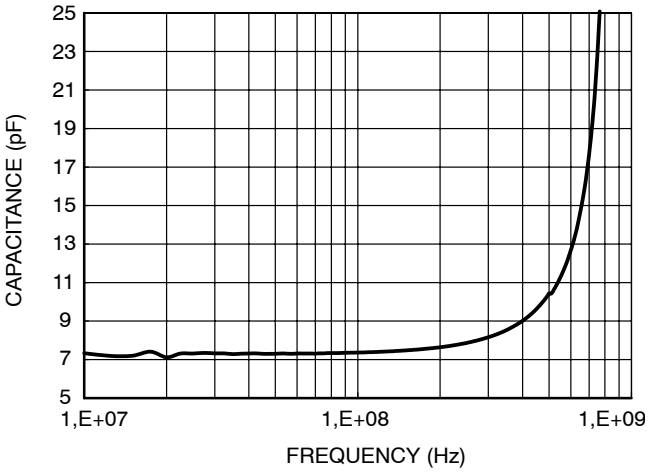


Figure 11. Typical Capacitance vs. Frequency

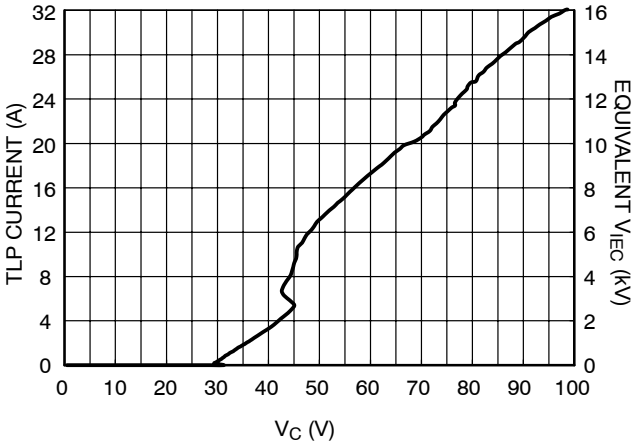


Figure 12. Positive TLP IV Curve

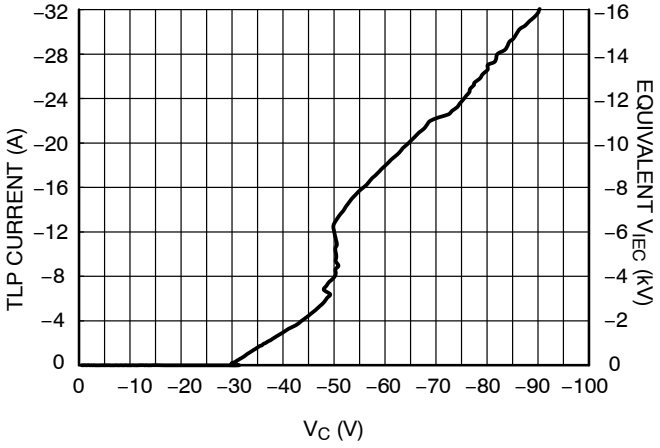


Figure 13. Negative TLP IV Curve

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APPLICATIONS

Background

The Controller Area Network (CAN) is a serial communication protocol designed for providing reliable high speed data transmission in harsh environments. Surge protection diodes provide a low cost solution to conducted and radiated Electromagnetic Interference (EMI) and Electrostatic Discharge (ESD) noise problems. The noise immunity level and reliability of CAN transceivers can be easily increased by adding external surge protection diodes to prevent transient voltage failures. The ESDONCAN1 provides a surge protection solution for CAN data communication lines. The ESDONCAN1 is a low capacitance dual bidirectional surge protection device in a compact SOT-23 package especially suitable for CAN2.1 (CAN-FD). This device is based on Zener technology that optimizes the active area of a PN junction to provide robust protection against transient EMI surge voltage and ESD. The ESDONCAN1 has been tested to EMI and ESD levels that exceed the specifications of popular high speed CAN networks.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how creates these screenshots and how to interpret them please refer to AND8307/D.

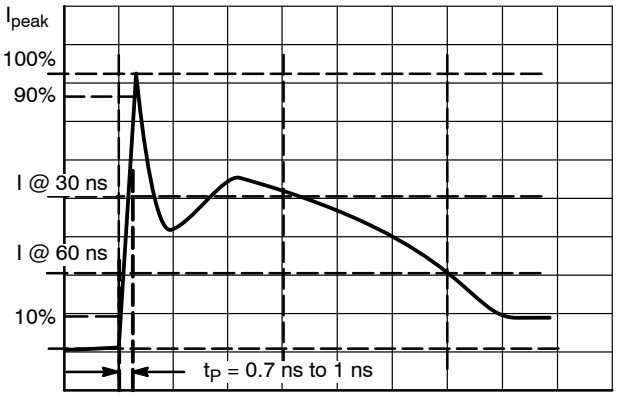


Figure 14. IEC61000-4-2 Current Waveform

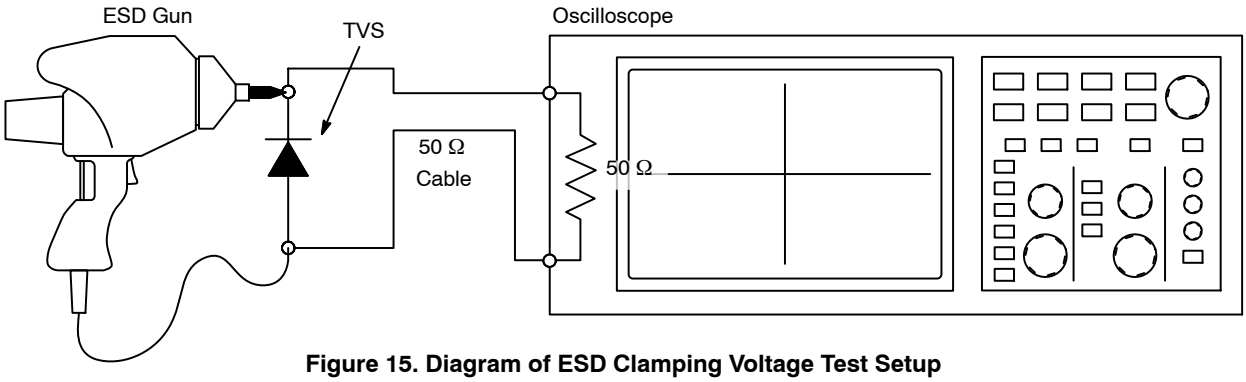


Figure 15. Diagram of ESD Clamping Voltage Test Setup

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Transmission Line Pulse (TLP) Measurement

TLP provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 16. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 17 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

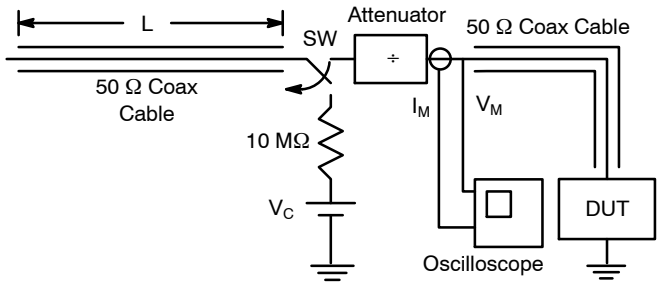


Figure 16. Basic TLP System

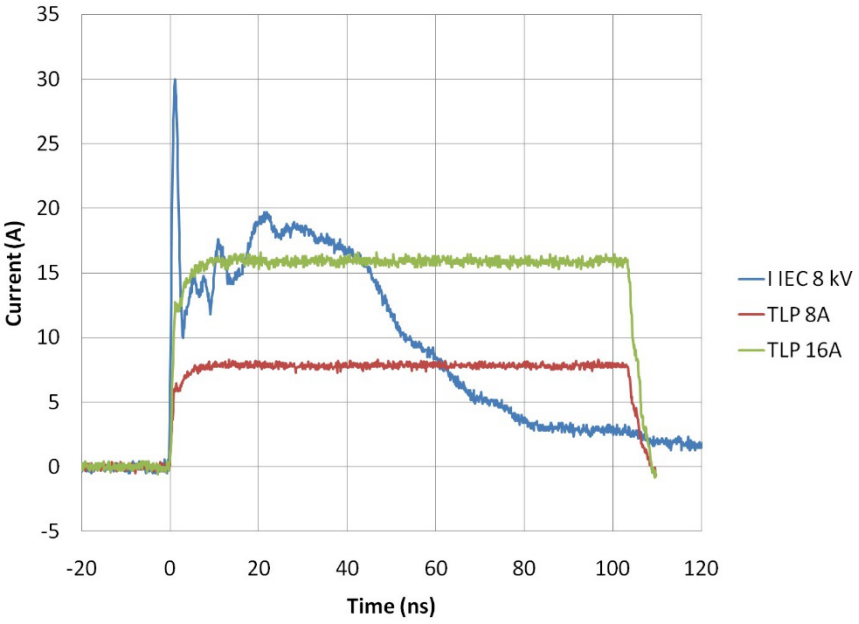


Figure 17. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

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DeviceNet is a trademark of Rockwell Automation.

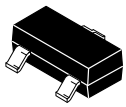
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REVISION HISTORY

Revision	Description of Changes	Date
4	Revision to update electrical characteristics data and add new characterization plots.	5/7/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

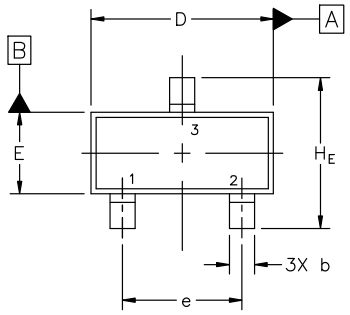
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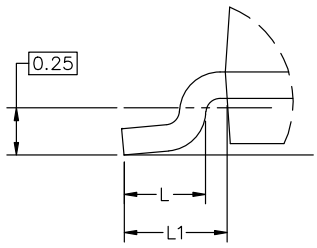
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SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

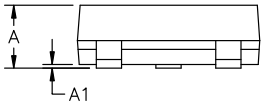
DATE 14 AUG 2024



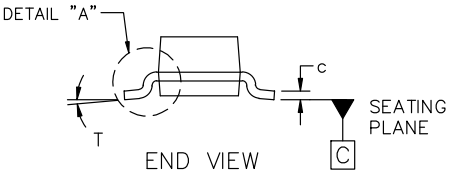
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

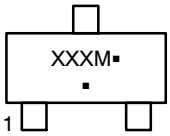


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

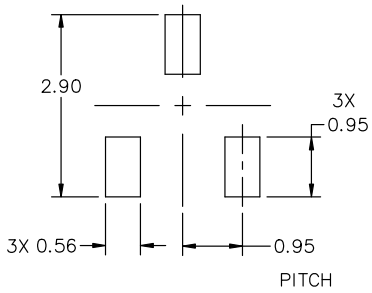
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**		**PAGE 1 OF 2**

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SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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