LDO Regulator - Ultra-Low Quiescent Current, I_Q 13 μA, Ultra-Low Noise
500 mA

NCV8705

The NCV8705 is a low noise, low power consumption and low dropout Linear Voltage Regulator. With its excellent noise and PSRR specifications, the device is ideal for use in products utilizing RF receivers, imaging sensors, audio processors or any component requiring an extremely clean power supply. The NCV8705 uses an innovative Adaptive Ground Current circuit to ensure ultra low ground current during light load conditions.

Features

- Operating Input Voltage Range: 2.5 V to 5.5 V
- Available – Fixed Voltage Option: 0.8 V to 3.5 V
  Available – Adjustable Voltage Option: 0.8 V to 5.5 V−V_{DROP}
- Reference Voltage 0.8 V
- Ultra−Low Quiescent Current of Typ. 13 μA
- Ultra−Low Noise: 12 μV_{RMS} from 100 Hz to 100 kHz
- Very Low Dropout: 230 mV Typical at 500 mA
- ±2% Accuracy Over Load/Line/Temperature
- High PSRR: 71 dB at 1 kHz
- Internal Soft−Start to Limit the Turn−On Inrush Current
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Active Output Discharge for Fast Turn−Off
- Wettable Flank Package Option Available
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

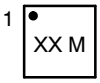
Typical Applicaitons

- ADAS, Infotainment & Cluster, and Telematics
- General Purpose Automotive & Industrial
- Building & Factory Automation, Smart Meters

MARKING DIAGRAM



WDFN6, 2x2
CASE 511BR



XX = Specific Device Code
M = Date Code



DFN8, 3x3
CASE 506DB



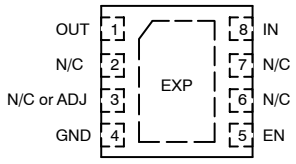


DFNW8, 3x3
CASE 507AD

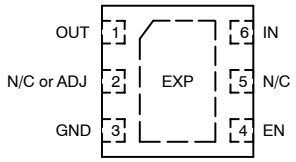


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



DFN8/DFNW8 3x3 mm
(Top View)



WDFN6 2x2 mm
(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 20 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 20.

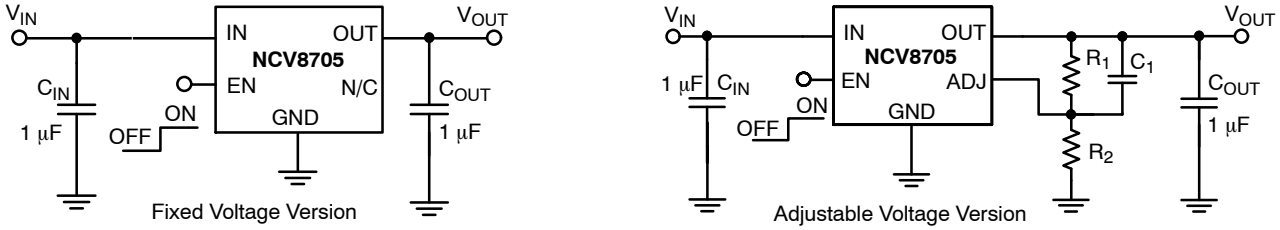


Figure 1. Typical Application Schematic

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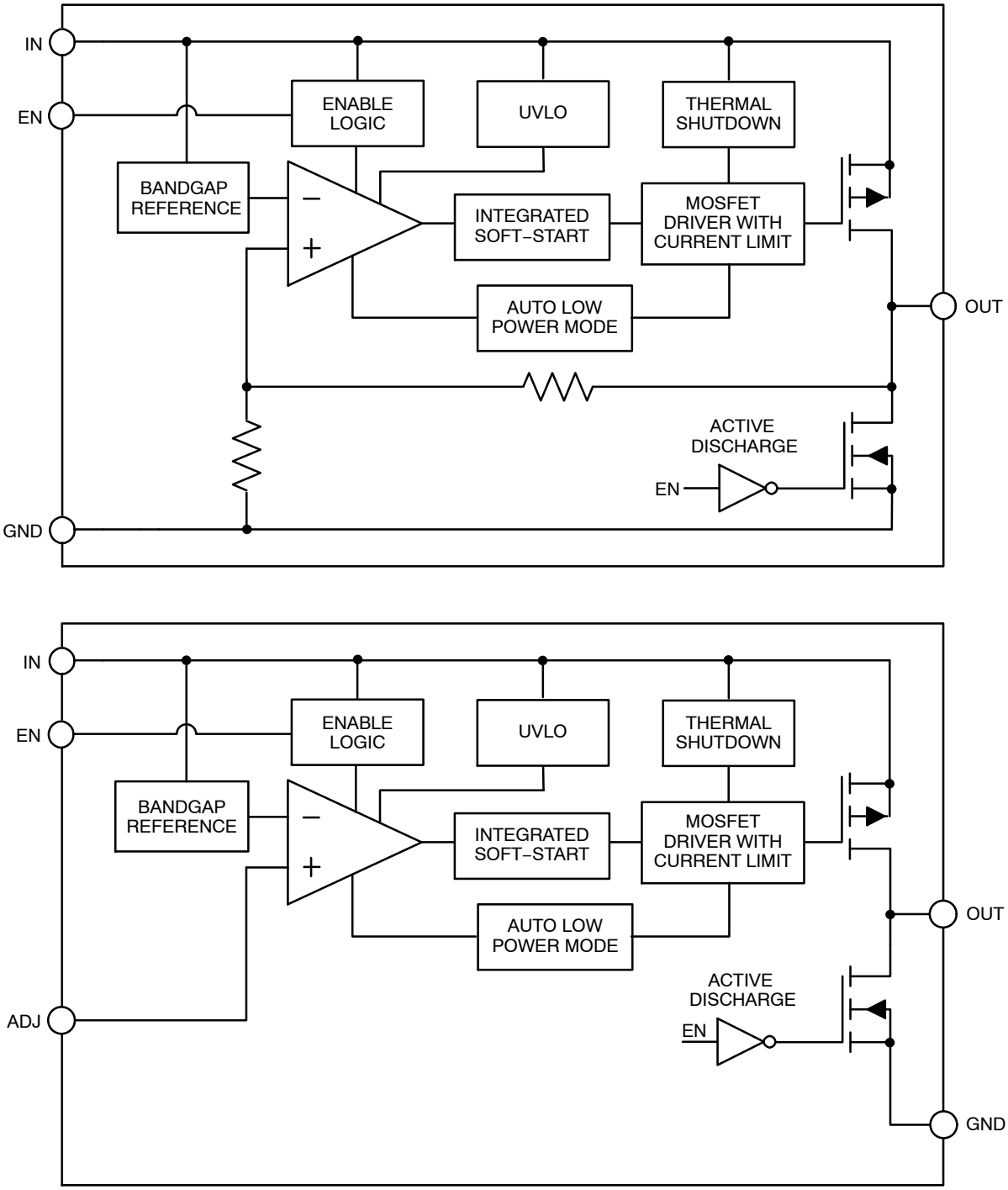


Figure 2. Simplified Schematic Block Diagrams

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Table 1. PIN FUNCTION DESCRIPTION

Pin Name	Pin No. – Fixed DFN8/DFNW8	Pin No. – Adjustable DFN8/DFNW8	Pin No. – Fixed WDFN6	Pin No. – Adjustable WDFN6	Description
OUT	1	1	1	1	Regulated output voltage pin. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
GND	4	4	3	3	Power supply ground. Expose pad must be tied with GND pin. Soldered to the copper plane allows for effective heat dissipation.
EN	5	5	4	4	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
IN	8	8	6	6	Input pin. A small capacitor is needed from this pin to ground to assure stability.
ADJ	–	3	–	2	Feedback pin for set−up output voltage. Use resistor divider for voltage selection.
N/C	2, 3, 6, 7	2, 6, 7	2, 5	5	Not connected. This pin can be tied to ground to improve thermal dissipation.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6 V	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V	V
Enable Input	V_{EN}	−0.3 V to V_{IN} + 0.3 V	V
Adjustable Input	V_{ADJ}	−0.3 V to V_{IN} + 0.3 V	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	125	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN6 2x2 mm Thermal Resistance, Junction−to−Air Thermal Resistance Parameter, Junction−to−Board	 θ_{JA} Ψ_{JB}	 116.5 30	°C/W
Thermal Characteristics, DFN8 3x3 mm / DFNW8 3x3 mm Thermal Resistance, Junction−to−Air Thermal Resistance Parameter, Junction−to−Board	 θ_{JA} Ψ_{JB}	 92.6 35.1	°C/W

3. Single component mounted on 1 oz, FR 4 PCB with 645 mm^2 Cu area.

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Table 4. ELECTRICAL CHARACTERISTICS
$-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 0.5$ V or 2.5 V, whichever is greater; V_{EN} = 0.9 V, I_{OUT} = 10 mA, $C_{IN} = C_{OUT}$ = 1 μF unless otherwise noted. Typical values are at T_J = +25°C. (Note 4)

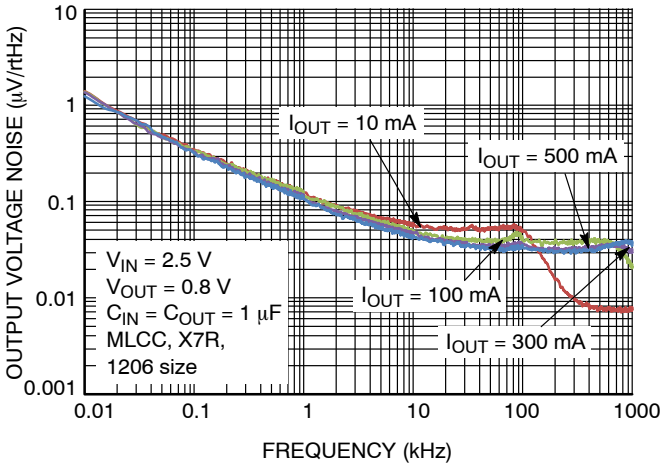
Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		V_{IN}	2.5		5.5	V
Output Voltage Range (Adjustable)		V_{OUT}	0.8		5.5–V_{DO}	V
Undervoltage Lock−out	V_{IN} rising	UVLO	1.2	1.6	1.9	V
Output Voltage Accuracy	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 0 − 500 mA	V_{OUT}	−2		+2	%
Reference Voltage		V_{REF}		0.8		V
Reference Voltage Accuracy	I_{OUT} = 10 mA	V_{REF}	−2		+2	%
Line Regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 4.5 V, I_{OUT} = 10 mA V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA	Reg_{LINE}		550 750		μV/V
Load Regulation	I_{OUT} = 0 mA to 500 mA	Reg_{LOAD}		12		μV/mA
Load Transient	I_{OUT} = 1 mA to 500 mA or 500 mA to 1 mA in 1 μs, C_{OUT} = 1 μF	$Tran_{LOAD}$		±120		mV
Dropout Voltage (Note 5)	I_{OUT} = 500 mA, $V_{OUT(nom)}$ = 2.8 V	V_{DO}		230	350	mV
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$	I_{CL}	510	750	950	mA
Quiescent Current	I_{OUT} = 0 mA	I_Q		13	25	μA
Ground Current	I_{OUT} = 500 mA	I_{GND}		260		μA
Shutdown Current	V_{EN} ≤ 0.4 V, T_J = +25°C	I_{DIS}		0.12		μA
	V_{EN} ≤ 0 V, V_{IN} = 2.0 to 4.5 V, T_J = −40 to +85°C	I_{DIS}		0.55	2	μA
EN Pin Threshold Voltage High Threshold Low Threshold	 V_{EN} Voltage increasing V_{EN} Voltage decreasing	 V_{EN_HI} V_{EN_LO}	 0.9		 0.4	V
EN Pin Input Current	V_{EN} = 5.5 V	I_{EN}		100	500	nA
ADJ Pin Current	V_{ADJ} = 0.8 V			1		nA
Turn−On Time	C_{OUT} = 1.0 μF, from assertion EN pin to 98% $V_{OUT(nom)}$	t_{ON}		150		μs
Power Supply Rejection Ratio	V_{IN} = 3.8 V, V_{OUT} = 2.8 V (Fixed), I_{OUT} = 500 mA; f = 100 Hz f = 1 kHz f = 10 kHz	PSRR		73 71 56		dB
Output Noise Voltage	V_{OUT} = 2.5 V (Fixed), V_{IN} = 3.5 V, I_{OUT} = 500 mA f = 100 Hz to 100 kHz	V_N		12		μV_{rms}
Thermal Shutdown Temperature	Temperature increasing from T_J = +25°C	T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}	T_{SDH}	–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at $V_{IN} = V_{OUT(NOM)} + 0.5$ V.

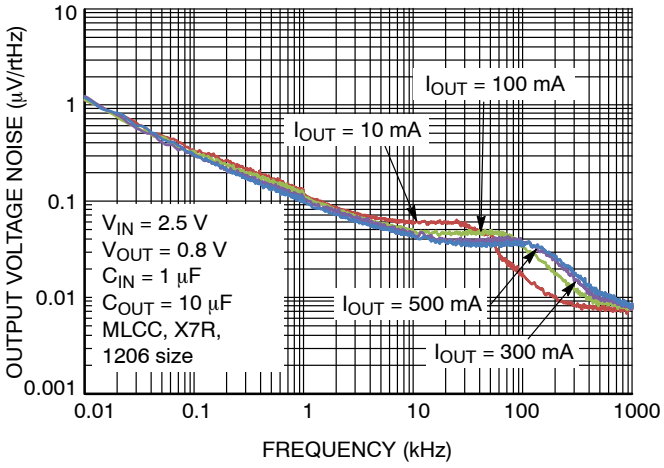
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TYPICAL CHARACTERISTICS



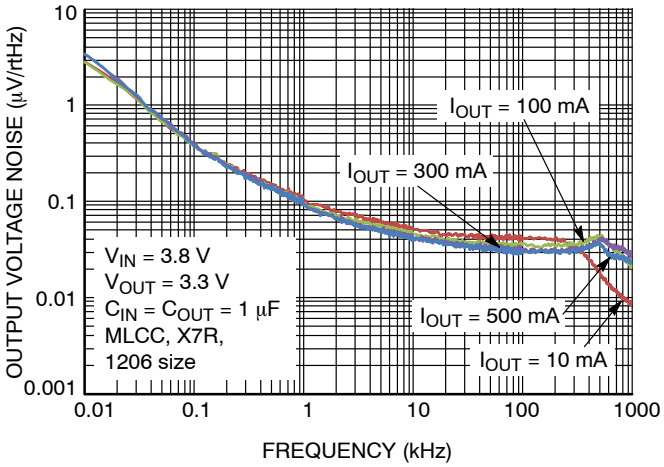
I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
10 mA	19.06	18.21
100 mA	15.99	15.04
300 mA	14.42	13.39
500 mA	13.70	12.60

Figure 3. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 1 μF



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
10 mA	16.17	15.28
100 mA	16.41	15.65
300 mA	14.94	14.10
500 mA	14.08	13.11

Figure 4. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 10 μF

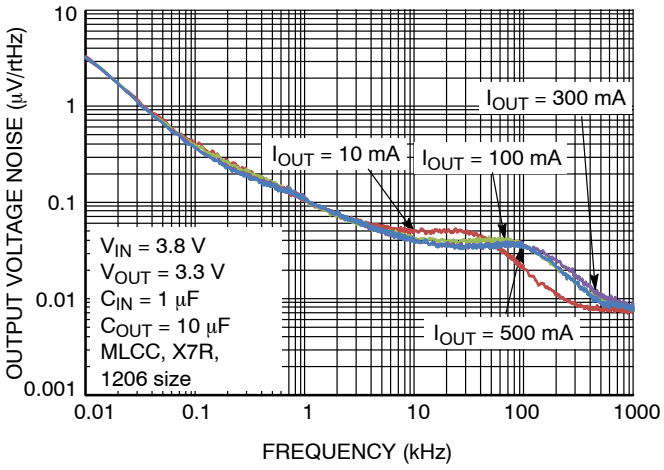


I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
10 mA	18.12	15.39
100 mA	16.42	13.50
300 mA	16.35	12.47
500 mA	16.00	12.10

Figure 5. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 1 μF

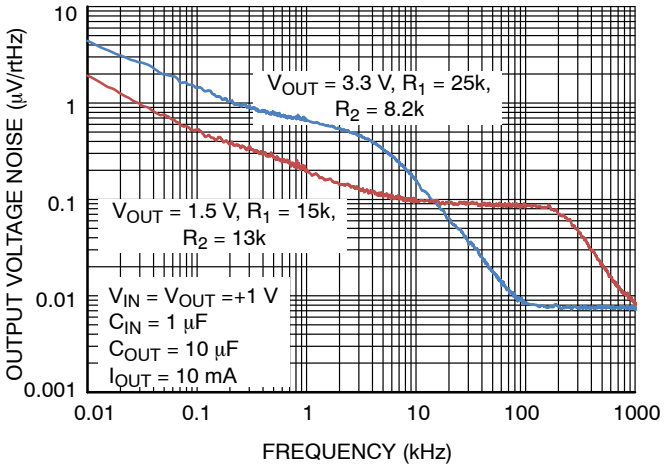
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TYPICAL CHARACTERISTICS



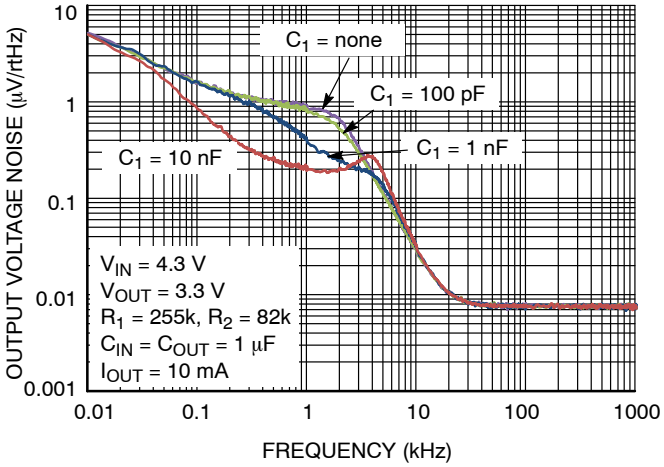
I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	17.35	14.07
100 mA	17.43	14.29
300 mA	16.55	13.33
500 mA	16.48	13.20

Figure 6. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 10 μF



V_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1.5 V	31.40	30.33
3.3 V	49.14	44.30

Figure 7. Output Voltage Noise Spectral Density for Adjustable Version – Different Output Voltage



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
none	50.17	43.85
100 pF	46.90	40.39
1 nF	36.92	27.99
10 nF	27.02	18.31

Figure 8. Output Voltage Noise Spectral Density for Adjustable Version for Various C1

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TYPICAL CHARACTERISTICS

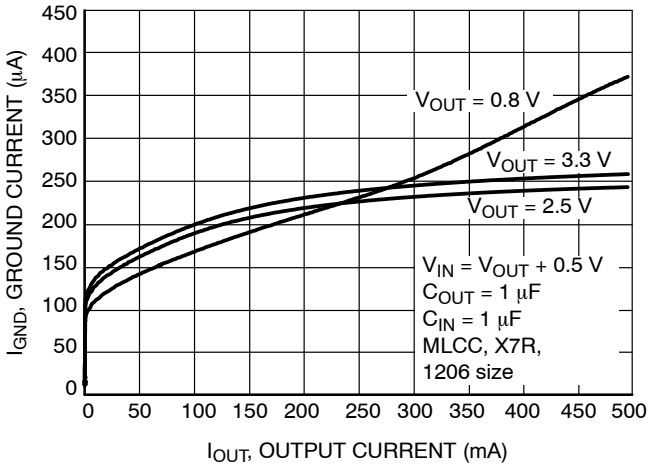


Figure 9. Ground Current vs. Output Current

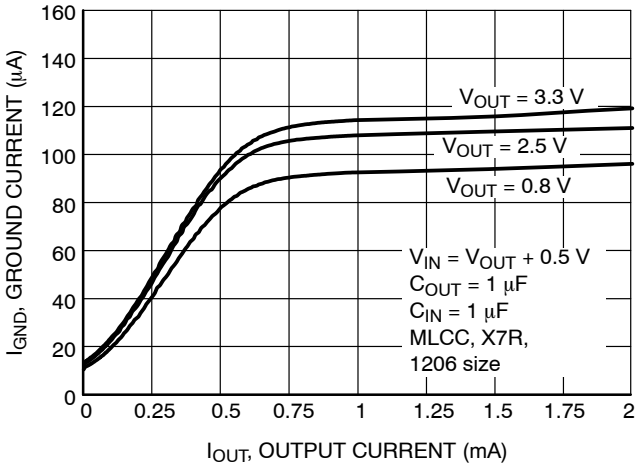


Figure 10. Ground Current vs. Output Current from 0 mA to 2 mA

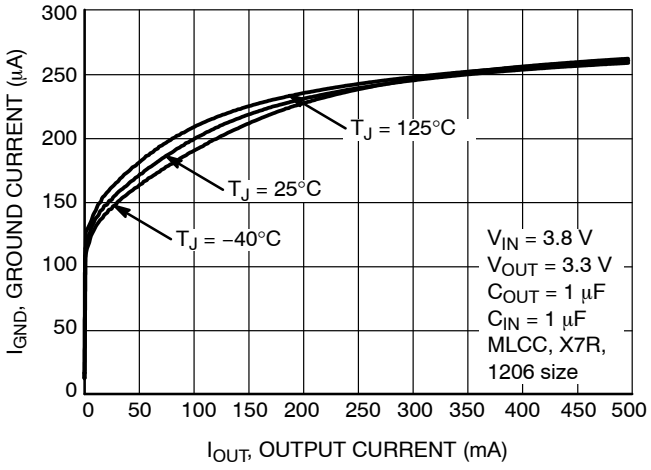


Figure 11. Ground Current vs. Output Current at Temperatures

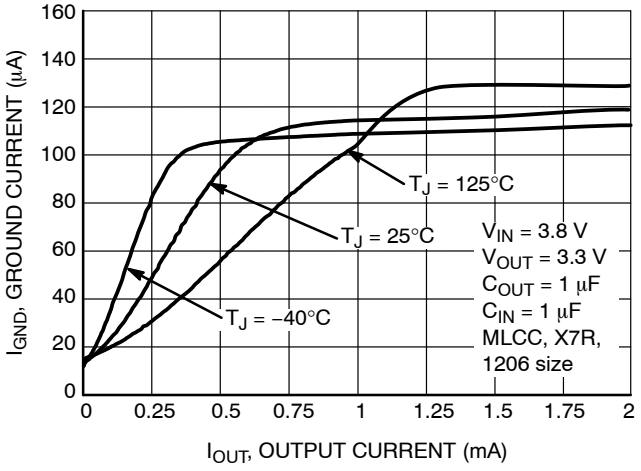


Figure 12. Ground Current vs. Output Current 0 mA to 2 mA at Temperature

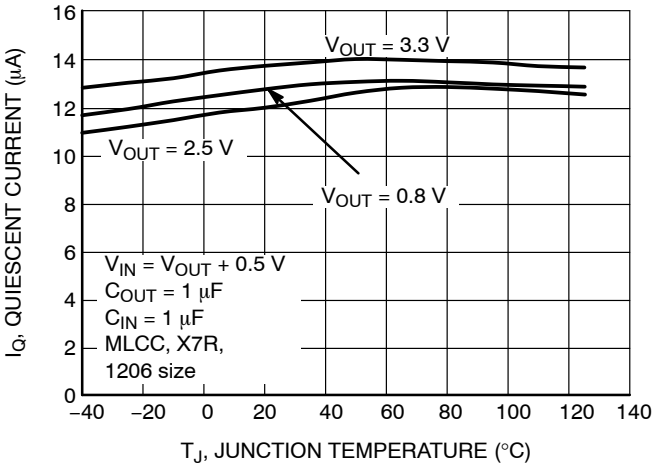


Figure 13. Quiescent Current vs. Temperature

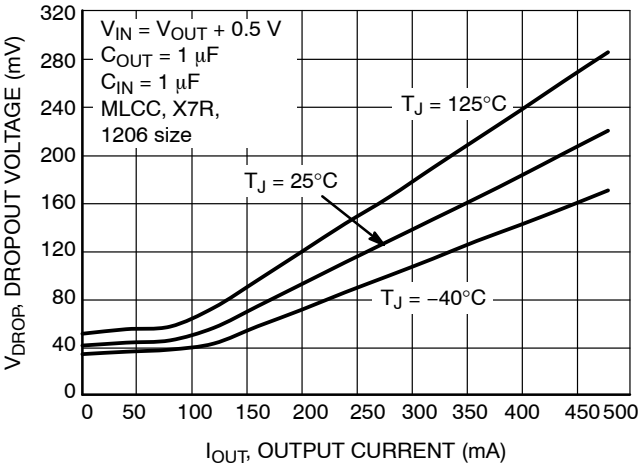


Figure 14. Dropout Voltage vs. Output Current at Temperature (2.5 V)

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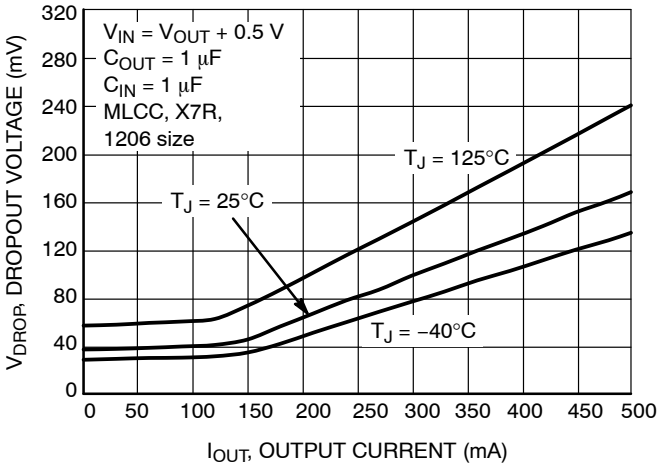


Figure 15. Dropout Voltage vs. Output Current at Temperatures (3.3 V)

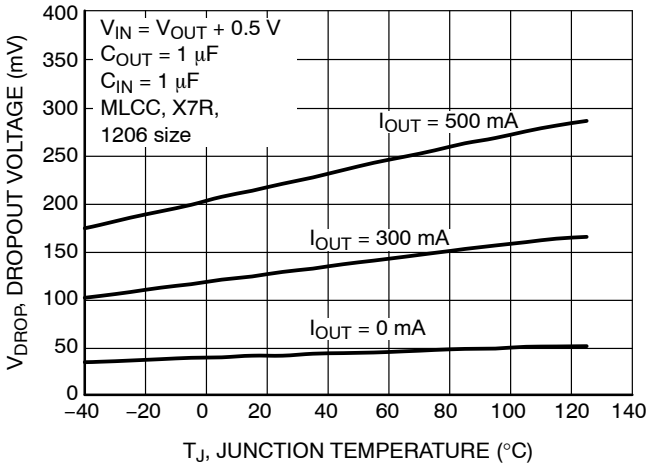


Figure 16. Dropout Voltage vs. Temperature (2.5 V)

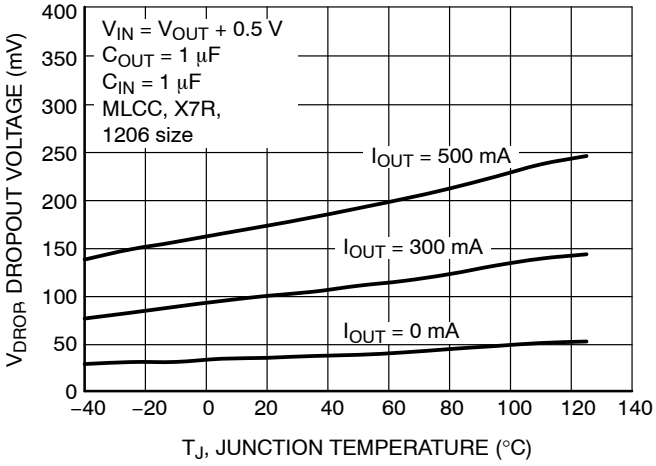


Figure 17. Dropout Voltage vs. Temperature, (3.3 V)

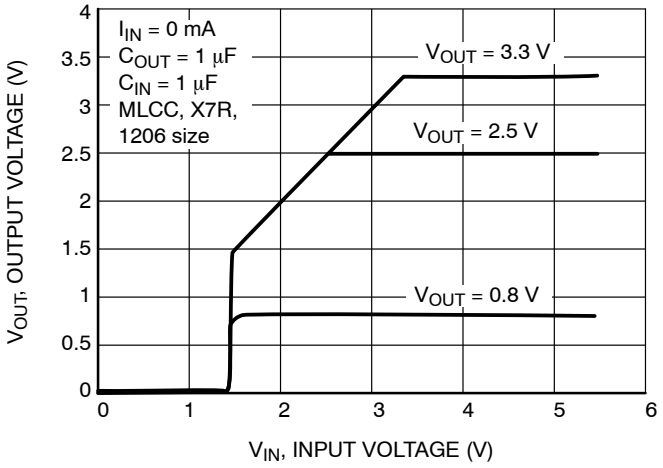


Figure 18. Input Voltage vs. Output Voltage

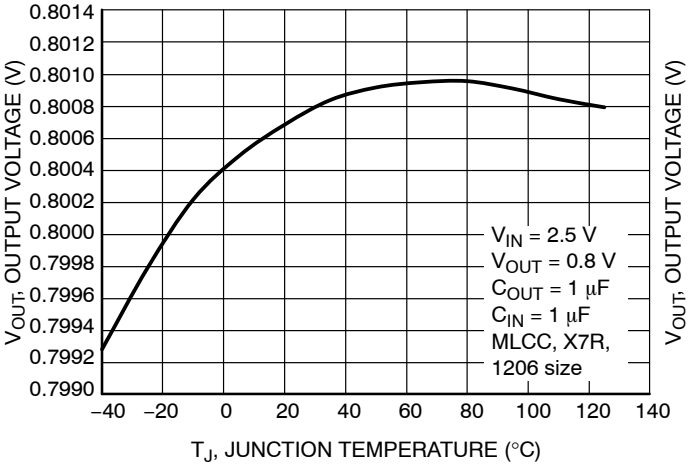


Figure 19. Output Voltage vs. Temperature, (0.8 V)

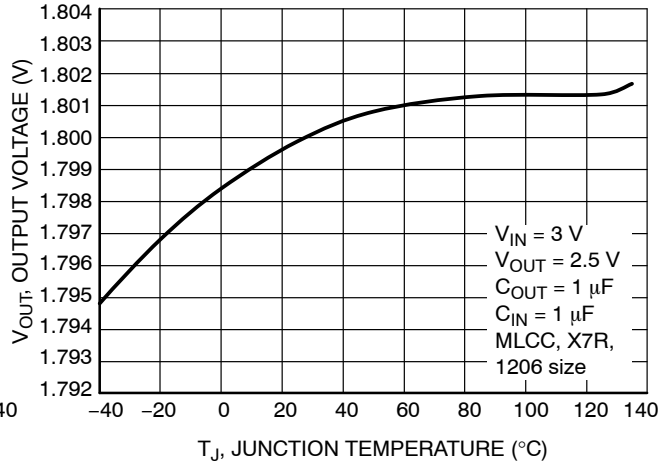


Figure 20. Output Voltage vs. Temperature, (2.5 V)

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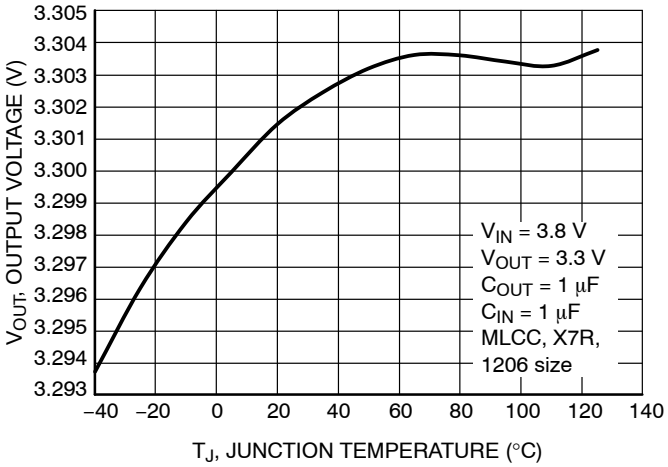


Figure 21. Output Voltage vs. Temperature, (3.3 V)

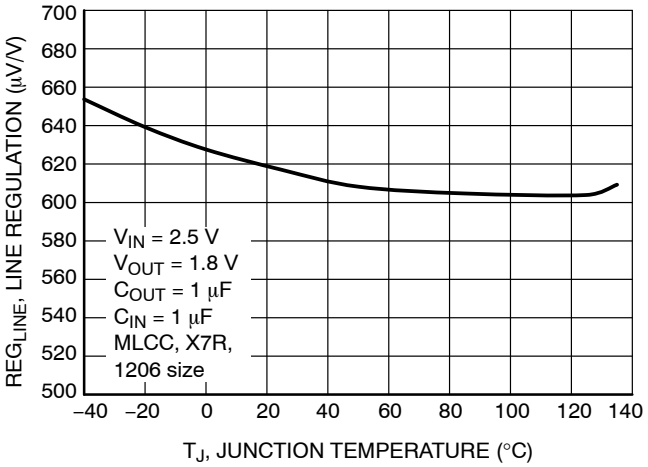


Figure 22. Line Regulation vs. Temperature, (1.8 V)

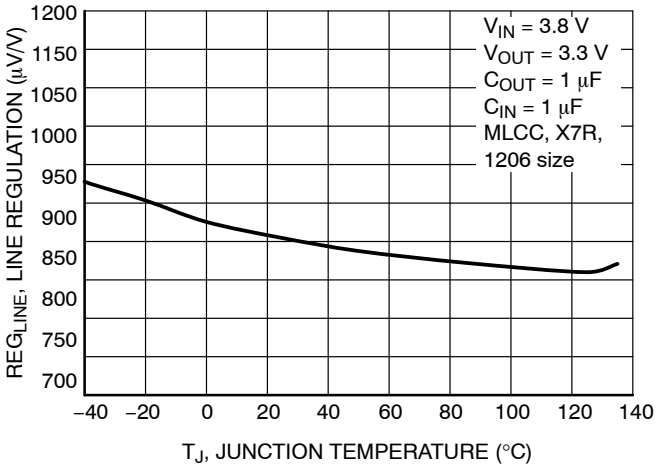


Figure 23. Line Regulation vs. Temperature, (3.3 V)

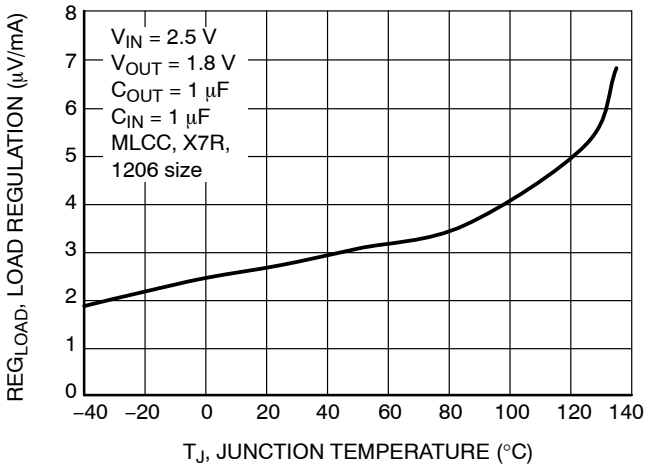


Figure 24. Load Regulation vs. Temperature, (1.8 V)

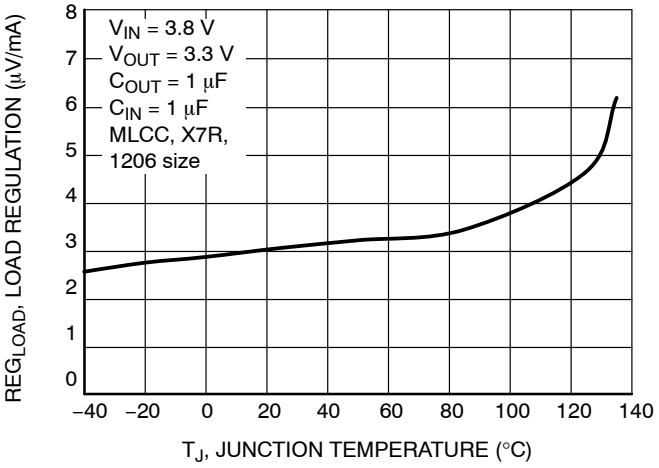


Figure 25. Load Regulation vs. Temperature, (3.3 V)

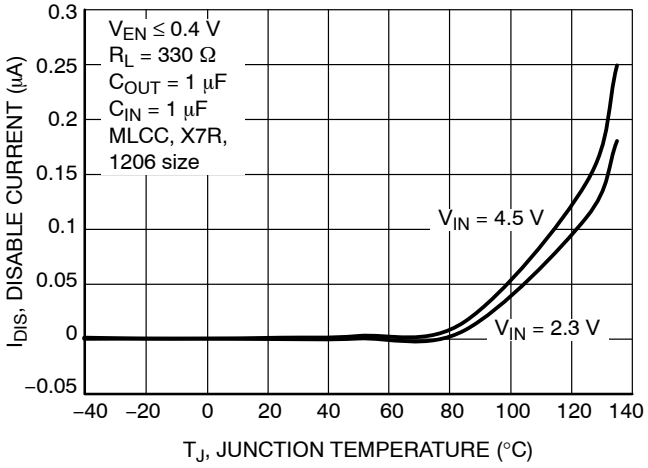


Figure 26. Disable Current vs. Temperature

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TYPICAL CHARACTERISTICS

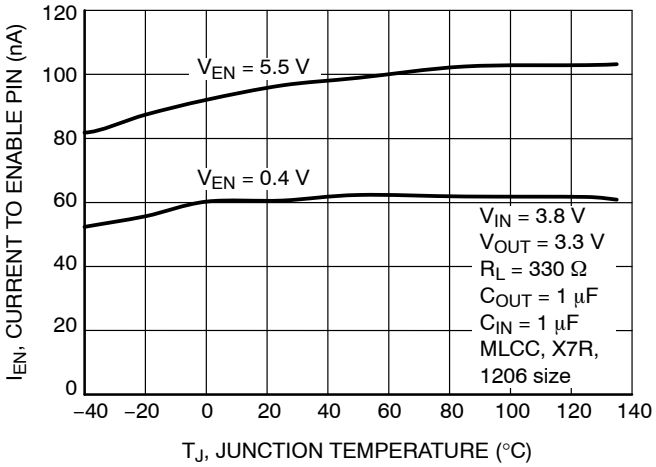


Figure 27. Enable Current vs. Temperature

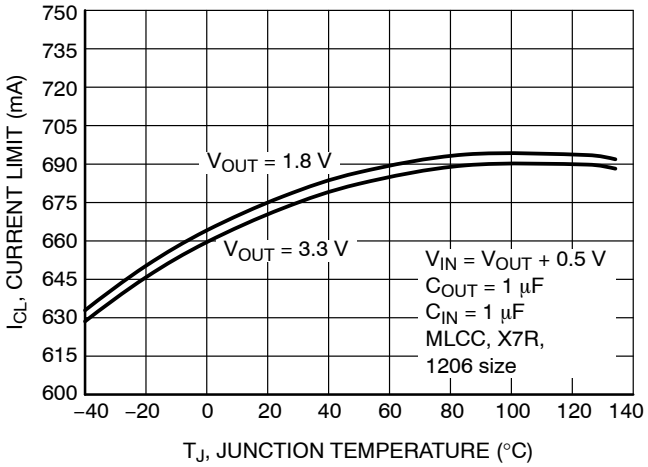


Figure 28. Current Limit vs. Temperature

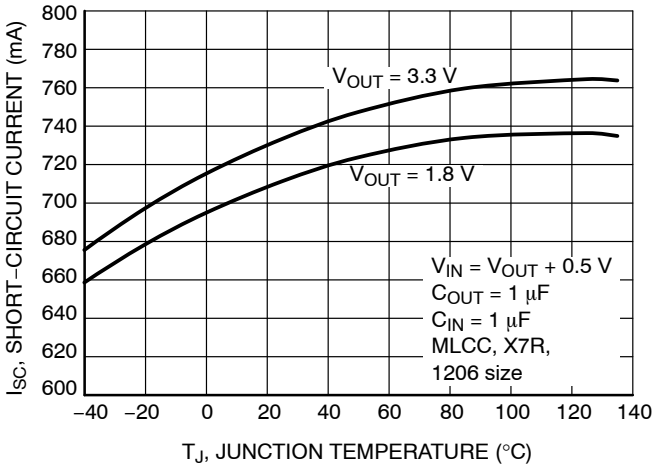


Figure 29. Short−Circuit vs. Temperature

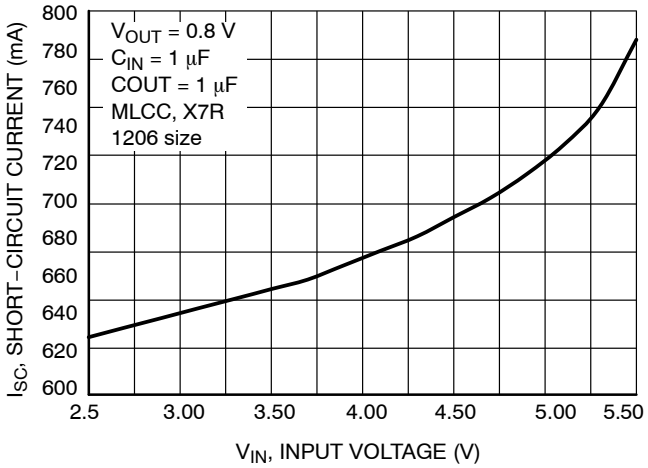


Figure 30. Short−Circuit Current vs. Temperature

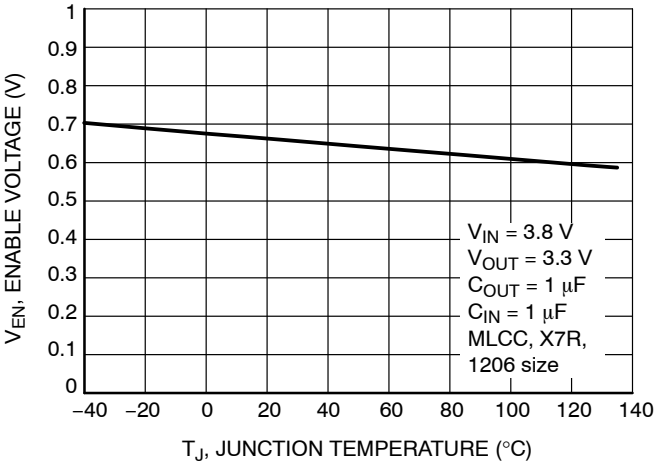


Figure 31. Enable Threshold (High)

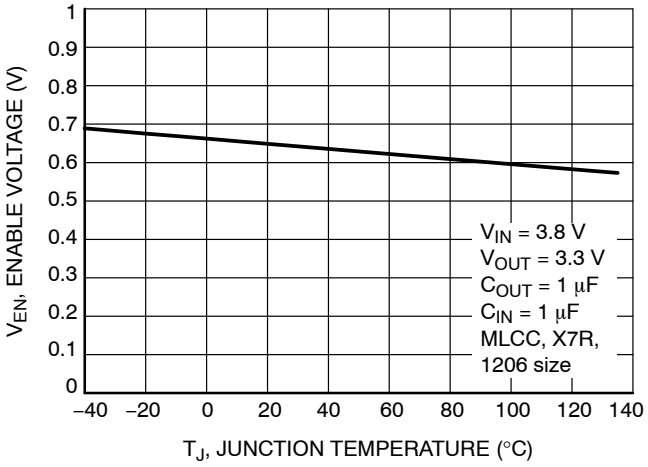


Figure 32. Enable Threshold (Low)

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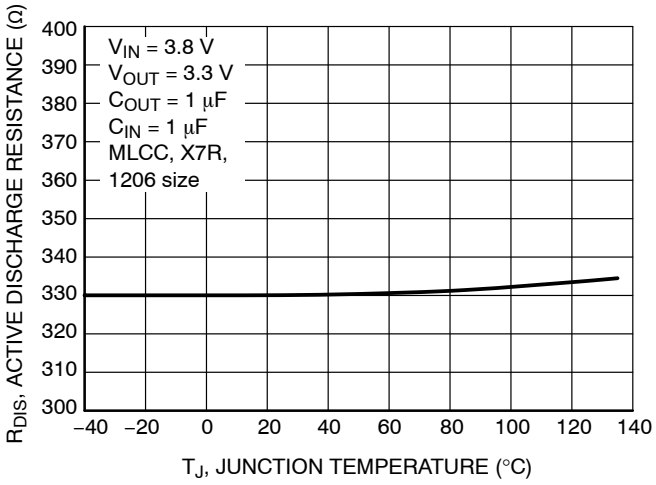


Figure 33. Discharge Resistance vs. Temperature

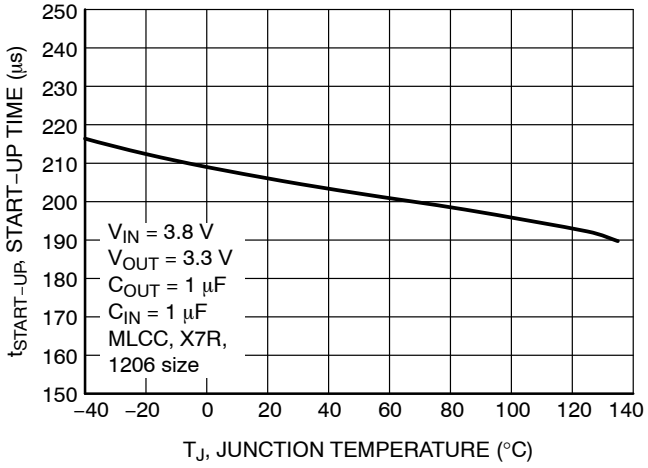


Figure 34. Start−up Time vs. Temperature

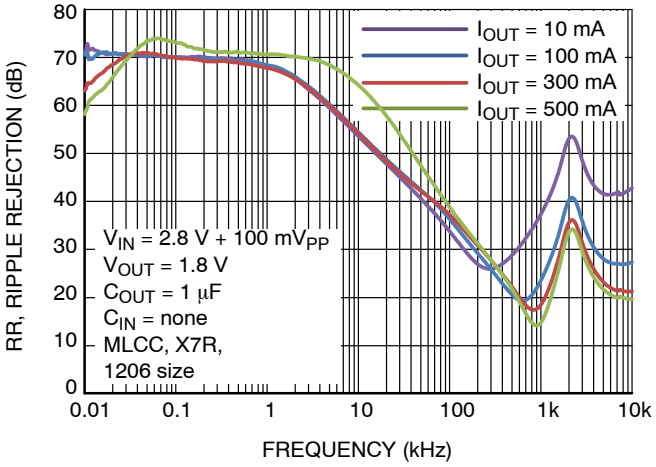


Figure 35. Power Supply Rejection Ratio, V_{OUT} = 1.8 V

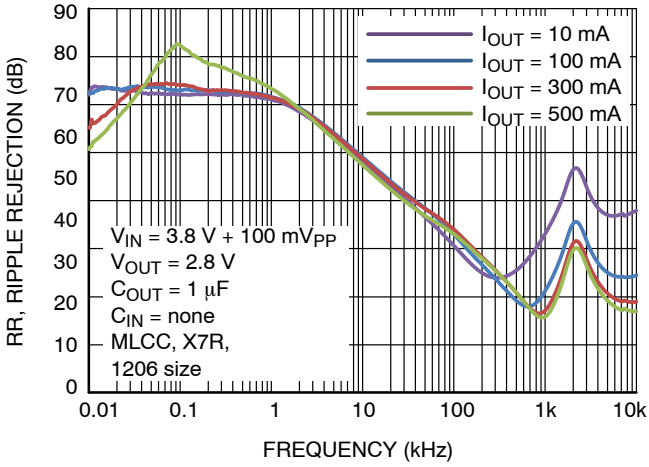


Figure 36. Power Supply Rejection Ratio, V_{OUT} = 2.8 V

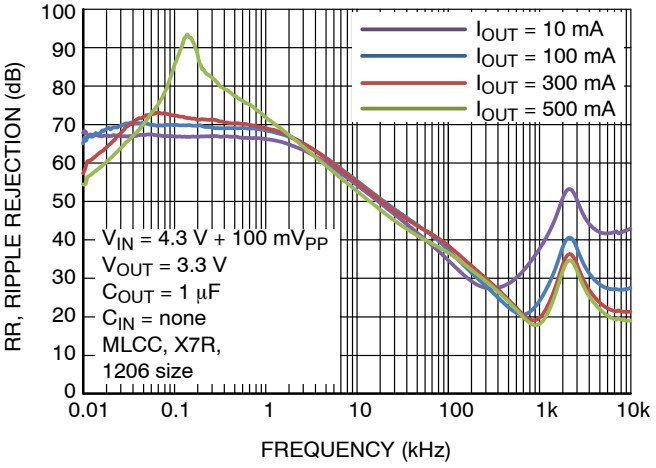


Figure 37. Power Supply Rejection Ratio, V_{OUT} = 3.3 V

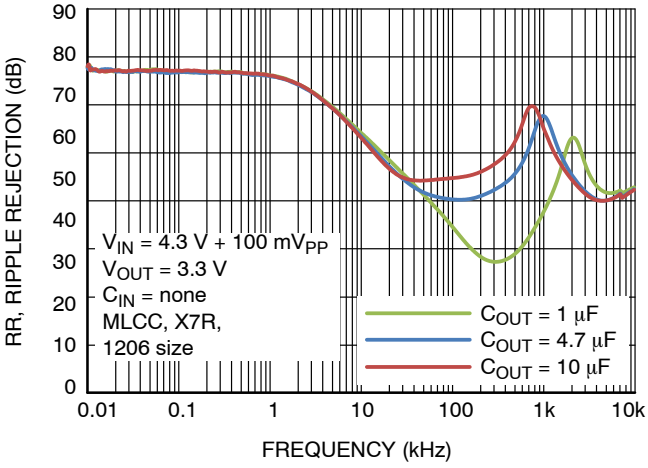


Figure 38. Power Supply Rejection Ratio, V_{OUT} = 3.3 V, I_{OUT} = 10 mA − Different C_{OUT}

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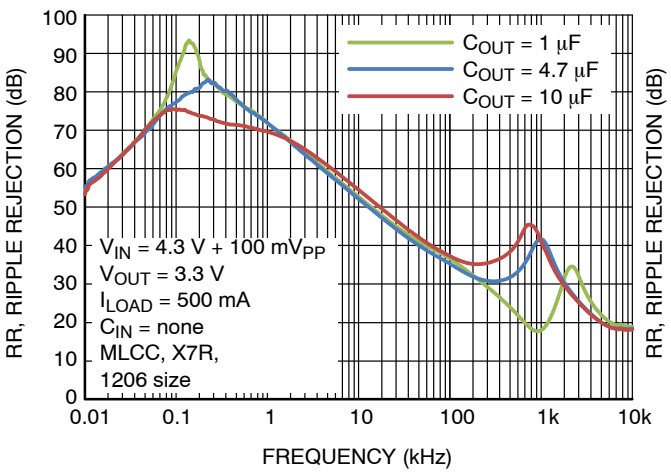


Figure 39. Power Supply Rejection Ratio, V_{OUT} = 3.3 V, I_{OUT} = 500 mA – Different C_{OUT}

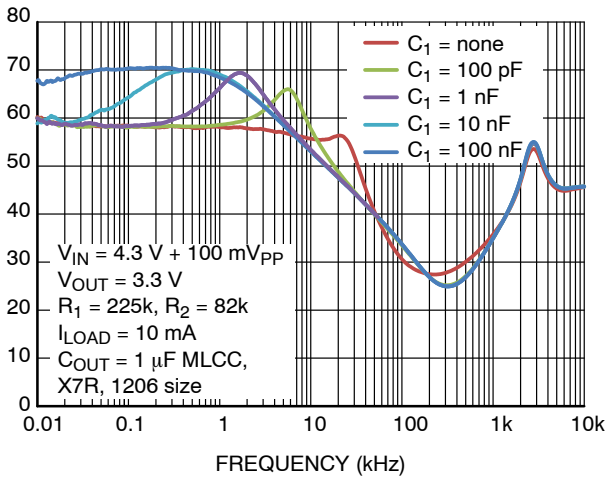


Figure 40. Power Supply Rejection Ratio, V_{OUT} = 3.3 V, I_{OUT} = 500 mA – Different C_{OUT}

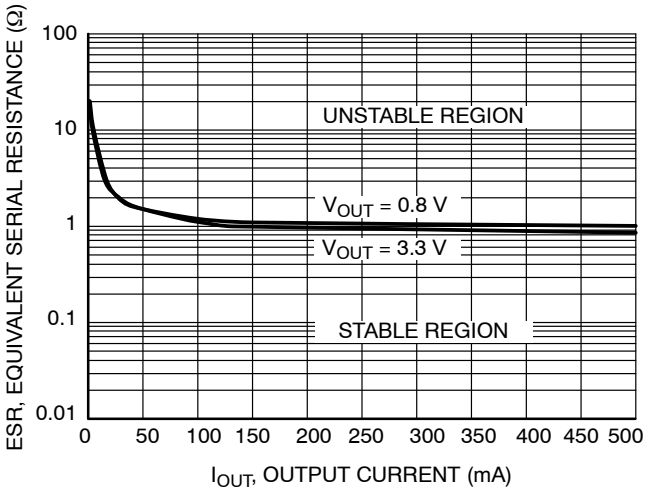


Figure 41. Output Capacitor ESR vs. Output Current

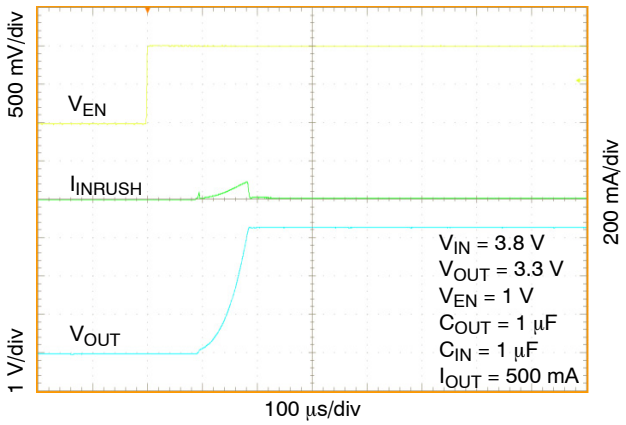


Figure 42. Enable Turn−on Response, C_{OUT} = 1 μF, I_{OUT} = 10 mA

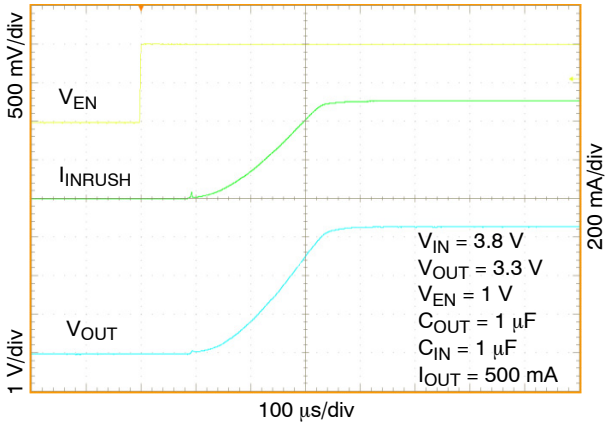


Figure 43. Enable Turn−on Response, C_{OUT} = 1 μF, I_{OUT} = 500 mA

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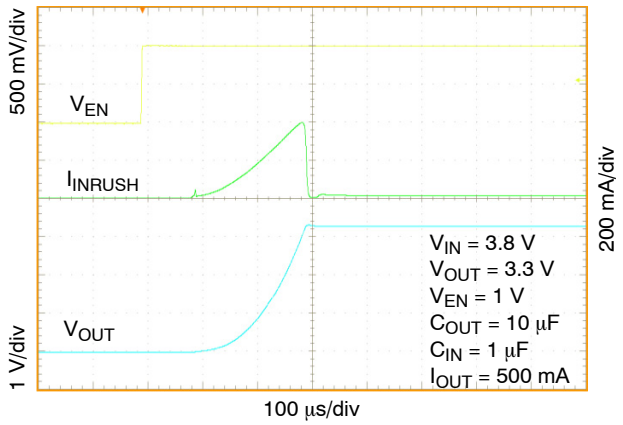


Figure 44. Enable Turn−on Response, C_{OUT} = 10 μF, I_{OUT} = 10 mA

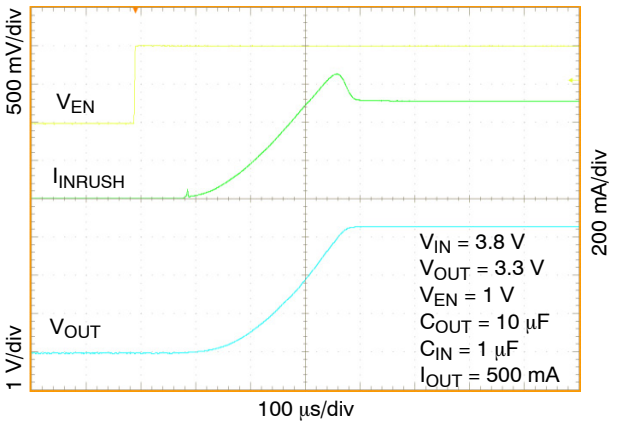


Figure 45. Enable Turn−on Response, C_{OUT} = 10 μF, I_{OUT} = 500 mA

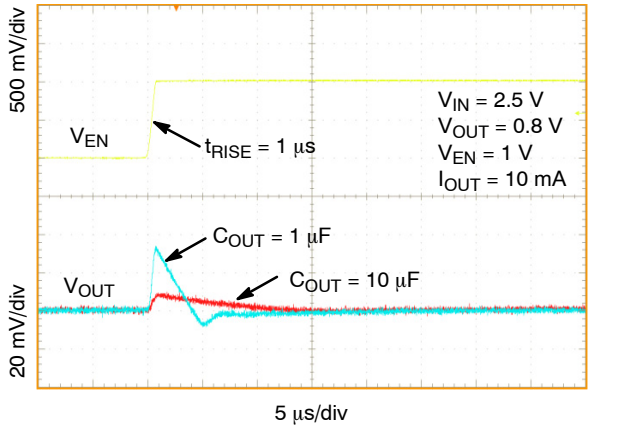


Figure 46. Line Transient Response − Rising Edge, V_{OUT} = 0.8 V, I_{OUT} = 10 mA

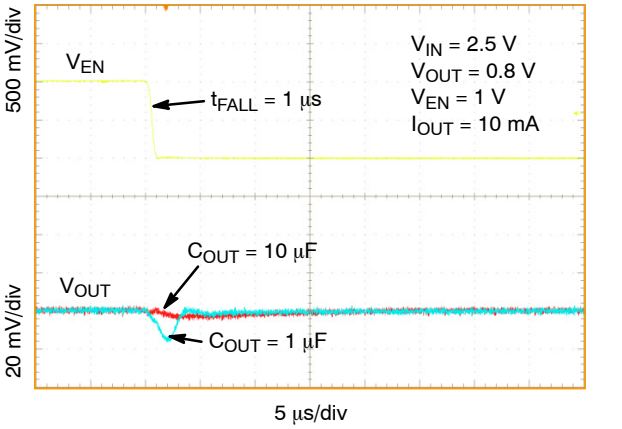


Figure 47. Line Transient Response − Falling Edge, V_{OUT} = 0.8 V, I_{OUT} = 10 mA

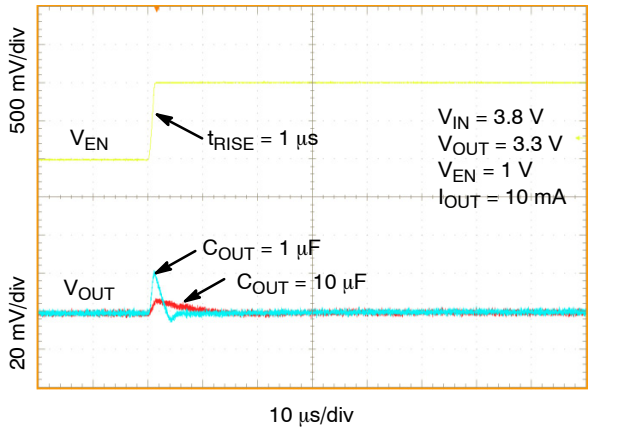


Figure 48. Line Transient Response − Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 10 mA

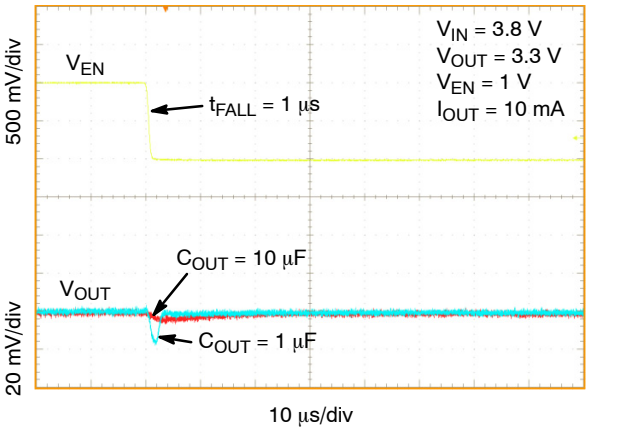


Figure 49. Line Transient Response − Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 10 mA

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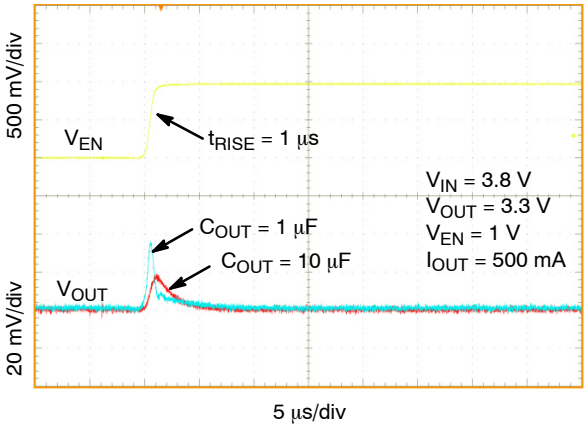


Figure 50. Line Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

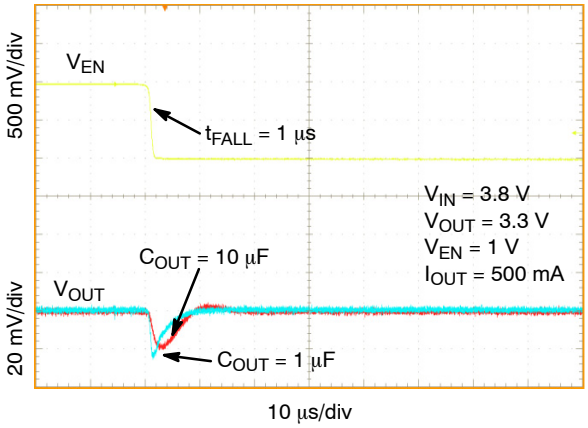


Figure 51. Line Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

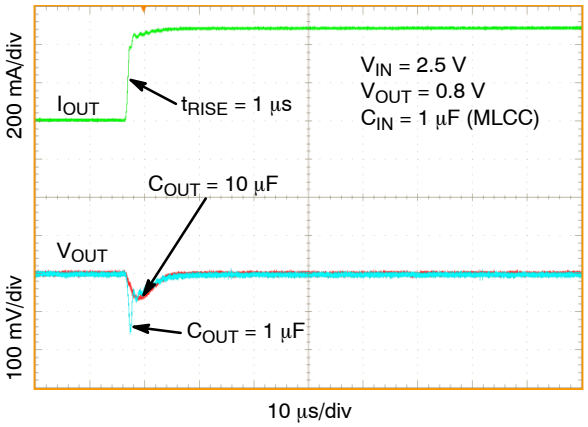


Figure 52. Load Transient Response – Rising Edge, V_{OUT} = 0.8 V, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 1 μF, 10 μF

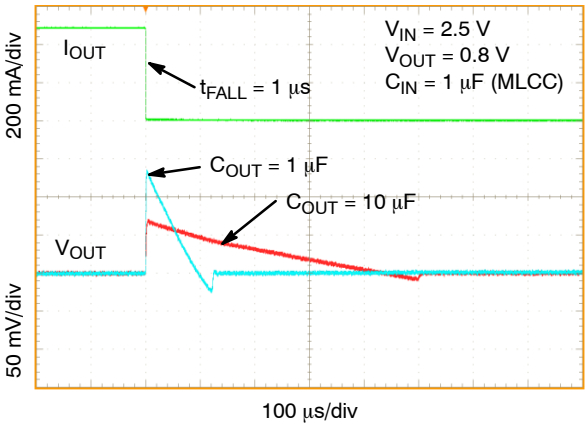


Figure 53. Load Transient Response – Falling Edge, V_{OUT} = 0.8 V, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 1 μF, 10 μF

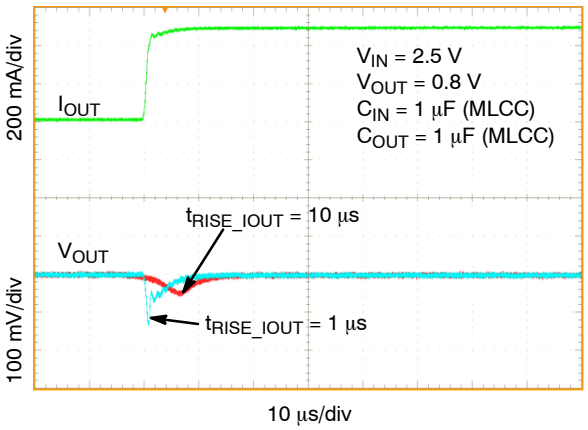


Figure 54. Load Transient Response – Rising Edge, V_{OUT} = 0.8 V, I_{OUT} = 1 mA to 500 mA, t_{RISE_IOUT} = 1 μs, 10 μs

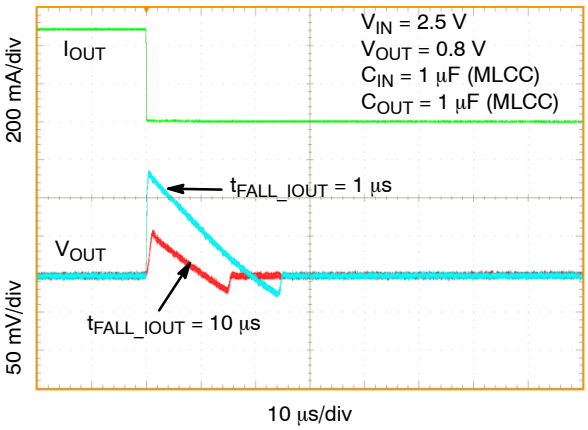


Figure 55. Load Transient Response – Falling Edge, V_{OUT} = 0.8 V, I_{OUT} = 1 mA to 500 mA, t_{FALL_IOUT} = 1 μs, 10 μs

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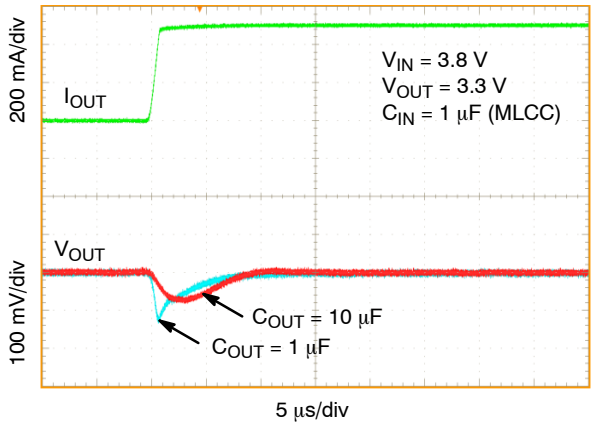


Figure 56. Load Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 1 μF, 10 μF

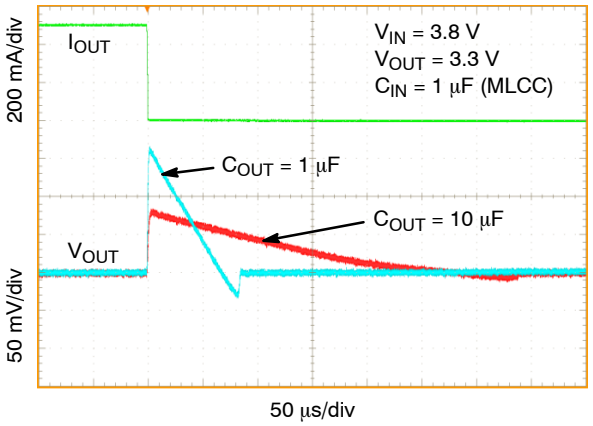


Figure 57. Load Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to 500 mA, C_{OUT} = 1 μF, 10 μF

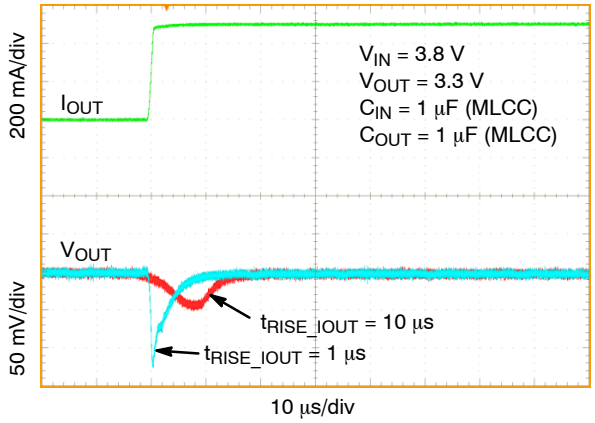


Figure 58. Load Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to 500 mA, t_{RISE_IOUT} = 1 μs, 10 μs

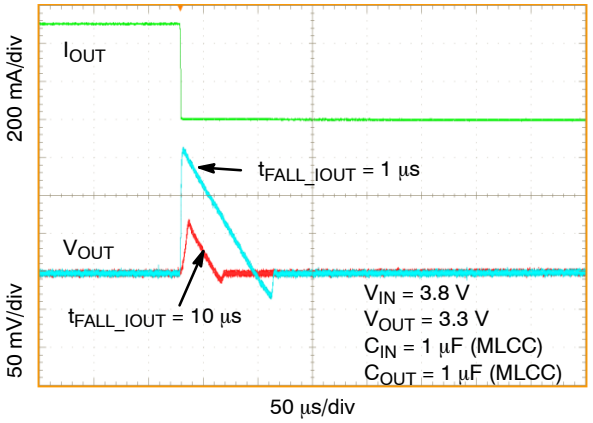


Figure 59. Load Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to 500 mA, t_{FALL_IOUT} = 1 μs, 10 μs

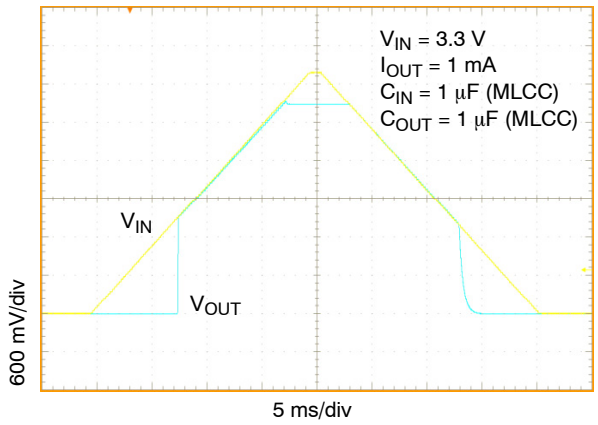


Figure 60. Turn−on/off, Slow Rising V_{IN}

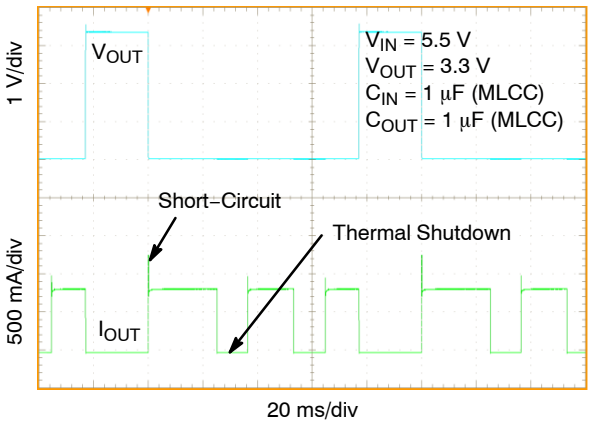


Figure 61. Short−Circuit and Thermal Shutdown

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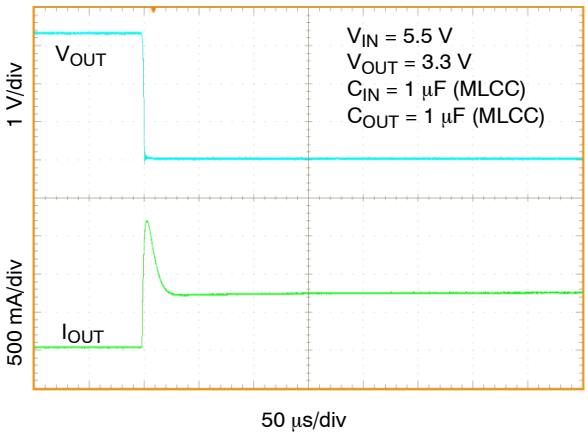


Figure 62. Short−Circuit Current Peak

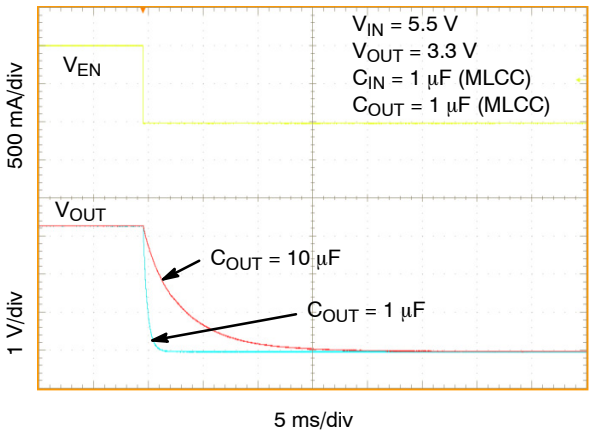


Figure 63. Enable Turn−off

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APPLICATIONS INFORMATION

General

The NCV8705 is a high performance 500 mA Low Dropout Linear Regulator. This device delivers excellent noise and dynamic performance. Thanks to its adaptive ground current feature the device consumes only 13 μA of quiescent current at no−load condition. The regulator features ultra−low noise of 12 μVRMS, PSRR of 71 dB at 1 kHz and very good load/line transient performance. Such excellent dynamic parameters and small package size make the device an ideal choice for powering the precision analog and noise sensitive circuitry in portable applications. The LDO achieves this ultra low noise level output without the need for a noise bypass capacitor. A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 10 nA from the IN pin. The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (CIN)

It is recommended to connect a minimum of 1 μF Ceramic X5R or X7R capacitor close to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. /max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (COUT)

The NCV8705 requires an output capacitor connected as close as possible to the output pin of the regulator. The minimal capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCV8705 is designed to remain stable with minimum effective capacitance of 1 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0402 the effective capacitance drops rapidly with the applied DC bias. Refer to the Figure 64, for the capacitance vs. package size and DC bias voltage dependence.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 900 mΩ. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR as shown in typical characteristics. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. The tantalum capacitors are generally more costly than ceramic capacitors.

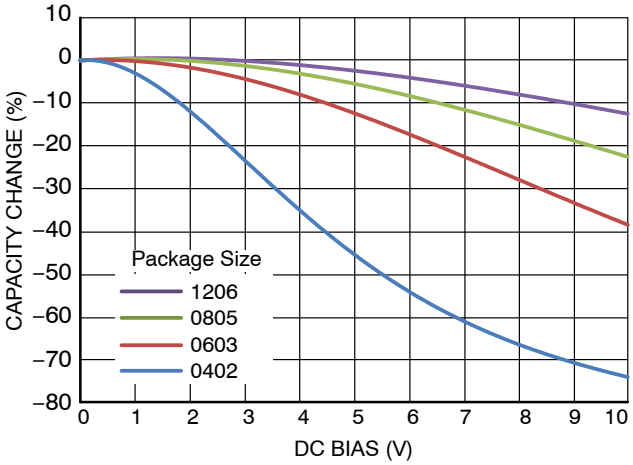


Figure 64. Capacitance Change vs. DC Bias

No−load Operation

The regulator remains stable and regulates the output voltage properly within the ±2% tolerance limits even with no external load applied to the output.

Adjustable Operation

The output voltage range can be set from 0.8 V to 5.5 V−V_{DO} by resistor divider network. Use Equations 1 and 2 to calculate appropriate values of resistors and output voltage. Typical current to ADJ pin is 1 nA. For output voltage 0.8 V ADJ pin can be tied directly to Vout pin.

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R_1}{R_2}\right) + R_1 \cdot I_{ADJ} \qquad \text{(eq. 1)}$$

$$R_2 \cong R_1 \cdot \frac{1}{\frac{V_{OUT}}{0.8} - 1} \qquad \text{(eq. 2)}$$

The resistor divider should be designed carefully to achieve the best performance. Recommended current through divider is 10 μA and more. Too high values of resistors (MΩ) cause increasing noise and longer start−up time. The suggested values of the resistors are in Table 5. To improve dynamic performance capacitor C1 should be at least 1 nF. Recommended range of capacity is between 10 nF and 100 nF. Higher value of capacitor C1 increasing start−up time.

Table 5. Proposal Resistor Values for Various V_{OUT}

V_{OUT}	R1	R2
1.5 V	130k	150k
3.3 V	256k	82k
5.0 V	430k	82k

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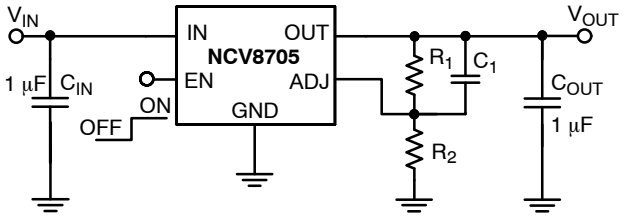


Figure 65. NCV8705 Adjustable with Noise Improvement Capacitor

Enable Operation

The NCV8705 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCV8705 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 110 nA which assures that the device is turned−off when the EN pin is not connected. Build in 2 mV hysteresis into the EN prevents from periodic on/off oscillations that can occur due to noise.

In the case where the EN function isn't required the EN should be tied directly to IN.

Undervoltage Lockout

The internal UVLO circuitry assures that the device becomes disabled when the V_{IN} falls below typ. 1.5 V. When the V_{IN} voltage ramps−up the NCV8705 becomes enabled, if V_{IN} rises above typ. 1.6 V. The 100 mV hysteresis prevents from on/off oscillations that can occur due to noise on V_{IN} line.

Output Current Limit

Output Current is internally limited within the IC to a typical 750 mA. The NCV8705 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 800 mA (typ). The current limit and short circuit protection will work properly up to V_{IN} = 5.5 V at T_A = 125°C. There is no limitation for the short circuit duration.

Internal Soft−Start circuit

NCV8705 contains an internal soft−start circuitry to protect against large inrush currents which could otherwise flow during the start−up of the regulator. Soft−start feature protects against power bus disturbances and assures a controlled and monotonic rise of the output voltage.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCV8705 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCV8705 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{\theta_{JA}} \quad \text{(eq. 3)}$$

The power dissipated by the NCV8705 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}@I_{OUT}\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 4)}$$

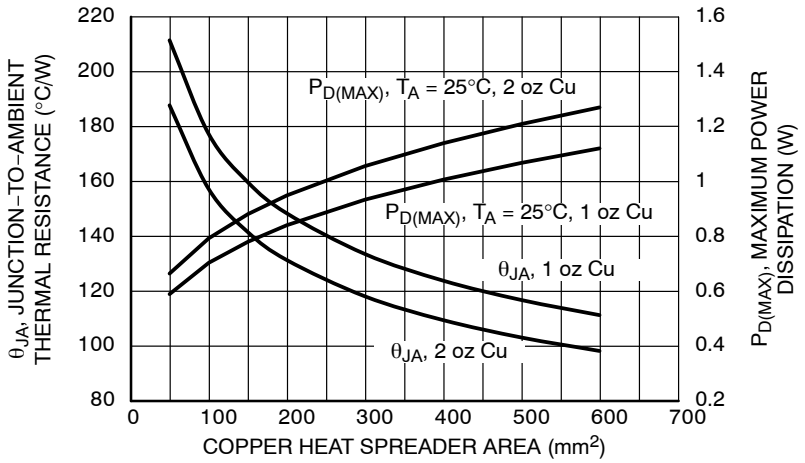


Figure 66. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (WDFN6)

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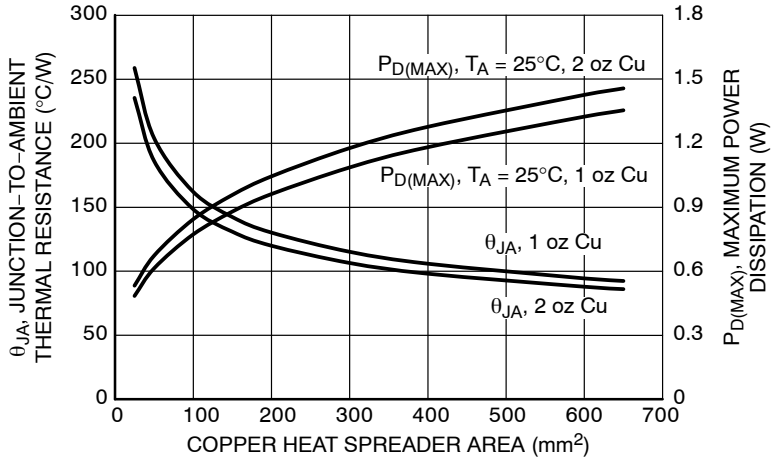


Figure 67. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (DFN8/DFNW8)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Load Regulation

The NCV8705 features very good load regulation of maximum 2 mV in 0 mA to 500 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause 50 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The IC features very good line regulation of 0.75 mV/V measured from $V_{IN} = V_{OUT} + 0.5$ V to 5.5V. For battery operated applications it may be important that the line regulation from $V_{IN} = V_{OUT} + 0.5$ V up to 4.5 V is only 0.55 mV/V.

Power Supply Rejection Ratio

The NCV8705 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Output Noise

The IC is designed for ultra−low noise output voltage without external noise filter capacitor (C_{nr}). Figures 3 – 6 shows NCV8705 noise performance. Generally the noise performance in the indicated frequency range improves with increasing output current.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 4).

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ORDERING INFORMATION

Device	Voltage Option	Marking	Package	Feature	Shipping†
NCV8705MT12TCG	1.2 V	VF	WDFN6 (Pb−Free)	Non−Wettable Flank	3000 / Tape & Reel
NCV8705MT18TCG	1.8 V	VA			
NCV8705MT28TCG	2.8 V	VC			
NCV8705MT33TCG	3.3 V	VE			
NCV8705MTADJTCG	Adjustable	VJ			
NCV8705MW18TCG	1.8 V	8705W 180	DFN8 (Pb−Free)	Wettable Flank, SFS Process	3000 / Tape & Reel
NCV8705MW28TCG	2.8 V	8705W 280			
NCV8705MW30TCG	3.0 V	8705W 300			
NCV8705MWADJTCG	Adjustable	8705W ADJ			
NCV8705ML33TCG	3.3 V	8705L 330	DFNW8 (Pb−Free)	Wettable Flank, SLP Process	3000 / Tape & Reel

DISCONTINUED (Note 6)

NCV8705MT30TCG	3.0 V	VD	WDFN6 (Pb−Free)	Non−Wettable Flank	3000 / Tape & Reel
NCV8705MW12TCG	1.2 V	8705W 120	DFN8 (Pb−Free)	Wettable Flank, SFS Process	3000 / Tape & Reel
NCV8705MW33TCG	3.3 V	8705W 330	DFN8 (Pb−Free)	Wettable Flank, SFS Process	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

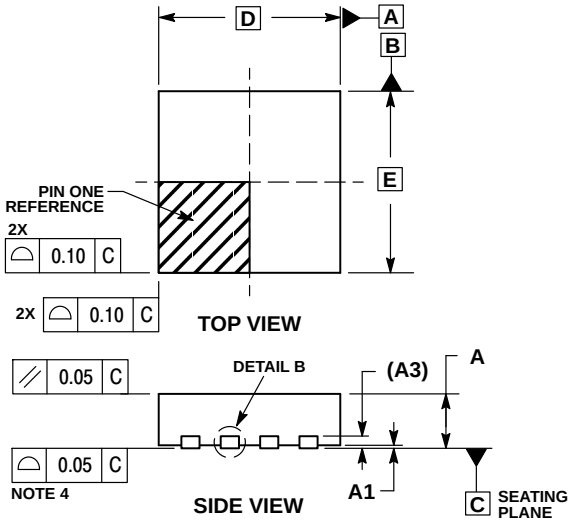
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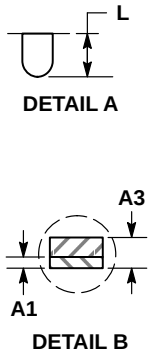


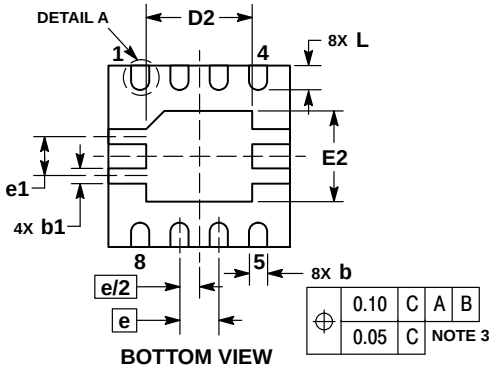
DFN8, 3x3, 0.65P
CASE 506DB
ISSUE A

DATE 12 OCT 2016

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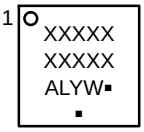




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.20	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.40	1.60
e	0.65 BSC	
e1	0.65 REF	
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

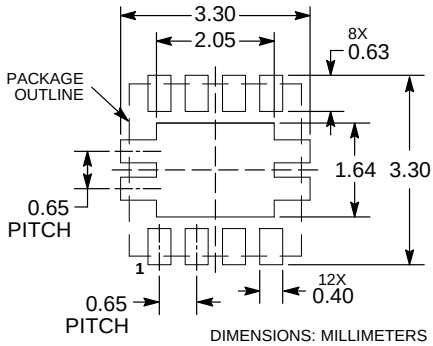


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN8, 3X3, 0.65P**		**PAGE 1 OF 1**

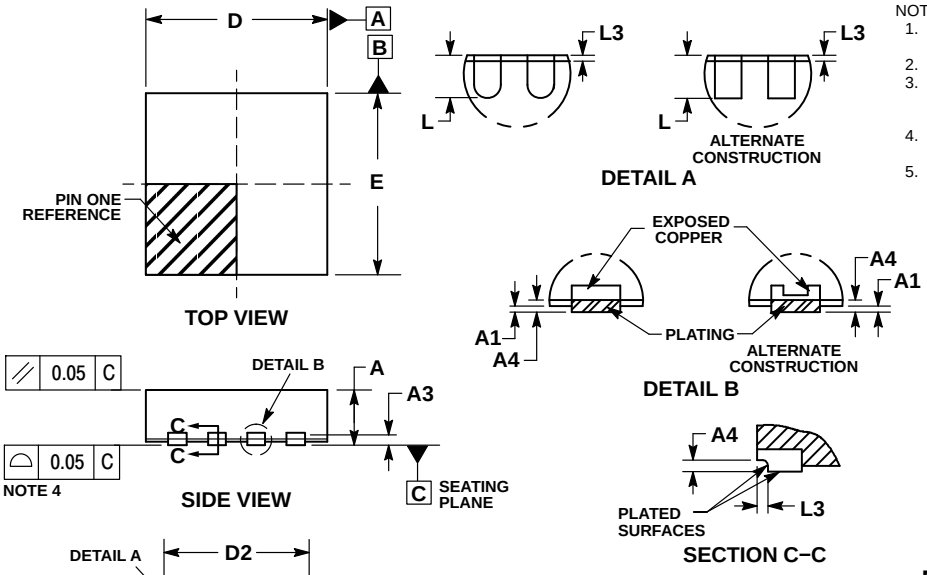
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SCALE 2:1

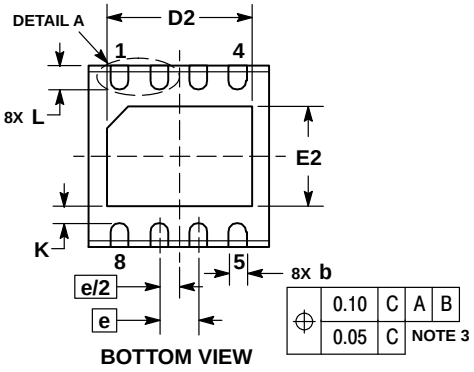
DFNW8 3x3, 0.65P
CASE 507AD
ISSUE A

DATE 15 JUN 2018

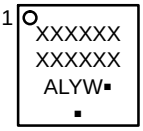


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	−−−	−−−	0.05
A3		0.20 REF	
A4	0.10	−−−	−−−
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D2	2.30	2.40	2.50
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
e		0.65 BSC	
K		0.28 REF	
L	0.30	0.40	0.50
L3		0.05 REF	



GENERIC MARKING DIAGRAM*

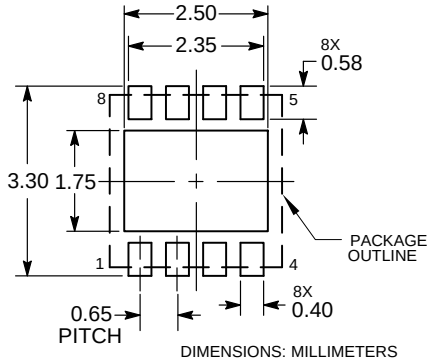


XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



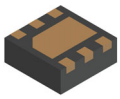
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFNW8 3x3, 0.65P**	**PAGE 1 OF 1**

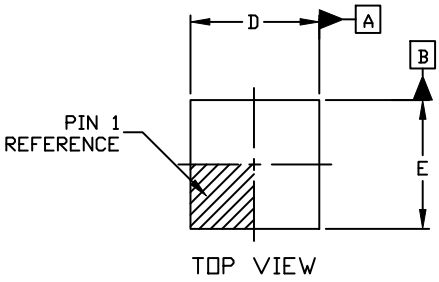
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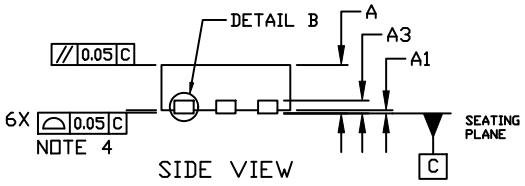
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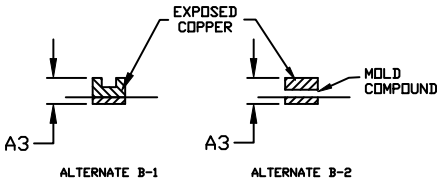


WDFN6 2x2, 0.65P
CASE 511BR
ISSUE C

DATE 01 DEC 2021



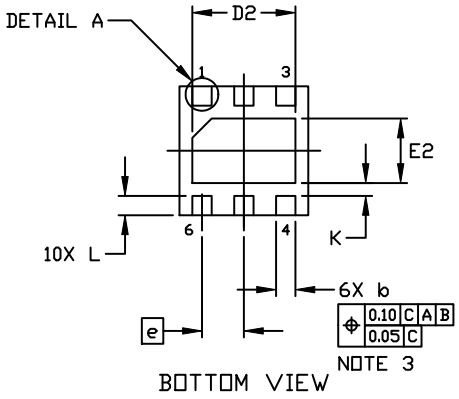


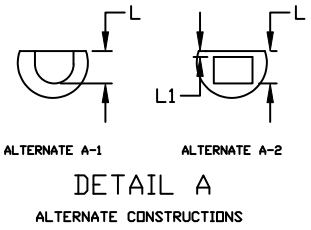


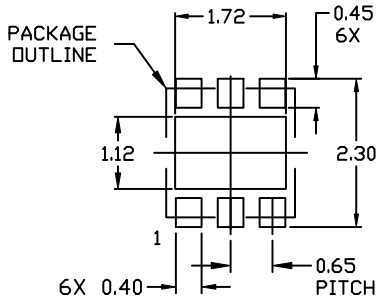
NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e		0.65 BSC	
K		0.20 REF	
L	0.20	0.30	0.40
L1	---	---	0.15







For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

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