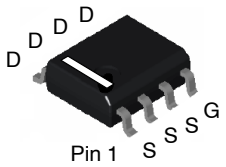
MOSFET – P-Channel, POWERTRENCH®

-30 V, -8.8 A, 20 mΩ

FDS4435BZ



SOIC8
CASE 751EB

Description

This P−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- Max $R_{DS(on)}$ = 20 mΩ at V_{GS} = −10 V, I_D = −8.8 A
- Max $R_{DS(on)}$ = 35 mΩ at V_{GS} = −4.5 V, I_D = −6.7 A
- Extended V_{GSS} Range (−25 V) for Battery Applications
- HBM ESD Protection Level of ±3.8 kV Typical (Note 3)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb−Free and RoHS Compliant

Specifications

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

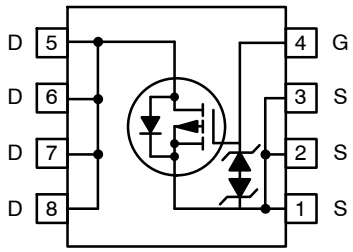
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	−30	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current – Continuous T_A = 25°C (Note 1a) – Pulsed	 −8.8 −50	A
P_D	Power Dissipation T_A = 25°C (Note 1a)	2.5	W
	Power Dissipation T_A = 25°C (Note 1b)	1.0	
E_{AS}	Single Pulse Avalanche Energy (Note 4)	24	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

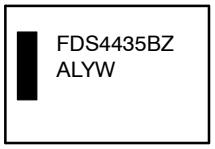
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CONNECTION



MARKING DIAGRAM



FDS4435BZ = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
FDS4435BZ	SOIC8 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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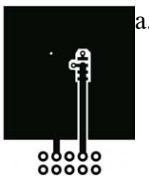
Table 1. ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−30			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C		−21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −24 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−1	−2.1	−3	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C		6		mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = −10 V, I_D = −8.8 A		16	20	mΩ
		V_{GS} = −4.5 V, I_D = −6.7 A		26	35	
		V_{GS} = −10 V, I_D = −8.8 A, T_J = 125°C		22	28	
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −8.8 A		24		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −15 V, V_{GS} = 0 V, f = 1MHz		1385	1845	pF
C_{oss}	Output Capacitance			275	365	pF
C_{rss}	Reverse Transfer Capacitance			230	345	pF
R_g	Gate Resistance	f = 1MHz		4.5		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −15 V, I_D = −8.8 A, V_{GS} = −10 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Rise Time			6	12	ns
$t_{d(off)}$	Turn−Off Delay Time			30	48	ns
t_f	Fall Time			12	22	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to −10 V, V_{DD} = −15 V, I_D = −8.8 A		28	40	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to −5 V, V_{DD} = −15 V, I_D = −8.8 A		16	23	nC
Q_{gs}	Gate to Source Charge	V_{DD} = −15 V, I_D = −8.8 A		5.2		nC
Q_{gd}	Gate to Drain “Miller” Charge			7.4		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = −8.8A (Note 2)		−0.9	−1.2	V
t_{rr}	Reverse Recovery Time	I_F = −8.8 A, di/dt = 100 A/μs		29	44	ns
Q_{rr}	Reverse Recovery Charge			23	35	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. Starting T_J = 25°C, L = 1 mH, I_{AS} = −7 A, V_{DD} = −30 V, V_{GS} = −10 V.

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TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

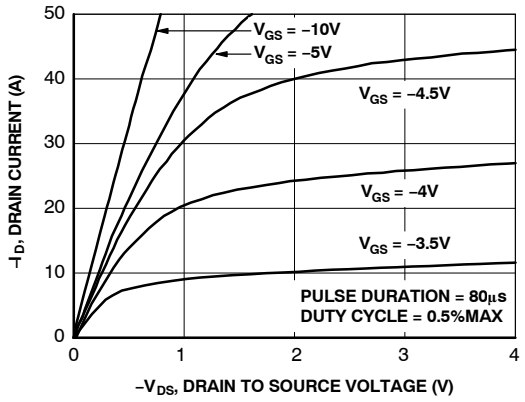


Figure 1. On−Region Characteristics

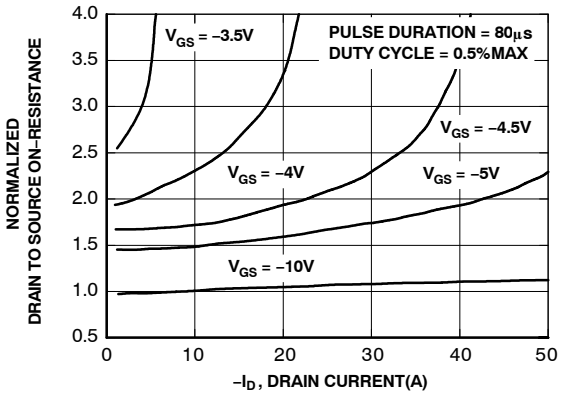


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

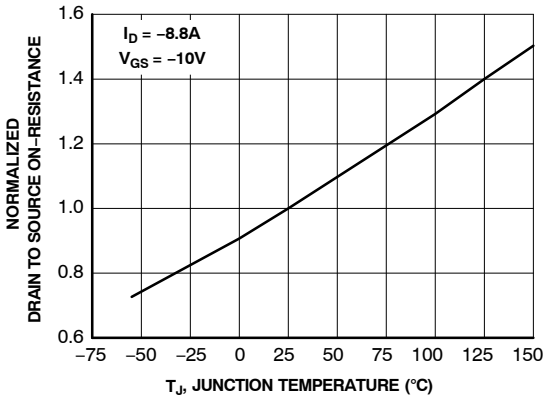


Figure 3. Normalized On−Resistance vs Junction Temperature

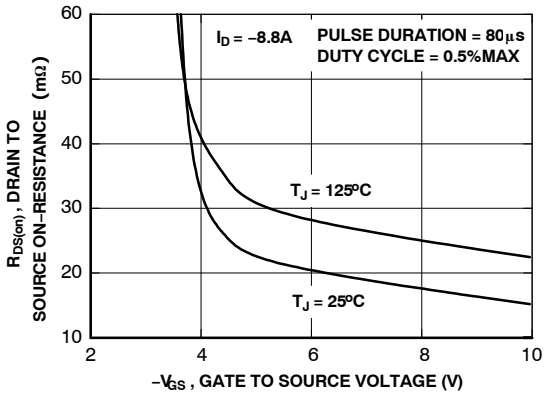


Figure 4. On−Resistance vs Gate to Source Voltage

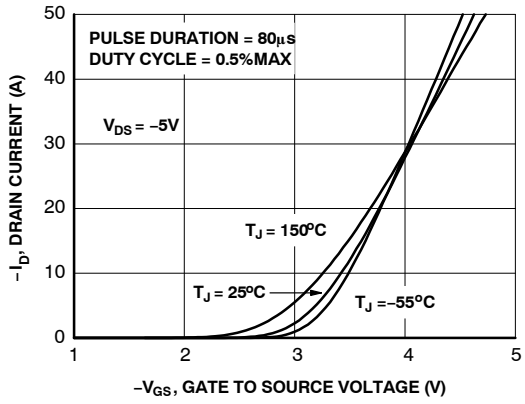


Figure 5. Transfer Characteristics

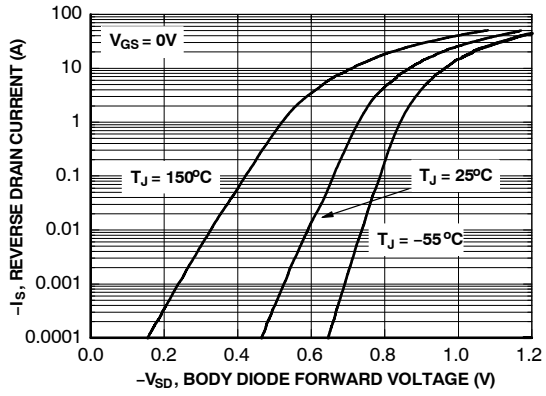


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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TYPICAL CHARACTERISTICS (Continued)

(T_J = 25°C unless otherwise noted)

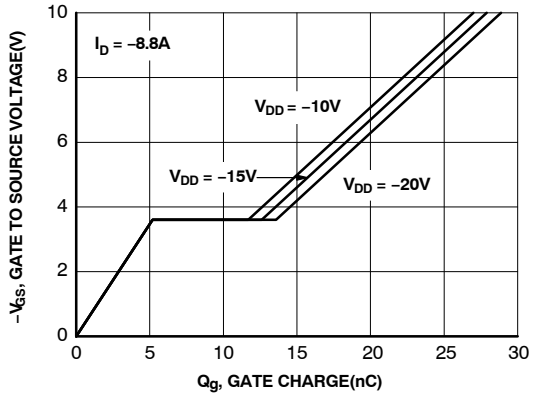


Figure 7. Gate Charge Characteristics

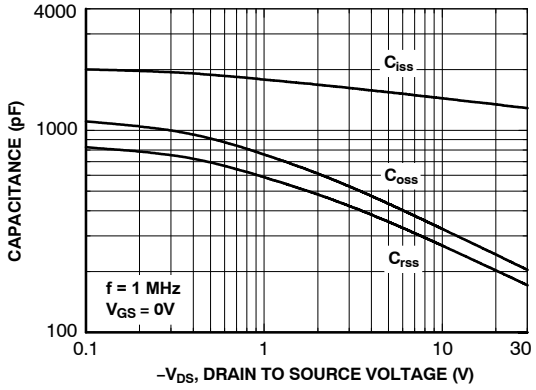


Figure 8. Capacitance vs Drain to Source Voltage

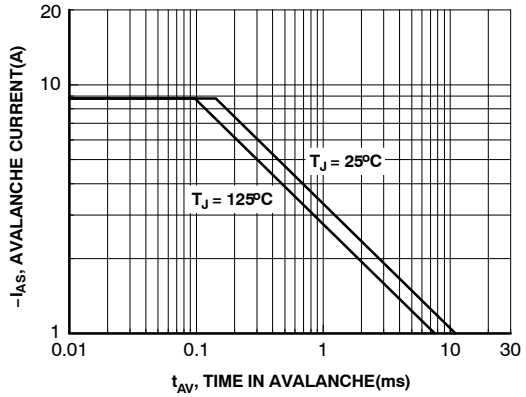


Figure 9. Unclamped Inductive Switching Capability

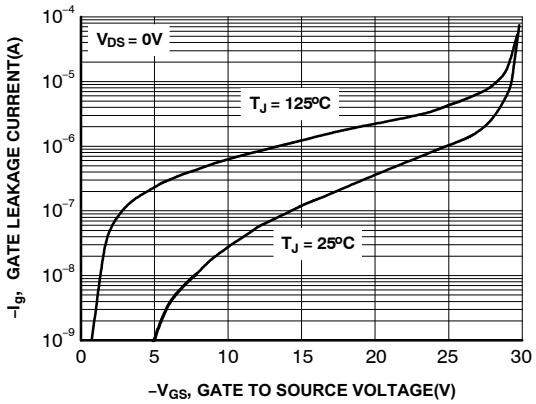


Figure 10. Gate Leakage Current vs Gate to Source Voltage

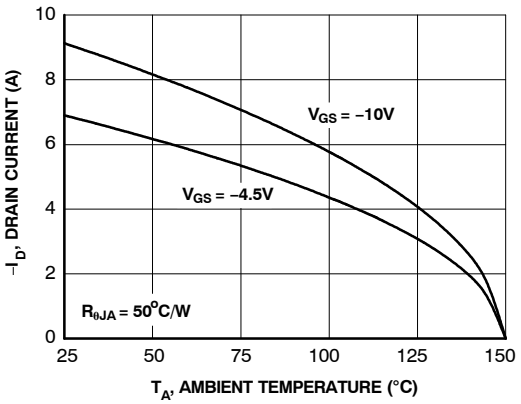


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

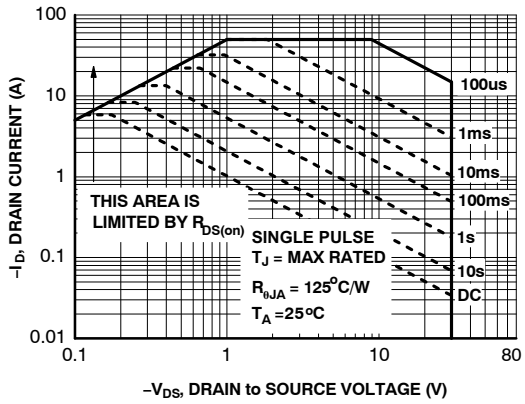


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS (Continued)

(T_J = 25°C unless otherwise noted)

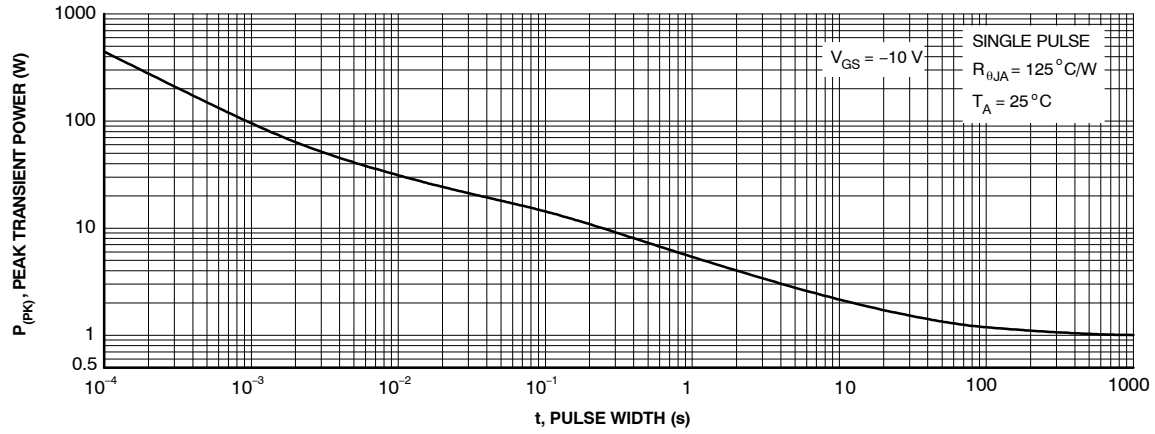


Figure 13. Single Pulse Maximum Power Dissipation

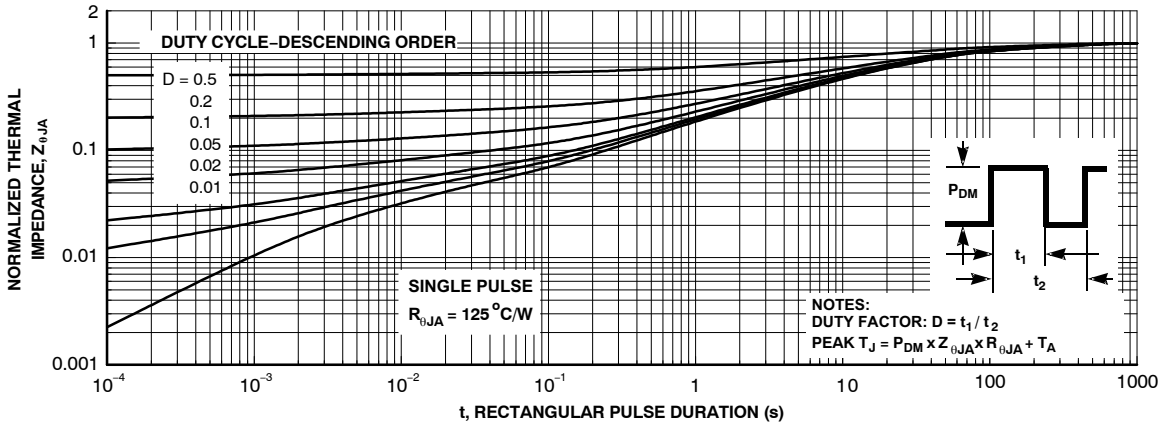


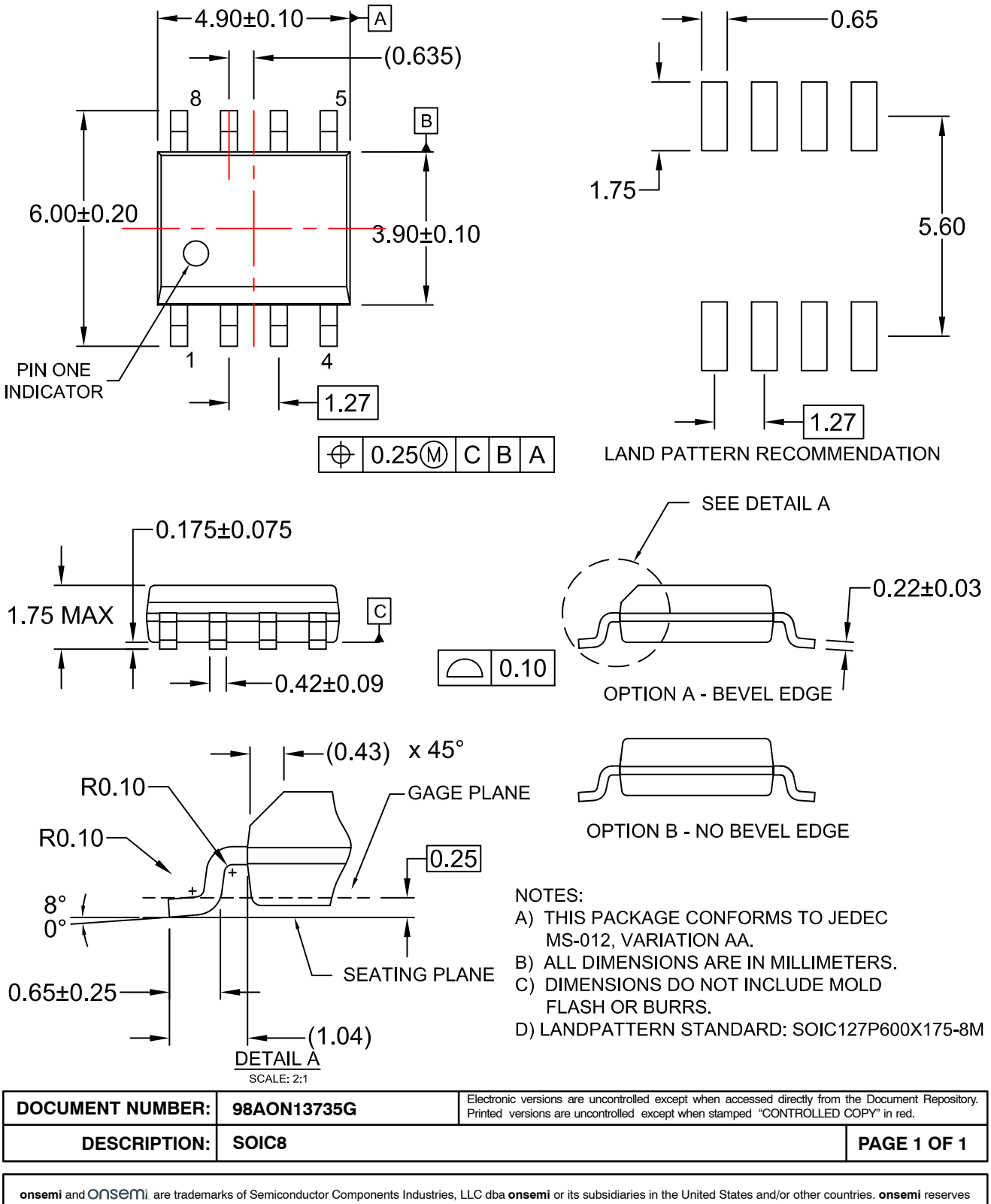
Figure 14. Junction To Ambient Transient Thermal Response Curve

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CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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