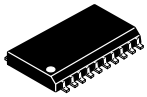
3.3 V ECL Dual Differential Data and Clock D Flip-Flop with Set and Reset

MC100LVEL29



SOIC−20 WB
DW SUFFIX
CASE 751D−05

Description

The MC100LVEL29 is a dual master-slave flip-flop. The device features fully differential Data and Clock inputs as well as outputs. The MC100LVEL29 is pin and functionally equivalent to the MC100EL29. Data enters the master latch when the clock is LOW and transfers to the slave upon a positive transition on the clock input.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE} and the $\overline{D}$ input will bias around $V_{CC}/2$. The outputs will go to a defined state, however the state will be random based on how the flip flop powers up.

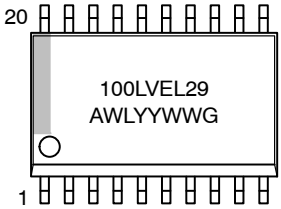
Both flip flops feature asynchronous, overriding Set and Reset inputs. Note that the Set and Reset inputs cannot both be HIGH simultaneously.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

- 1100 MHz Flip-Flop Toggle Frequency
- ESD Protection: > 2 kV Human Body Model
- 580 ps Typical Propagation Delays
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free) (For Additional Information, see Application Note AND8003/D)
- Flammability Rating: UL 94 V−0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 313 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

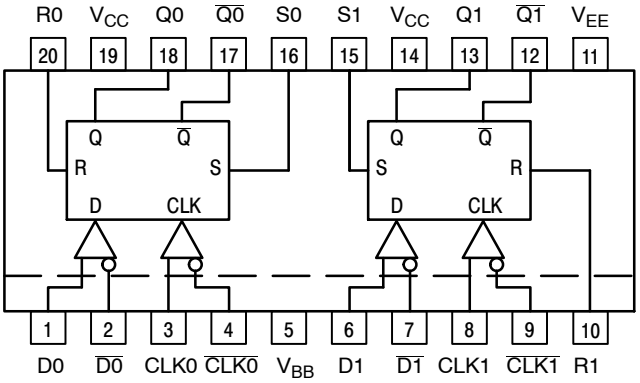
*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL29DWG	SOIC−20 WB (Pb-Free)	38 Units / Tube
MC100LVEL29DWR2G	SOIC−20 WB (Pb-Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2016



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagram and Pinout: 20-Lead SOIC (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0, $\overline{D0}$; D1, $\overline{D1}$	ECL Differential Data Inputs
R0, R1	ECL Reset Inputs
CLK0, $\overline{CLK0}$	ECL Differential Clock Inputs
CLK1, $\overline{CLK1}$	ECL Differential Clock Inputs
S0, S1	ECL Set Inputs
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Table 2. TRUTH TABLE

R	S	D	CLK	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don't Care

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 to 0 −6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC−20 WB SOIC−20 WB	90 60	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC−20 WB	30 to 35	°C/W
T_{sol}	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Share Feedback
Your Opinion Matters

Table 4. LVPECL DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		35	50		35	50		35	50	mA
V_{OH}	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3) Vpp < 500 mV Vpp ≥ 500 mV	 1.3 1.5		 2.9 2.9	 1.2 1.4		 2.9 2.9	 1.2 1.4		 2.9 2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	 0.5 −300			 0.5 −300			 0.5 −300			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 5. LVNECL DC CHARACTERISTICS (V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		35	50		35	50		35	50	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
V_{OL}	Output LOW Voltage (Note 2)	−1830	−1695	−1555	−1810	−1705	−1620	−1810	−1705	−1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{BB}	Output Voltage Reference	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3) Vpp < 500 mV Vpp ≥ 500 mV	 −2.0 −1.8		 −0.4 −0.4	 −2.1 −1.9		 −0.4 −0.4	 −2.1 −1.9		 −0.4 −0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	 0.5 −300			 0.5 −300			 0.5 −300			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Share Feedback
Your Opinion Matters

Table 6. AC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1.1			1.1			1.1			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Output S, R	480 480		680 700	500 500	580	700 720	520 520		720 740	ps
t_S t_H	Setup Time Hold Time	0 100			0 100			0 100			ps
t_{RR}	Set/Reset Recovery	100			100			100			ps
t_{PW}	Minimum Pulse Width CLK, Set, Reset	400			400			400			ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20%−80%)	280		550	280		550	280		550	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. V_{EE} can vary ±0.3 V.
2. V_{PP}(min) is the minimum input swing for which AC parameters guaranteed.

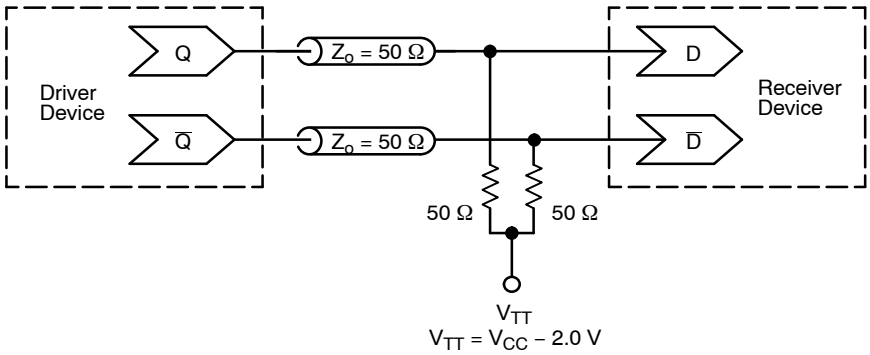


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices)

Resource Reference of Application Notes

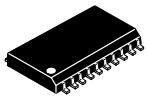
AN1405/D – ECL Clock Distribution Techniques
AN1406/D – Designing with PECL (ECL at +5.0 V)
AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D – Metastability and the ECLinPS Family
AN1568/D – Interfacing Between LVDS and ECL
AN1672/D – The ECL Translator Guide
AND8001/D – Odd Number Counters Design
AND8002/D – Marking and Date Codes
AND8020/D – Termination of ECL Logic Devices
AND8066/D – Interfacing with ECLinPS
AND8090/D – AC Characteristics of ECL Devices

ECLinPS is registered trademark of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries.

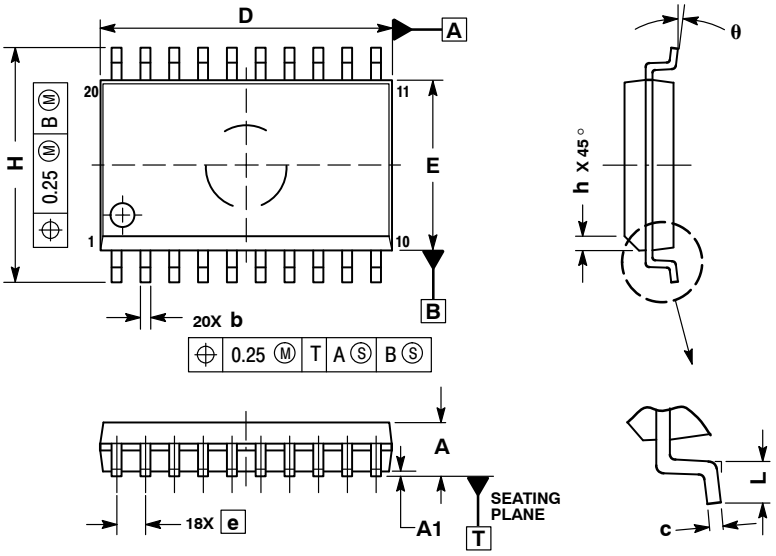
Share Feedback
Your Opinion Matters

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



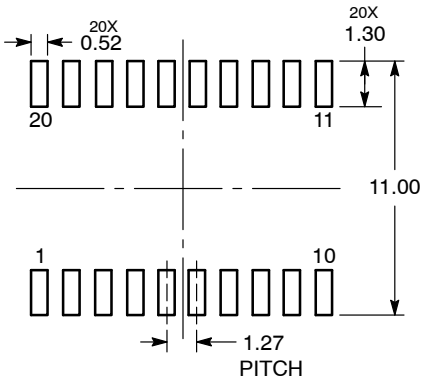
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

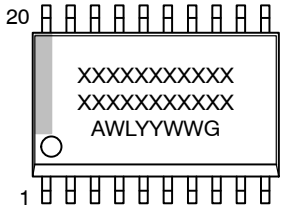
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−20 WB**		**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales