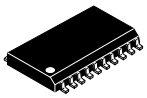
# Low-Voltage CMOS Octal Buffer

## With 5 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

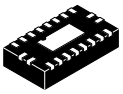
# MC74LCX244



SOIC−20 WB
DW SUFFIX
CASE 751D



TSSOP−20
DT SUFFIX
CASE 948E



QFN20
MN SUFFIX
CASES 485AA
& 485CB

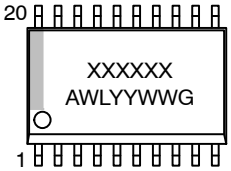
The MC74LCX244 is a high performance, non−inverting octal buffer operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $V_I$ specification of 5.5 V allows MC74LCX244 inputs to be safely driven from 5 V devices. The MC74LCX244 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs. The Output Enable ($\overline{OE}$) input, when HIGH, disables the output by placing them in a HIGH Z condition.

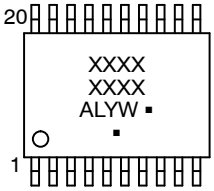
### Features

- Designed for 1.65 to 5.5 V $V_{CC}$ Operation
- 5 V Tolerant − Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$ Specification Guarantees High Impedance When $V_{CC}$ = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - ♦ Human Body Model >2000 V
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

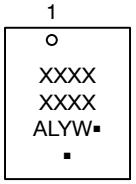
### MARKING DIAGRAMS



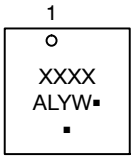

SOIC−20 WB




TSSOP−20




QFN20 − 485AA




QFN20 − 485CB

| | | |
|---|---|---|
| A | = | Assembly Location |
| L, WL | = | Wafer Lot |
| Y, YY | = | Year |
| W, WW | = | Work Week |
| G or ▪ | = | Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.

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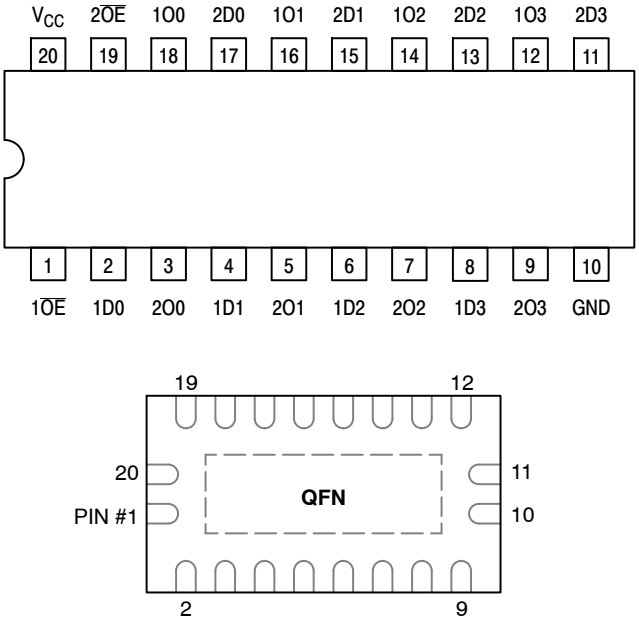



**Figure 1. Pinouts: 20−Lead** (Top View)

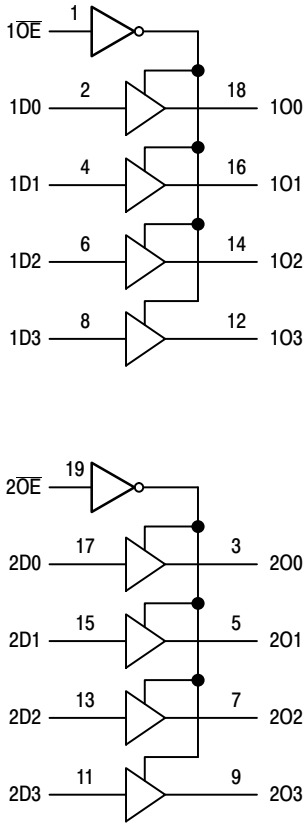



**Figure 2. Logic Diagram**

**PIN NAMES**

| PINS | FUNCTION |
|---|---|
| n$\overline{OE}$ | Output Enable Inputs |
| 1Dn, 2Dn | Data Inputs |
| 1On, 2On | 3−State Outputs |

**TRUTH TABLE**

| INPUTS | | OUTPUTS |
|---|---|---|
| **1$\overline{OE}$ 2$\overline{OE}$** | **1Dn 2Dn** | **1On, 2On** |
| L | L | L |
| L | H | H |
| H | X | Z |

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions are Acceptable
For $I_{CC}$ reasons, DO NOT FLOAT Inputs


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## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_I$ | DC Input Voltage (Note 1) | | −0.5 to +6.5 | V |
| $V_O$ | DC Output Voltage (Note 1) | Active−Mode (High or Low State) | −0.5 to $V_{CC}$ + 0.5 | V |
| | | Tri−State Mode | −0.5 to +6.5 | |
| | | Power−Down Mode ($V_{CC}$ = 0 V) | −0.5 to +6.5 | |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < GND | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < GND | −50 | mA |
| $I_O$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ or $I_{GND}$ | DC Supply Current per Supply Pin or Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | SOIC−20W | 96 | °C/W |
| | | WQFN20 | 99 | |
| | | QFN20 | 111 | |
| | | TSSOP−20 | 150 | |
| $P_D$ | Power Dissipation in Still Air | SOIC−20W | 1302 | mW |
| | | WQFN20 | 1256 | |
| | | QFN20 | 1127 | |
| | | TSSOP−20 | 833 | |
| MSL | Moisture Sensitivity | SOIC−20W | Level 3 | − |
| | | All Other Packages | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | − |
| $V_{ESD}$ | ESD Withstand Voltage (Note 3) | Human Body Model | > 2000 | V |
| | | Charged Device Model | N/A | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_O$ absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.



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## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating | 1.65 | 3.3 | 5.5 | V |
| | | Data Retention Only | 1.5 | 3.3 | 5.5 | |
| $V_I$ | Digital Input Voltage | | 0 | – | 5.5 | V |
| $V_O$ | Output Voltage | Active Mode (High or Low State) | 0 | – | $V_{CC}$ | V |
| | | Tri–State Mode | 0 | – | 5.5 | |
| | | Power Down Mode ($V_{CC}$ = 0 V) | 0 | – | 5.5 | |
| $T_A$ | Operating Free–Air Temperature | | –55 | – | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Rate | $V_{CC}$ = 1.65 V to 1.95 V | 0 | – | 20 | nS/V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0 | – | 20 | |
| | | $V_I$ from 0.8 V to 2.0 V, $V_{CC}$ = 3.0 V | 0 | – | 10 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0 | – | 5 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = –40°C to +85°C | | $T_A$ = –55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $V_{IH}$ | High–Level Input Voltage | | 1.65 to 1.95 | 0.65 x $V_{CC}$ | | 0.65 x $V_{CC}$ | | V |
| | | | 2.3 to 2.7 | 1.7 | | 1.7 | | |
| | | | 2.7 to 3.6 | 2.0 | | 2.0 | | |
| | | | 4.5 to 5.5 | 0.7 x $V_{CC}$ | | 0.7 x $V_{CC}$ | | |
| $V_{IL}$ | Low–Level Input Voltage | | 1.65 to 1.95 | | 0.35 x $V_{CC}$ | | 0.35 x $V_{CC}$ | V |
| | | | 2.3 to 2.7 | | 0.7 | | 0.7 | |
| | | | 2.7 to 3.6 | | 0.8 | | 0.8 | |
| | | | 4.5 to 5.5 | | 0.3 x $V_{CC}$ | | 0.3 x $V_{CC}$ | |
| $V_{OH}$ | High–Level Output Voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | V |
| | | $I_{OH}$ = –100 μA | 1.65 to 5.5 | $V_{CC}$ – 0.1 | – | $V_{CC}$ – 0.1 | – | |
| | | $I_{OH}$ = –4 mA | 1.65 | 1.2 | – | 1.2 | – | |
| | | $I_{OH}$ = –8 mA | 2.3 | 1.8 | – | 1.8 | – | |
| | | $I_{OH}$ = –12 mA | 2.7 | 2.2 | – | 2.2 | – | |
| | | $I_{OH}$ = –16 mA | 3.0 | 2.4 | – | 2.4 | – | |
| | | $I_{OH}$ = –24 mA | 3.0 | 2.2 | – | 2.2 | – | |
| | | $I_{OH}$ = –32 mA | 4.5 | 3.8 | | 3.8 | | |
| $V_{OL}$ | Low–Level Output Voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | V |
| | | $I_{OL}$ = 100 μA | 1.65 to 5.5 | – | 0.1 | – | 0.1 | |
| | | $I_{OL}$ = 4 mA | 1.65 | – | 0.45 | – | 0.45 | |
| | | $I_{OL}$ = 8 mA | 2.3 | – | 0.6 | – | 0.6 | |
| | | $I_{OL}$ = 12 mA | 2.7 | – | 0.4 | – | 0.4 | |
| | | $I_{OL}$ = 16 mA | 3.0 | – | 0.4 | – | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | – | 0.55 | – | 0.55 | |
| | | $I_{OL}$ = 32 mA | 4.5 | | 0.6 | | 0.6 | |



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## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40°C to +85°C | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $I_I$ | Input Leakage Current | $V_I$ = 0 to 5.5 V | 3.6 | – | ±5.0 | – | ±5.0 | μA |
| $I_{OZ}$ | 3−State Output Leakage Current | $V_I = V_{IH}$ or $V_{IL}$, $V_O$ = 0 V to 5.5 V | 3.6 | – | ±5.0 | – | ±5.0 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_I$ = 5.5 V or $V_O$ = 5.5 V | 0 | – | 10 | – | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_I$ = 5.5 V or GND | 3.6 | – | 10 | – | 10 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH} = V_{CC}$ − 0.6 V | 2.3 to 3.6 | – | 500 | – | 500 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These values of $V_I$ are used to test DC electrical characteristics only.

## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | $V_{CC}$ (V) | $T_A$ = −40°C to +85°C | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, D to O | See Figures 3 and 4 | 1.65 to 1.95 | – | 10.3 | – | 10.3 | ns |
| | | | 2.3 to 2.7 | – | 7.8 | – | 7.8 | |
| | | | 2.7 | – | 7.5 | – | 7.5 | |
| | | | 3.0 to 3.6 | – | 6.5 | – | 6.5 | |
| | | | 4.5 to 5.5 | – | 5.9 | – | 5.9 | |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time,OE to $\overline{OE}$ to O | See Figures 3 and 4 | 1.65 to 1.95 | – | 13.0 | – | 13.0 | ns |
| | | | 2.3 to 2.7 | – | 10.0 | – | 10.0 | |
| | | | 2.7 | – | 9.0 | – | 9.0 | |
| | | | 3.0 to 3.6 | – | 8.0 | – | 8.0 | |
| | | | 4.5 to 5.5 | – | 7.3 | – | 7.3 | |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time, $\overline{OE}$ to O | See Figures 3 and 4 | 1.65 to 1.95 | – | 11.0 | – | 11.0 | ns |
| | | | 2.3 to 2.7 | – | 8.4 | – | 8.4 | |
| | | | 2.7 | – | 8.0 | – | 8.0 | |
| | | | 3.0 to 3.6 | – | 7.0 | – | 7.0 | |
| | | | 4.5 to 5.5 | – | 6.0 | – | 6.0 | |
| $t_{OSHL}$, $t_{OSLH}$ | Output to Output Skew (Note 5) | | 1.65 to 1.95 | – | – | – | – | ns |
| | | | 2.3 to 2.7 | – | – | – | – | |
| | | | 2.7 | – | – | – | – | |
| | | | 3.0 to 3.6 | – | 1.0 | – | 1.0 | |

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW ($t_{OSHL}$) or LOW−to−HIGH ($t_{OSLH}$); parameter guaranteed by design.



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## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A$ = +25°C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 7) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | 0.8<br>0.6 | | V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 7) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | −0.8<br>−0.6 | | V |

7. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

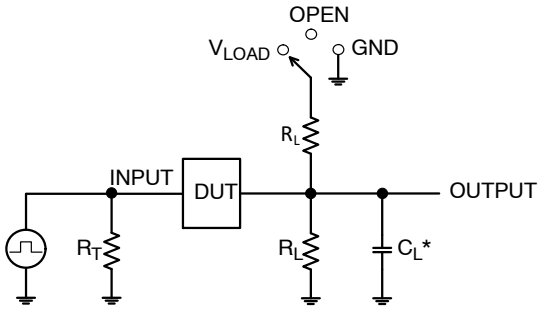
## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typ | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 8) | 10 MHz, $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 25 | pF |

8. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC2} \bullet f_{in} + I_{CC} \bullet V_{CC}$.



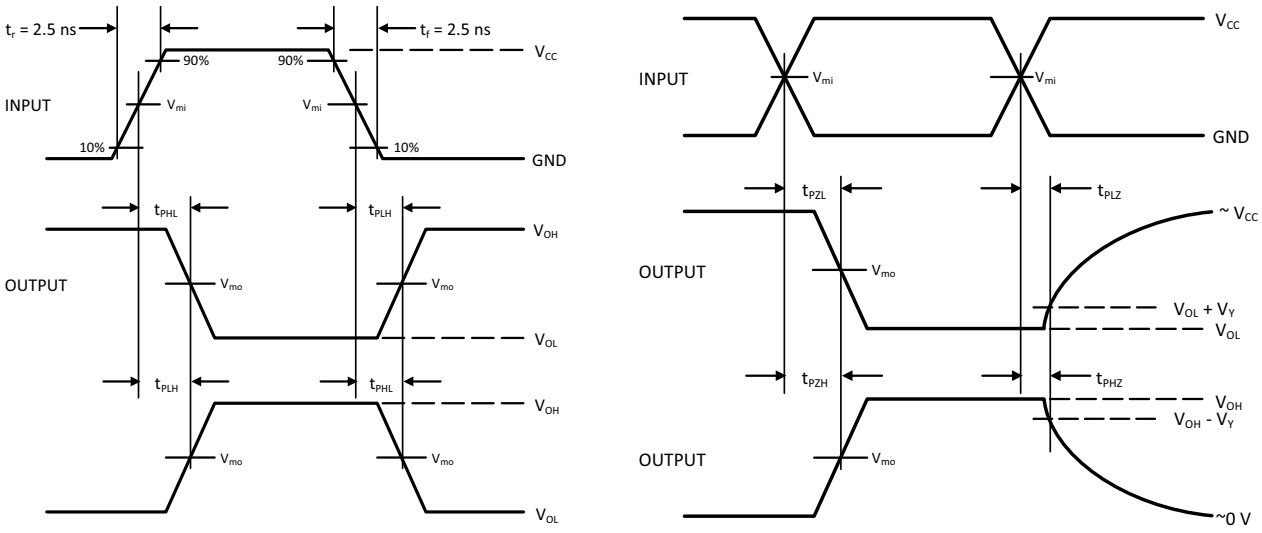
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| Test | Switch Position |
|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}$ / $t_{PZH}$ | GND |

$C_L$ includes probe and jig capacitance
$R_T$ is $Z_{OUT}$ of pulse generator (typically 50 Ω)
f = 1 MHz

**Figure 3. Test Circuit**




| $V_{CC}$, V | $R_L$, Ω | $C_L$, pF | $V_{LOAD}$ | $V_{mi}$, V | $V_{mo}$, V | $V_Y$, V |
|---|---|---|---|---|---|---|
| 1.65 to 1.95 | 500 | 30 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.15 |
| 2.3 to 2.7 | 500 | 30 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.15 |
| 2.7 | 500 | 50 | 6 V | 1.5 | $V_{CC}$/2 | 0.3 |
| 3.0 to 3.6 | 500 | 50 | 6 V | 1.5 | $V_{CC}$/2 | 0.3 |
| 4.5 to 4.5 | 500 | 50 | 2 x $V_{CC}$ | $V_{CC}$/2 | $V_{CC}$/2 | 0.3 |

**Figure 4. Switching Waveforms**


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## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MC74LCX244DWG | LCX244 | SOIC−20 WB | 38 Units / Rail |
| MC74LCX244DWR2G | LCX244 | SOIC−20 WB | 1000 / Tape & Reel |
| MC74LCX244DTG | LCX<br>244 | TSSOP−20 | 75 Units / Rail |
| MC74LCX244DTR2G | LCX<br>244 | TSSOP−20 | 2500 / Tape & Reel |
| MC74LCX244DTR2G−Q* | LCX<br>244 | TSSOP−20 | 2500 / Tape & Reel |
| MC74LCX244MNTWG | LCX<br>244 | QFN20, 2.5x4.5 | 3000 / Tape & Reel<br>(4 mm pitch carrier tape) |

**DISCONTINUED** (Note 9)

| | | | |
|---|---|---|---|
| NLV74LCX244DTR2G* | | TSSOP−20<br>(Pb−Free) | 2500 / Tape & Reel |
| MC74LCX244MN2TWG | | QFN20, 2.5x3.5<br>(Pb−Free) | 3000 / Tape & Reel<br>(4 mm pitch carrier tape) |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffx for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

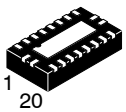
9. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



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# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

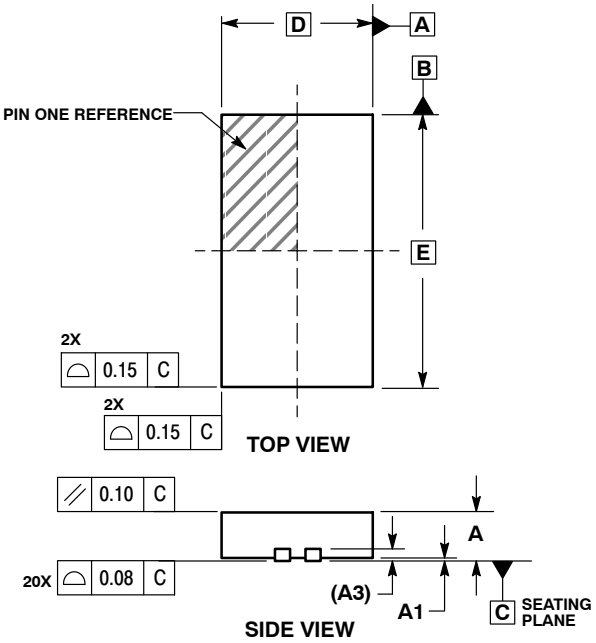
ON Semiconductor®




**SCALE 2:1**

**QFN20, 2.5x4.5 MM**
CASE 485AA−01
ISSUE B

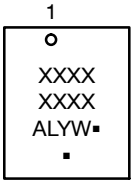
DATE 30 APR 2010




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.50 BSC | |
| D2 | 0.85 | 1.15 |
| E | 4.50 BSC | |
| E2 | 2.85 | 3.15 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |

### GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON12653D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **QFN20. 2.5X4.5 MM** | **PAGE 1 OF 1** |

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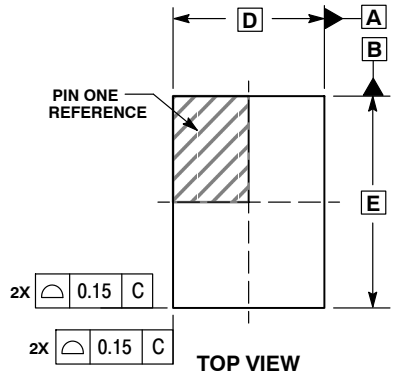
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**QFN20, 2.5x3.5, 0.4P**
CASE 485CB
ISSUE O

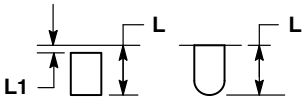
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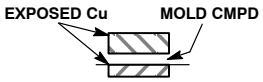
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**TOP VIEW**



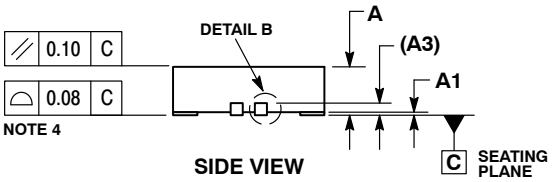

**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**



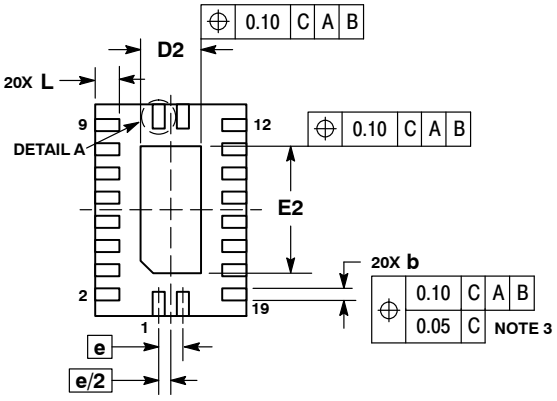

**DETAIL B**
**ALTERNATE CONSTRUCTIONS**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.15 | 0.25 |
| D | 2.50 BSC | |
| D2 | 0.90 | 1.10 |
| E | 3.50 BSC | |
| E2 | 2.00 | 2.20 |
| e | 0.40 BSC | |
| L | 0.35 | 0.45 |
| L1 | --- | 0.15 |




**SIDE VIEW**




**BOTTOM VIEW**

## GENERIC MARKING DIAGRAM*

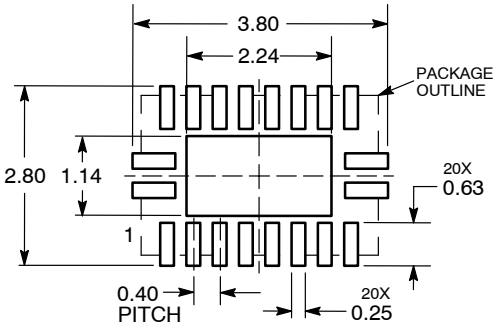



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

## SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

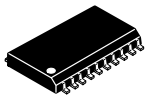
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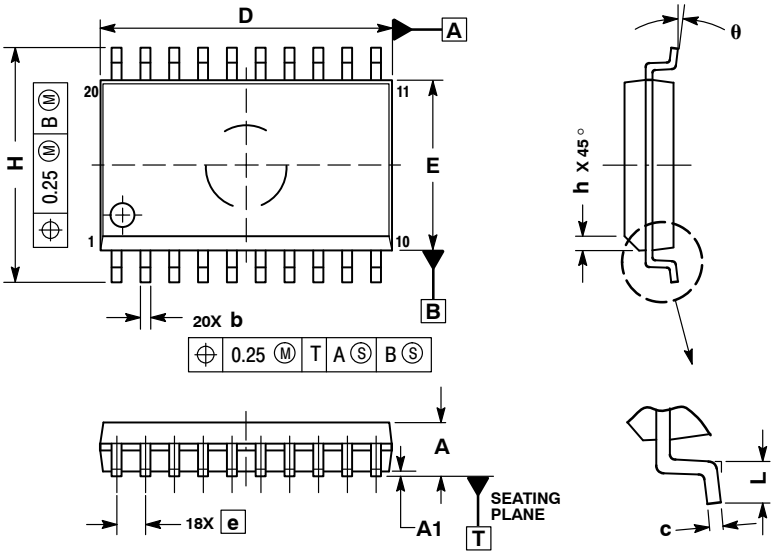
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**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



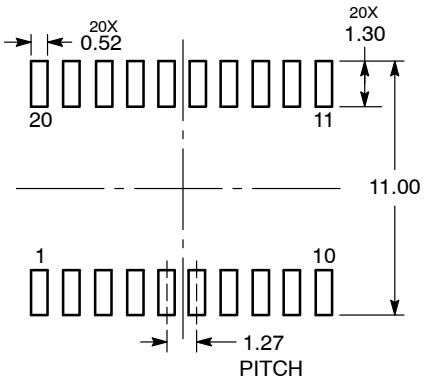
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

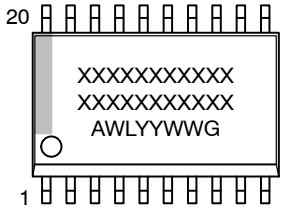
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
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