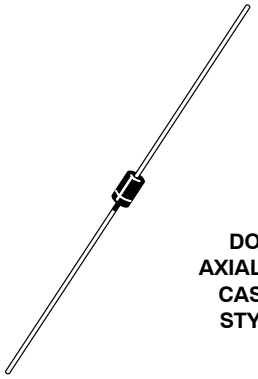
Axial Lead Rectifier

MBR1100

SCHOTTKY BARRIER RECTIFIER 1.0 AMPERE, 100 VOLTS

These rectifiers employ the Schottky Barrier principle in a large area metal−to−silicon power diode. State−of−the−art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low−voltage, high−frequency inverters, free wheeling diodes, and polarity protection diodes.



DO−41
AXIAL LEAD
CASE 59
STYLE 1

Features

- Low Reverse Current
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency
- Highly Stable Oxide Passivated Junction
- Guard−Ring for Stress Protection
- Low Forward Voltage
- 175°C Operating Junction Temperature
- High Surge Capacity
- These Devices are Pb−Free and are RoHS Compliant

Mechanical Characteristics:

- Case: Epoxy, Molded
- Weight: 0.4 Gram (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Polarity: Cathode Indicated by Polarity Band

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{RRM} V_{RWM} V_R	Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	100	V
I_O	Average Rectified Forward Current ($V_{R(equiv)} \le 0.2\ V_R$ (dc), $R_{\theta JA}$ = 50°C/W, P.C. Board Mounting, [see Note 3], T_A = 120°C)	1.0	A
I_{FRM}	Peak Repetitive Forward Current ($V_{R(equiv)} \le 0.2\ V_R$ (dc), $R_{\theta JA}$ = 50°C/W, P.C. Board Mounting, [see Note 3], T_A = 110°C)	2.0	A
I_{FSM}	Non−Repetitive Peak Surge Current (Surge Applied at Rated Load Conditions Halfwave, Single Phase, 60 Hz)	50	A
T_J, T_{stg}	Operating and Storage Junction Temperature Range (Note 1)	−65 to +175	°C
dv/dt	Voltage Rate of Change (Rated V_R)	10	V/ns

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The heat generated must be less than the thermal conductivity from Junction−to−Ambient: $dP_D/dT_J < 1/R_{\theta JA}$.

ORDERING INFORMATION

Device	Package	Shipping†
MBR1100G	Axial Lead (Pb−Free)	1000 Units/Bag
MBR1100RLG	Axial Lead (Pb−Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS (See Note 4)

Symbol	Characteristic	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	See Note 3	°C/W

ELECTRICAL CHARACTERISTICS (T_L = 25°C unless otherwise noted)

Symbol	Characteristic	Max	Unit
V_F	Maximum Instantaneous Forward Voltage (Note 2) (i_F = 1 A, T_L = 25°C) (i_F = 1 A, T_L = 100°C)	 0.79 0.69	V
i_R	Maximum Instantaneous Reverse Current @ Rated dc Voltage (Note 2) (T_L = 25°C) (T_L = 100°C)	 0.5 5.0	mA

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

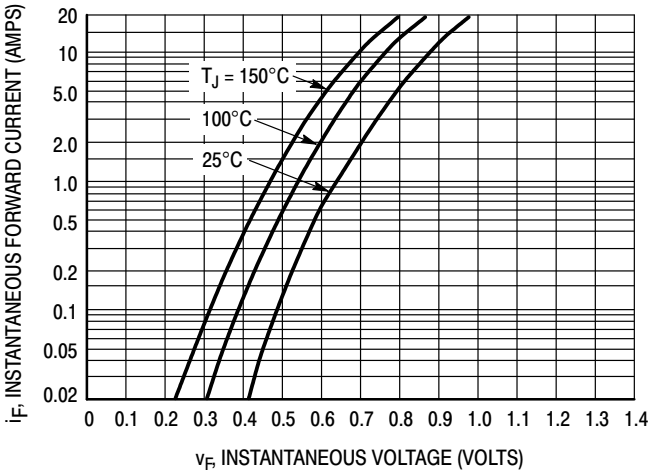


Figure 1. Typical Forward Voltage

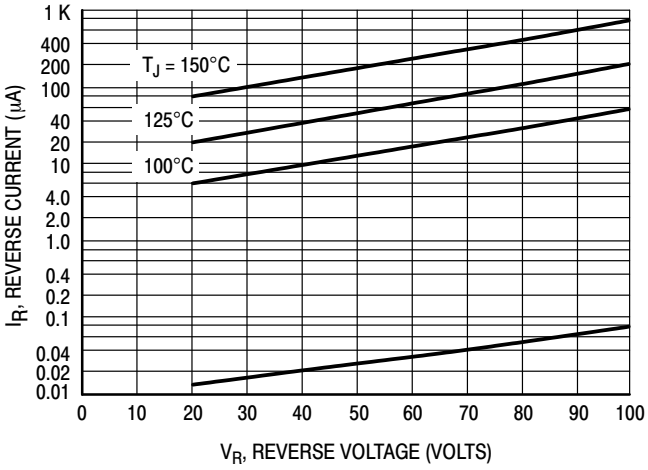


Figure 2. Typical Reverse Current †

† The curves shown are typical for the highest voltage device in the voltage grouping. Typical reverse current for lower voltage selections can be estimated from these same curves if V_R is sufficiently below rated V_R.

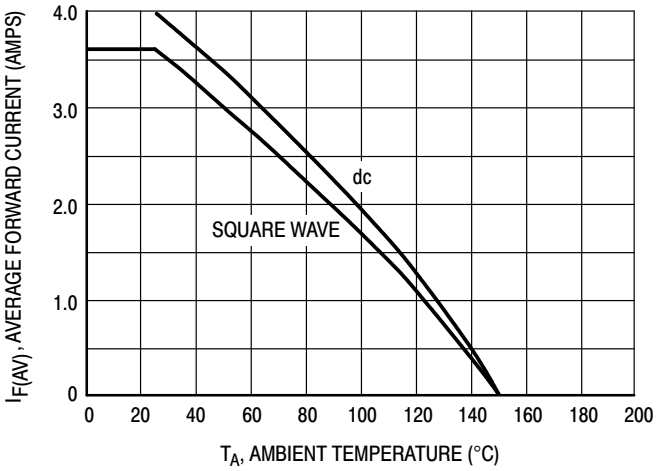


Figure 3. Current Derating (Mounting Method 3 per Note 3)

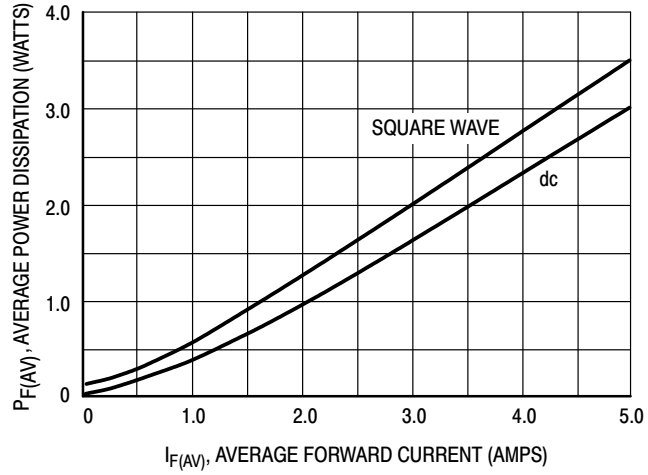


Figure 4. Power Dissipation

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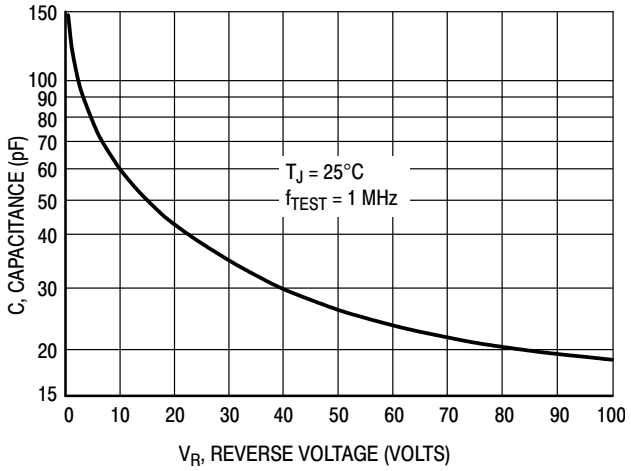


Figure 5. Typical Capacitance

NOTE 3 — MOUNTING DATA:

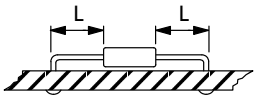
Data shown for thermal resistance junction−to−ambient ($R_{\theta JA}$) for the mounting shown is to be used as a typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

Typical Values for $R_{\theta JA}$ in Still Air

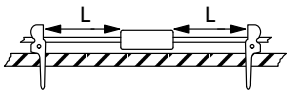
Mounting Method	Lead Length, L (in)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	52	65	72	85	°C/W
2	67	80	87	100	°C/W
3	—	50			°C/W

Mounting Method 1

P.C. Board with 1−1/2″ x 1−1/2″ copper surface.

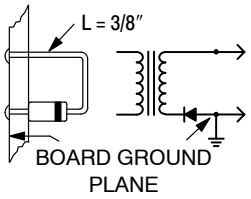


Mounting Method 2



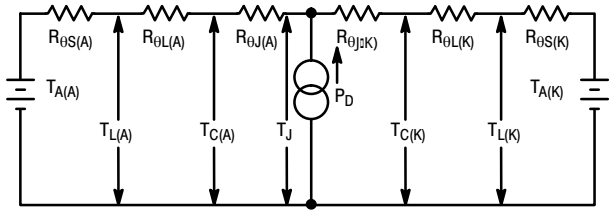
Mounting Method 3

P.C. Board with 1−1/2″ x 1−1/2″ copper surface.



NOTE 4 — THERMAL CIRCUIT MODEL:

(For heat conduction through the leads)



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature T_C = Case Temperature
T_L = Lead Temperature T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides, respectively.) Values for thermal resistance components are:
$R_{\theta L}$ = 100°C/W/in typically and 120°C/W/in maximum.
$R_{\theta J}$ = 36°C/W typically and 46°C/W maximum.

NOTE 5 — HIGH FREQUENCY OPERATION:

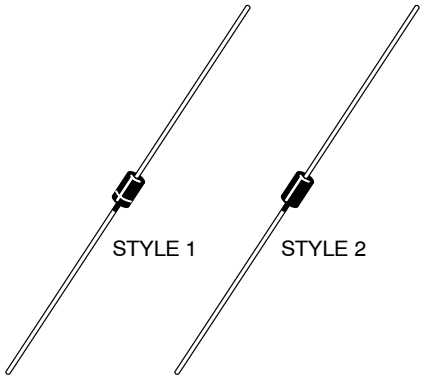
Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 5)

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 percent at 2 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss: it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

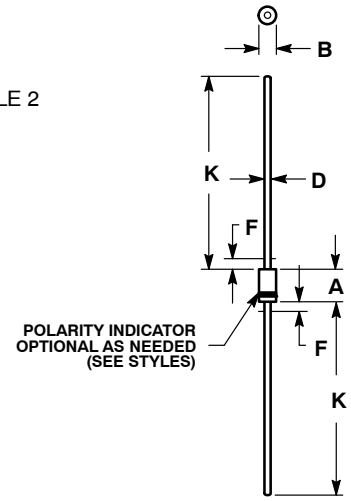
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AXIAL LEAD
CASE 59−10
ISSUE U

DATE 15 FEB 2005



SCALE 1:1



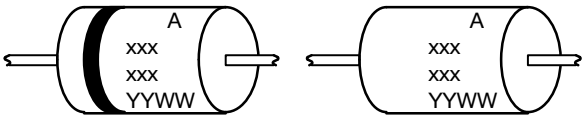
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO−41 OUTLINE SHALL APPLY
4. POLARITY DENOTED BY CATHODE BAND.
5. LEAD DIAMETER NOT CONTROLLED WITHIN F DIMENSION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.161	0.205	4.10	5.20
B	0.079	0.106	2.00	2.70
D	0.028	0.034	0.71	0.86
F	−−−	0.050	−−−	1.27
K	1.000	−−−	25.40	−−−

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

GENERIC MARKING DIAGRAM*



STYLE 1 STYLE 2

xxx = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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