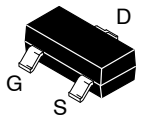
P-Channel Enhancement Mode Field Effect Transistor

NDS0605



SOT−23 (TO−236)
CASE 318

General Description

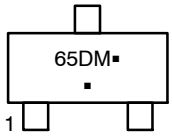
These P −Channel enhancement mode field effect transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on−state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 180 mA DC and can deliver current up to 1 A.

This product is particularly suited to low voltage applications requiring a low current high side switch.

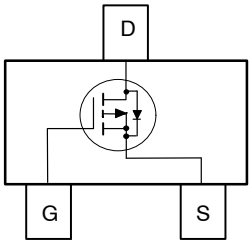
Features

- −0.18 A, −60 V
  - $R_{DS(on)}$ = 5 Ω @ V_{GS} = −10 V
- Voltage Controlled P−Channel Small Signal Switch
- High Density Cell Design for Low $R_{DS(on)}$
- High Saturation Current
- This Device is Pb−Free, Halide Free and is RoHS Compliant

MARKING DIAGRAM



65D = Specific Device Code
M = Date Code
▪ = Pb−Free Package



P−Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted.

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain−Source Voltage	−60	V
V_{GSS}	Gate−Source Voltage	±20	V
I_D	Drain Current − Continuous (Note 1)	−0.18	A
	Drain Current − Pulsed	−1	
P_D	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.9	mW/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1)	350	°C/W

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 350°C/W when mounted on a minimum pad.

ORDERING INFORMATION

Device	Package	Shipping†
NDS0605	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = −10 μA	−60	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = −10 μA, Referenced to 25°C	–	−53	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −48 V, V_{GS} = 0 V	–	–	−1	μA
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 125°C	–	–	−500	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−1	−1.7	−3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	3	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = −10 V, I_D = −0.5 A	–	1.0	5.0	Ω
		V_{GS} = −4.5 V, I_D = −0.25 A	–	1.3	7.5	
		V_{GS} = −10 V, I_D = −0.5 A, T_J = 125°C	–	1.7	10	
$I_{D(on)}$	On–State Drain Current	V_{GS} = −10 V, V_{DS} = −10 V	−0.6	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = −10 V, I_D = −0.2 A	0.07	0.43	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −25 V, V_{GS} = 0 V, f = 1.0 MHz	–	79	–	pF
C_{oss}	Output Capacitance		–	10	–	pF
C_{rss}	Reverse Transfer Capacitance		–	4	–	pF
R_G	Gate Resistance	V_{GS} = −15 mV, f = 1.0 MHz	–	10	–	Ω
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = −25 V, I_D = −0.2 A, V_{GS} = −10 V, R_{GEN} = 6 Ω	–	2.5	5	ns
t_r	Turn–On Rise Time		–	6.3	12.6	ns
$t_{d(off)}$	Turn–Off Delay Time		–	10	20	ns
t_f	Turn–Off Fall Time		–	7.5	15	ns
Q_g	Total Gate Charge	V_{DS} = −48 V, I_D = −0.5 A, V_{GS} = −10 V	–	1.8	2.5	nC
Q_{gs}	Gate–Source Charge		–	0.3	–	nC
Q_{gd}	Gate–Drain Charge		–	0.4	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	−0.18	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −0.5 A (Note 2)	–	−0.8	−1.5	V
t_{rr}	Diode Reverse Recovery Time	I_F = −0.5 A, d_{IF}/d_t = 100 A/μs (Note 2)	–	17	–	ns
Q_{rr}	Diode Reverse Recovery Charge		–	15	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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TYPICAL CHARACTERISTICS

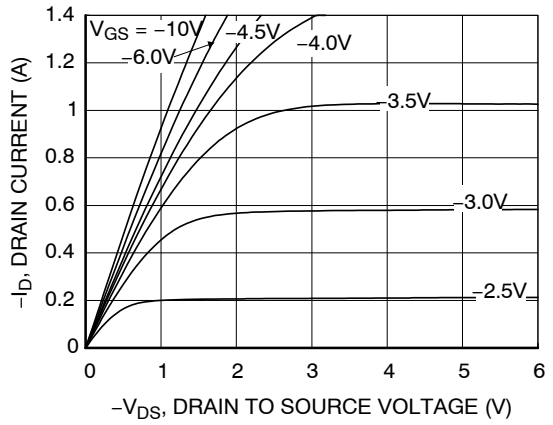

Figure 1. On−Region Characteristics

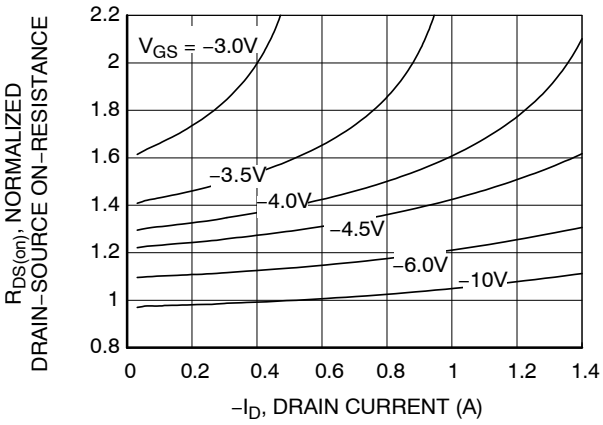

Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

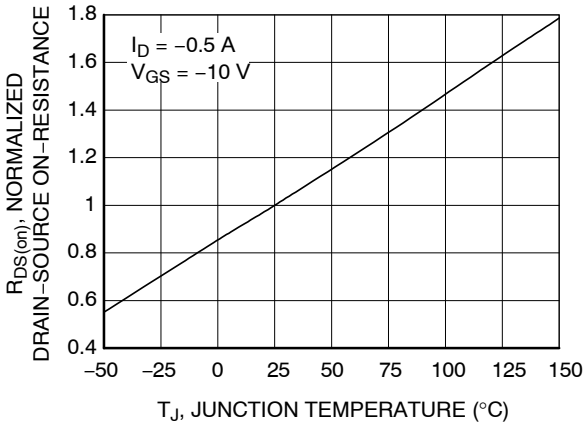

Figure 3. On−Resistance Variation with Temperature

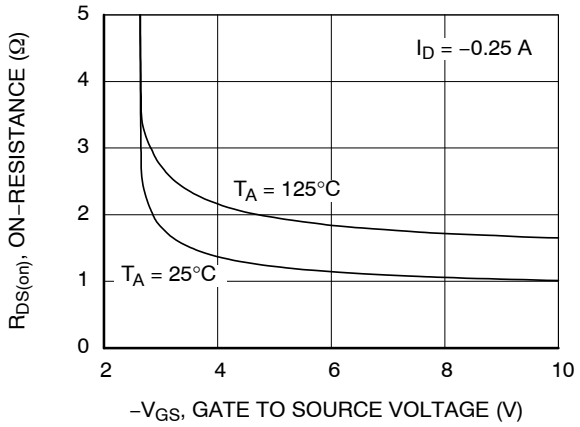

Figure 4. On−Resistance Variation with Gate to Source Voltage

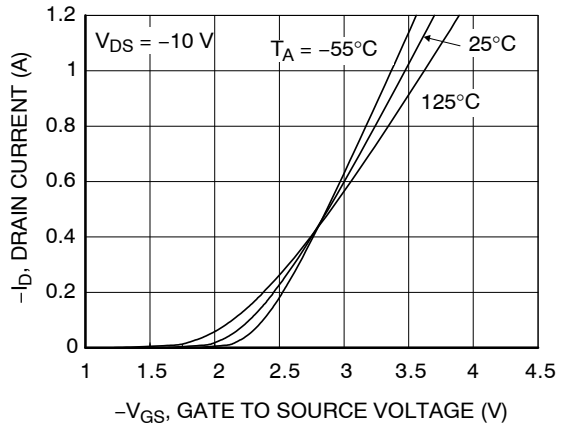

Figure 5. Transfer Characteristics

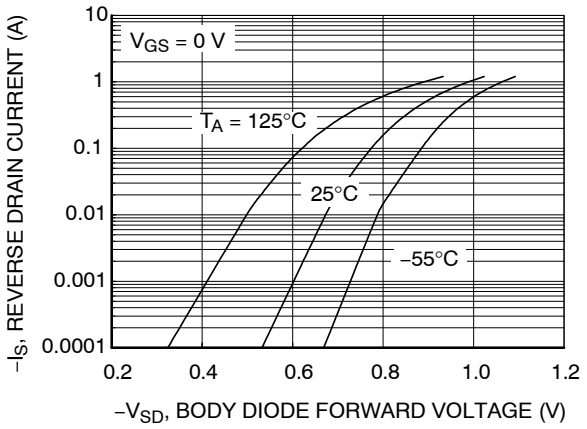

Figure 6. Body Diode Forward Voltage Variation with Source Current and temperature

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TYPICAL CHARACTERISTICS (continued)

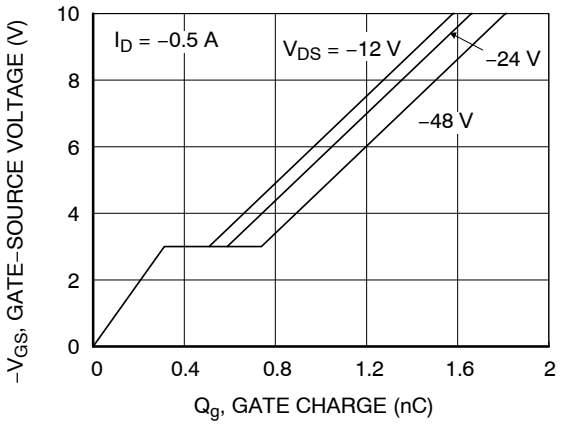

Figure 7. Gate Charge Characteristics

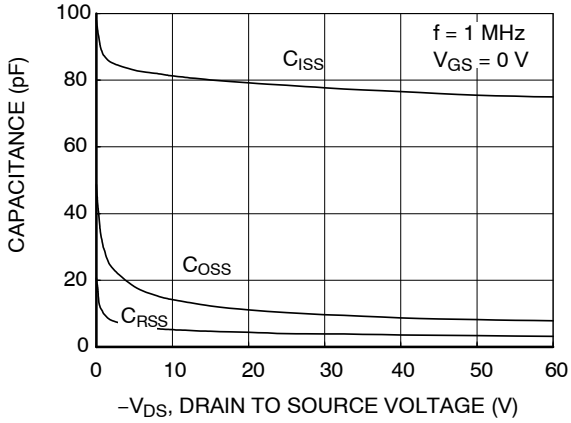

Figure 8. Capacitance Characteristics

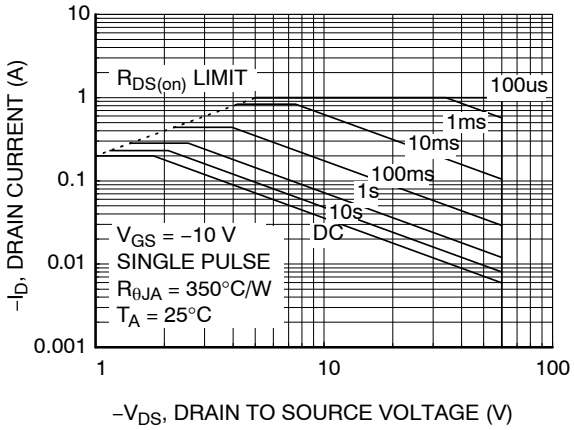

Figure 9. Maximum Safe Operating Area

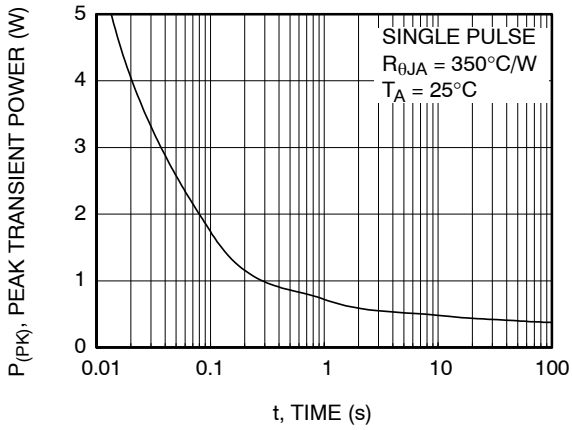

Figure 10. Single Pulse Maximum Power Dissipation

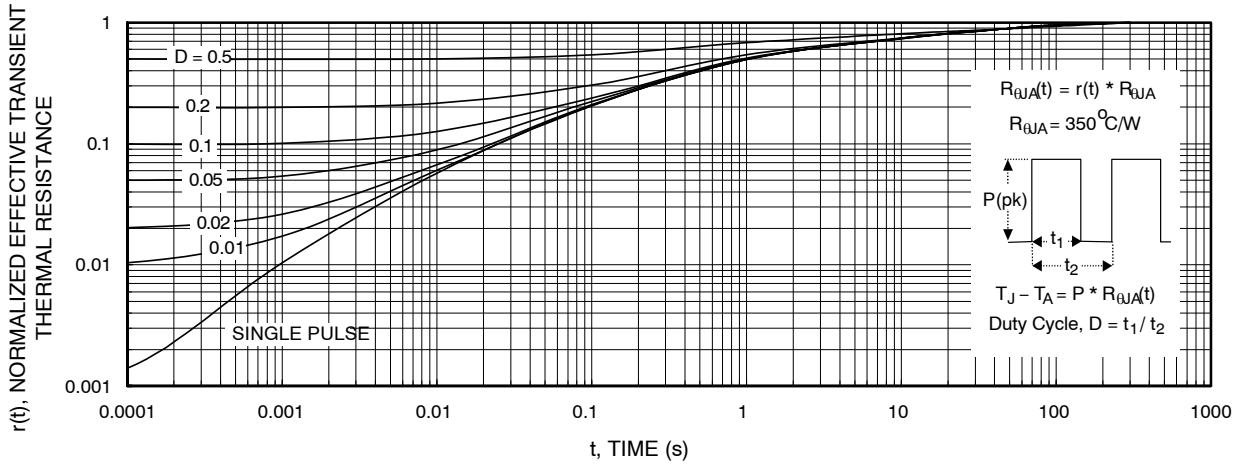

Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1a.
Transient thermal response will change depending on the circuit board design.

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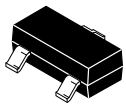
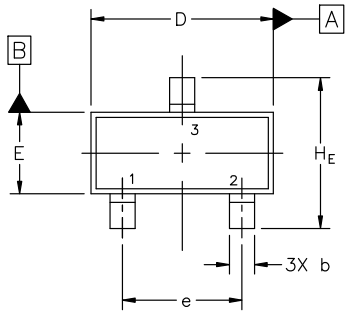


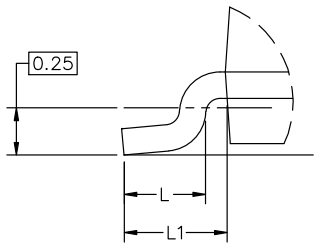
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

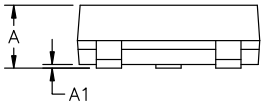
DATE 14 AUG 2024



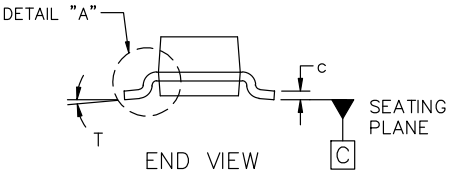
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

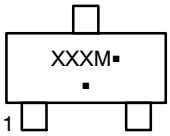


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

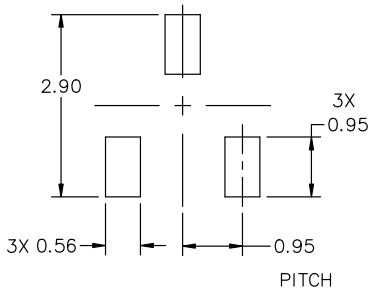
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**		**PAGE 1 OF 2**

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CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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