Quad 3-State Noninverting Buffers

High−Performance Silicon−Gate CMOS

MC74HC125A, MC74HCT125A, MC74HC126A

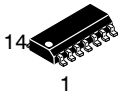
The MC74HC125A/MC74HCT125A and MC74HC126A are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT125A device inputs are compatible with Standard CMOS or TTL outputs.

The HC125A and HC126A noninverting buffers are designed to be used with 3−state memory address drivers, clock drivers, and other bus−oriented systems. The devices have four separate output enables that are active−low (HC125A) or active−high (HC126A).

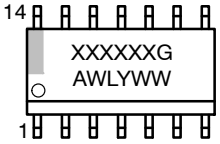
Features

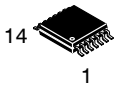
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS

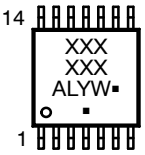


SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G



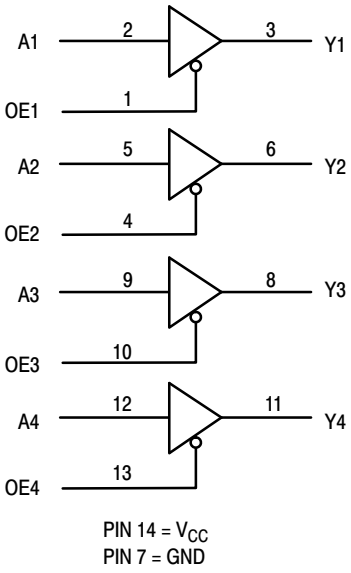
XXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
Ww, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

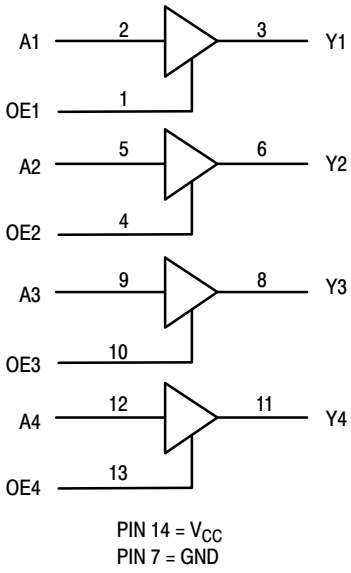
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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125A – Active–Low Output Enables



126A – Active–High Output Enables

Figure 1. Logic Diagrams

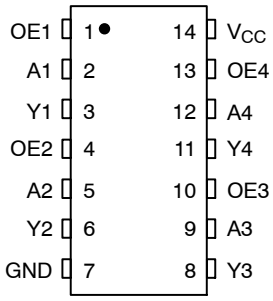


Figure 2. Pinout Diagram

FUNCTION TABLE

125A		
Inputs		Output
A	OE	Y
H	L	H
L	L	L
X	H	Z

126A		
Inputs		Output
A	OE	Y
H	H	H
L	H	L
X	L	Z

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +6.5	V
V_{IN}	DC Input Voltage		–0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage		–0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		±150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC–14 TSSOP–14	116 150	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC–14 TSSOP–14	1077 833	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	>2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm–by–114mm, 2–ounce copper trace no air flow per JESD51–7.
2. HBM tested to EIA / JESD22–A114–A. CDM tested to JESD22–C101–A. JEDEC recommends that ESD qualification to EIA/JESD22–A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74HC					
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND) (Note 3)		0	V_{CC}	V
T_A	Operating Free–Air Temperature		–55	+125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns
MC74HCT					
V_{CC}	DC Supply Voltage (Referenced to GND)		4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, DC Output Voltage (Referenced to GND) (Note 3)		0	V_{CC}	V
T_A	Operating Free–Air Temperature		–55	+125	°C
t_r, t_f	Input Rise or Fall Time		0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (MC74HC125A, MC74HC126A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL}					V
		$\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	
		$\|I_{out}\| \leq 3.6$ mA $\|I_{out}\| \leq 6.0$ mA $\|I_{out}\| \leq 7.8$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL}					V
		$\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	
		$\|I_{out}\| \leq 3.6$ mA $\|I_{out}\| \leq 6.0$ mA $\|I_{out}\| \leq 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (MC74HC125A, MC74HC126A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figure 4)	2.0 3.0 4.5 6.0	90 36 18 15	115 45 23 20	135 60 27 23	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figure 4)	2.0 3.0 4.5 6.0	120 45 24 20	150 60 30 26	180 80 36 31	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Y (Figure 4)	2.0 3.0 4.5 6.0	90 36 18 15	115 45 23 20	135 60 27 23	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 4)	2.0 3.0 4.5 6.0	60 22 12 10	75 28 15 13	90 34 18 15	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum 3–State Output Capacitance (Output in High–Impedance State)	–	15	15	15	pF

			Typical @ 25°C	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output) (Note 4)	5.0	30	pF

4. Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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DC ELECTRICAL CHARACTERISTICS (MC74HCT125A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL}					V
		$\|I_{out}\| \le 20\ \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	
		$\|I_{out}\| \le 6.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL}					V
		$\|I_{out}\| \le 20\ \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	
		$\|I_{out}\| \le 6.0$ mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	2.0	20	80	μA

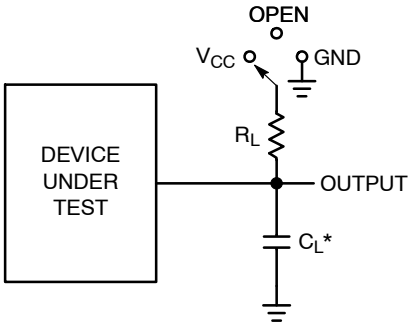
ΔI_{CC}	Additional Quiescent Supply Current	V_{IN} = 2.4 V; Any One Input V_{IN} = V_{CC} or GND, Other Inputs; I_{OUT} = 0 μA	5.5	≥–55°C	25°C to 125°C	
				2.9	2.4	mA

AC ELECTRICAL CHARACTERISTICS (MC74HCT125A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figure 4)	5.0	18	23	27	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figure 4)	5.0	24	30	36	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Y (Figure 4)	5.0	18	23	27	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 4)	5.0	12	15	18	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum 3–State Output Capacitance (Output in High–Impedance State)	–	15	15	15	pF

			Typical @ 25°C	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output) (Note 4)	5.0	30	pF

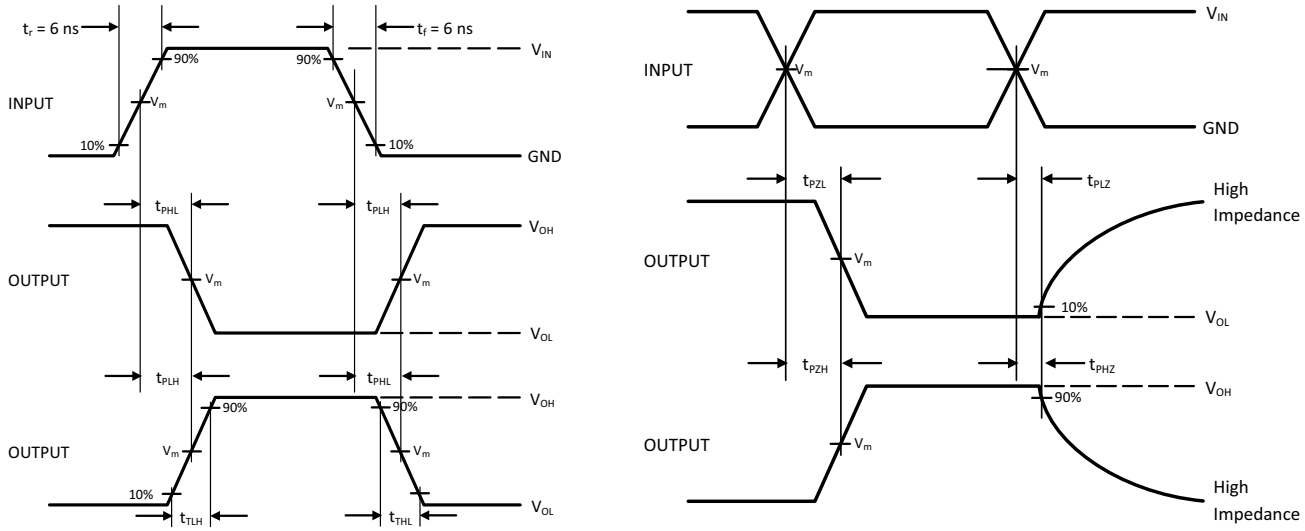
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*C_L Includes probe and jig capacitance

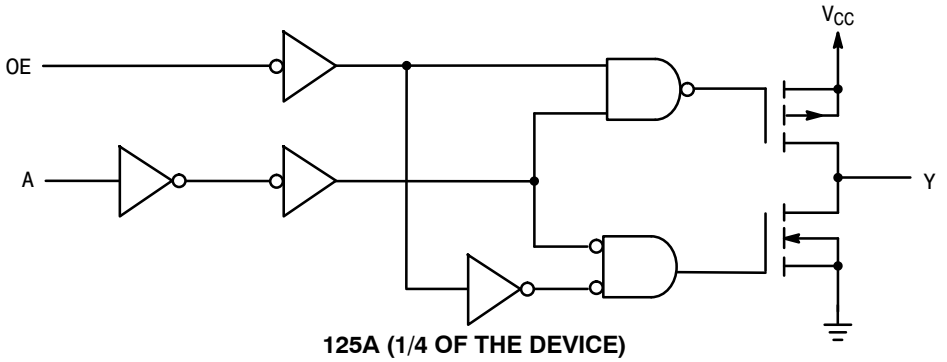
Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 3. Test Circuit

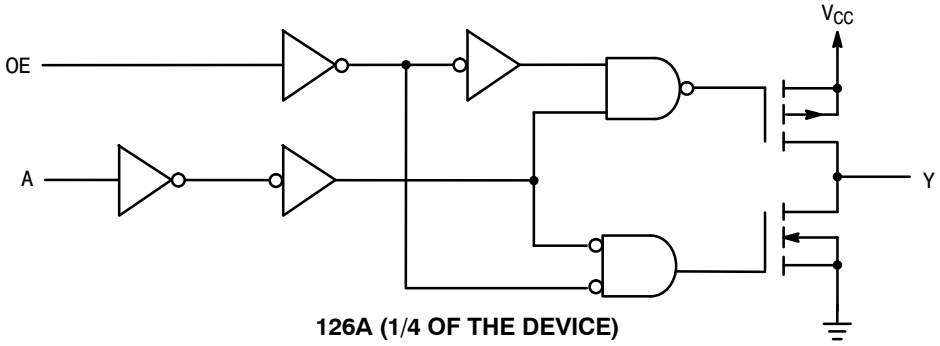


Device	V_{IN}, V	V_m, V
MC74HC125A, MC74HC126A	V_{CC}	50% x V_{CC}
MC74HCT125A	3 V	1.3 V

Figure 4. Switching Waveforms



125A (1/4 OF THE DEVICE)



126A (1/4 OF THE DEVICE)

Figure 5. Expanded Logic Diagrams

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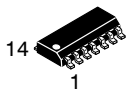
ORDERING INFORMATION

Device	Package	Marking	Shipping†
MC74HC125ADG	SOIC−14	HC125A	55 Units / Rail
MC74HC125ADR2G	SOIC−14	HC125A	2500 / Tape & Reel
MC74HC125ADR2G−Q*	SOIC−14	HC125A	2500 / Tape & Reel
MC74HC125ADTG	TSSOP−14	HC 125A	2500 / Tape & Reel
MC74HC125ADTR2G	TSSOP−14	HC 125A	2500 / Tape & Reel
MC74HC125ADTR2G−Q*	TSSOP−14	HC 125A	2500 / Tape & Reel
MC74HCT125ADR2G	SOIC−14	HCT125A	2500 / Tape & Reel
MC74HCT125ADR2G−Q*	SOIC−14	HCT125A	2500 / Tape & Reel
MC74HCT125ADTR2G	TSSOP−14	HCT 125A	2500 / Tape & Reel
MC74HCT125ADTR2G−Q*	TSSOP−14	HCT 125A	2500 / Tape & Reel
MC74HC126ADR2G	SOIC−14	HC126A	2500 / Tape & Reel
MC74HC126ADR2G−Q*	SOIC−14	HC126A	2500 / Tape & Reel
MC74HC126ADTR2G	TSSOP−14	HC 126A	2500 / Tape & Reel
MC74HC126ADTR2G−Q*	TSSOP−14	HC 126A	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

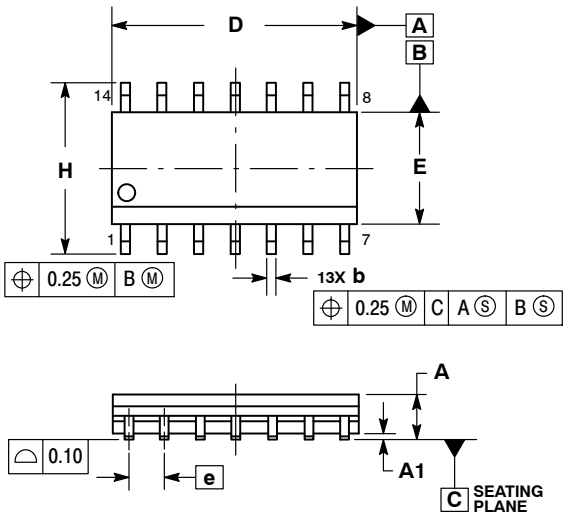
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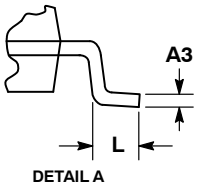


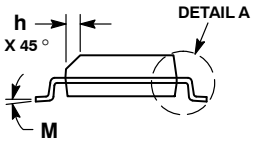
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



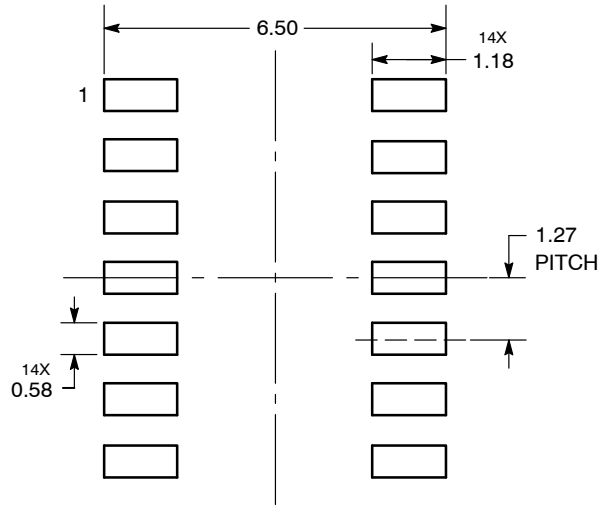




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

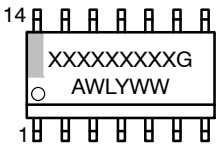
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

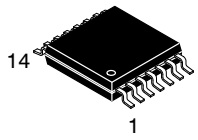
STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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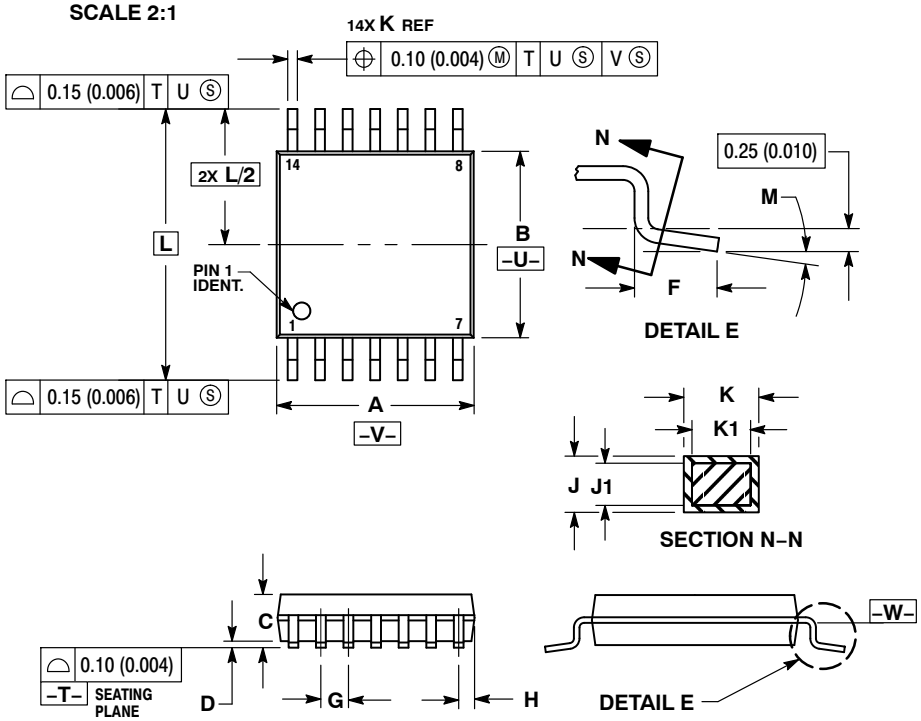
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SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

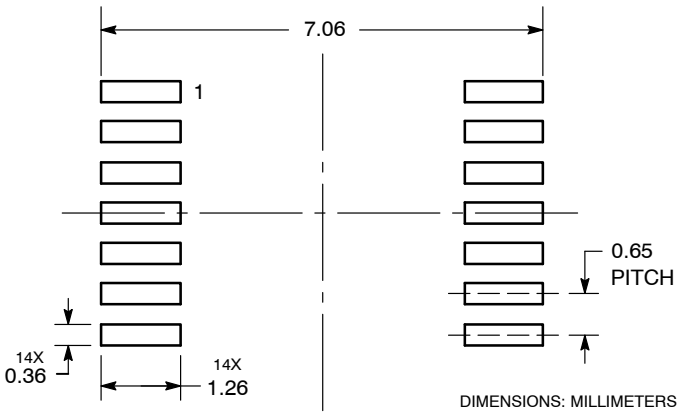
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

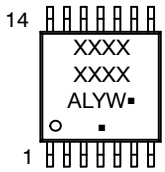
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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