# Complementary Silicon Plastic Power Transistors

## DPAK−3 for Surface Mount Applications

# MJD243 (NPN), MJD253 (PNP)

Designed for low voltage, low−power, high−gain audio amplifier applications.

### Features

- High DC Current Gain
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“−1” Suffix)
- Low Collector−Emitter Saturation Voltage
- High Current−Gain − Bandwidth Product
- Annular Construction for Low Leakage
- Epoxy Meets UL 94 V−0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS

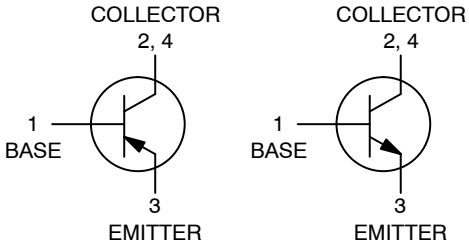
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Base Voltage | $V_{CB}$ | 100 | Vdc |
| Collector−Emitter Voltage | $V_{CEO}$ | 100 | Vdc |
| Emitter−Base Voltage | $V_{EB}$ | 7.0 | Vdc |
| Collector Current − Continuous | $I_C$ | 4.0 | Adc |
| Collector Current − Peak | $I_{CM}$ | 8.0 | Adc |
| Base Current | $I_B$ | 1.0 | Adc |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 12.5<br>0.1 | W<br>W/°C |
| Total Device Dissipation @ $T_A$ = 25°C (Note 2)<br>Derate above 25°C | $P_D$ | 1.4<br>0.011 | W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | −65 to +150 | °C |
| ESD − Human Body Model | HBM | 3B | V |
| ESD − Machine Model | MM | C | V |

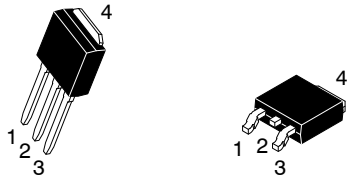
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted on minimum pad sizes recommended.

## 4.0 A, 100 V, 12.5 W POWER TRANSISTOR

### COMPLEMENTARY

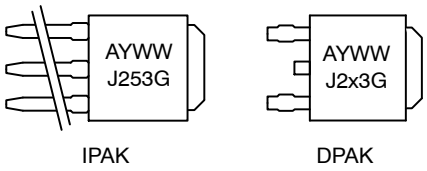



**IPAK**
**CASE 369D**
**STYLE 1**

**DPAK−3**
**CASE 369C**
**STYLE 1**

### MARKING DIAGRAM




IPAK DPAK

A = Assembly Location
Y = Year
WW = Work Week
x = 4 or 5
G = Pb−Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the device on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

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## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance<br>Junction−to−Case<br>Junction−to−Ambient (Note 2) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>10<br>89.3 | °C/W |

2. When surface mounted on minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Collector−Emitter Sustaining Voltage (Note 3)<br>($I_C$ = 10 mAdc, $I_B$ = 0) | $V_{CEO(sus)}$ | <br>100 | <br>– | Vdc |
| Collector Cutoff Current<br>($V_{CB}$ = 100 Vdc, $I_E$ = 0)<br>($V_{CB}$ = 100 Vdc, $I_E$ = 0, $T_J$ = 125°C) | $I_{CBO}$ | <br>–<br>– | <br>100<br>100 | <br>nAdc<br>μAdc |
| Emitter Cutoff Current<br>($V_{BE}$ = 7.0 Vdc, $I_C$ = 0) | $I_{EBO}$ | <br>– | <br>100 | nAdc |
| DC Current Gain (Note 3)<br>($I_C$ = 200 mAdc, $V_{CE}$ = 1.0 Vdc)<br>($I_C$ = 1.0 Adc, $V_{CE}$ = 1.0 Vdc) | $h_{FE}$ | <br>40<br>15 | <br>180<br>– | – |
| Collector−Emitter Saturation Voltage (Note 3)<br>($I_C$ = 500 mAdc, $I_B$ = 50 mAdc)<br>($I_C$ = 1.0 Adc, $I_B$ = 100 mAdc) | $V_{CE(sat)}$ | <br>–<br>– | <br>0.3<br>0.6 | Vdc |
| Base−Emitter Saturation Voltage (Note 3)<br>($I_C$ = 2.0 Adc, $I_B$ = 200 mAdc) | $V_{BE(sat)}$ | <br>– | <br>1.8 | Vdc |
| Base−Emitter On Voltage (Note 3)<br>($I_C$ = 500 mAdc, $V_{CE}$ = 1.0 Vdc) | $V_{BE(on)}$ | <br>– | <br>1.5 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Current−Gain − Bandwidth Product (Note 4)<br>($I_C$ = 100 mAdc, $V_{CE}$ = 10 Vdc, $f_{test}$ = 10 MHz) | $f_T$ | <br>40 | <br>– | MHz |
| Output Capacitance<br>($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 0.1 MHz) | $C_{ob}$ | <br>– | <br>50 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
4. $f_T = |h_{FE}| \bullet f_{test}$.



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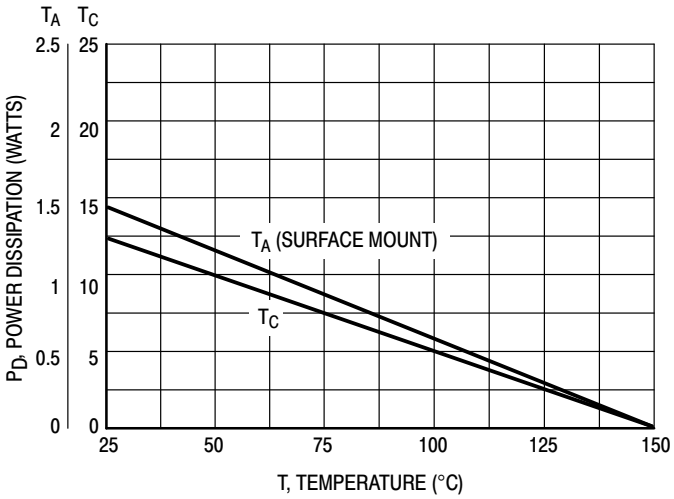



**Figure 1. Power Derating**

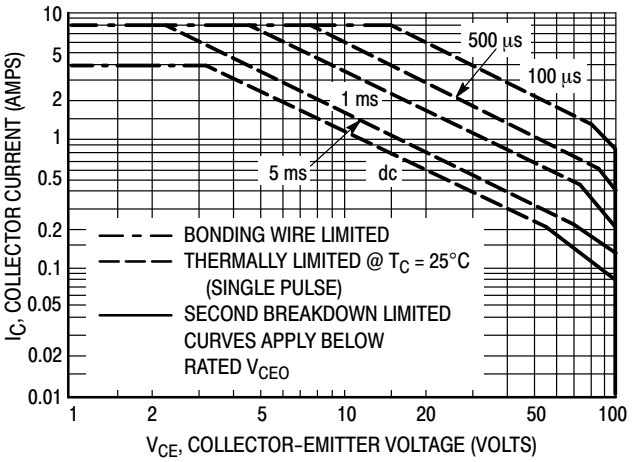



**Figure 2. Active Region Maximum Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; $T_C$ is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

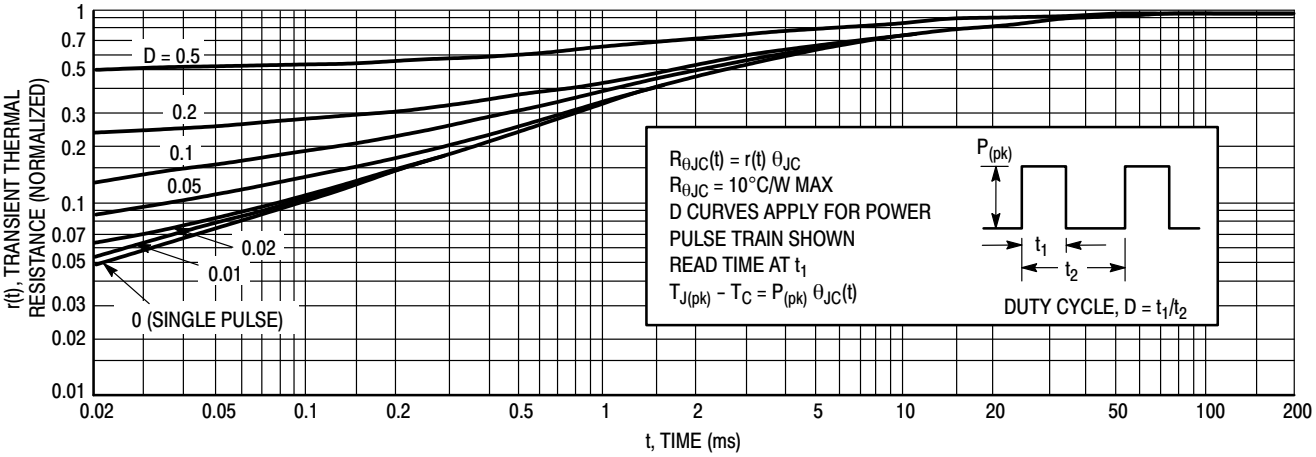
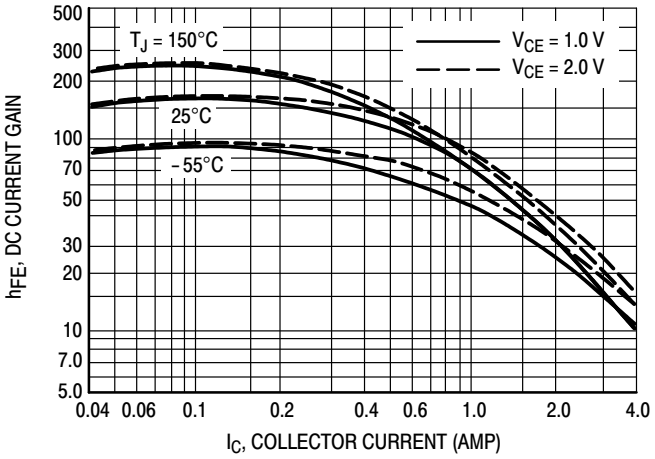



**Figure 3. Thermal Response**



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**NPN**
**MJD243**




**PNP**
**MJD253**

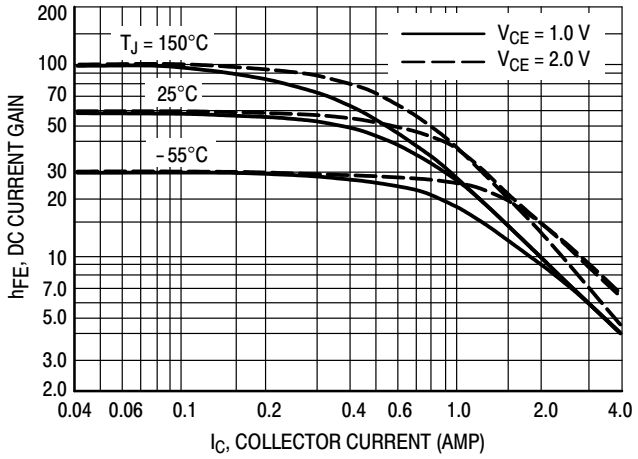
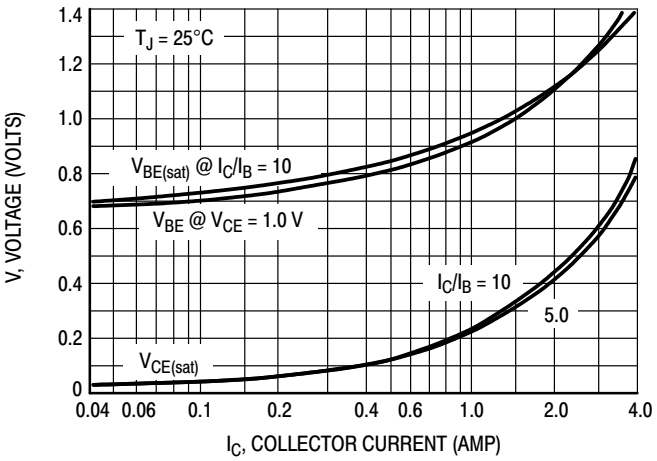



**Figure 4. DC Current Gain**



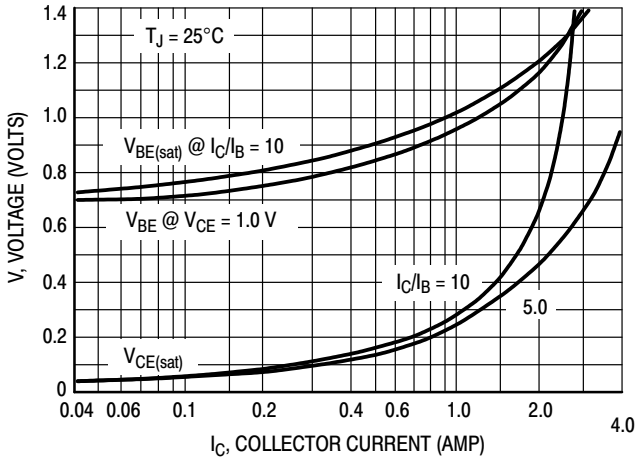
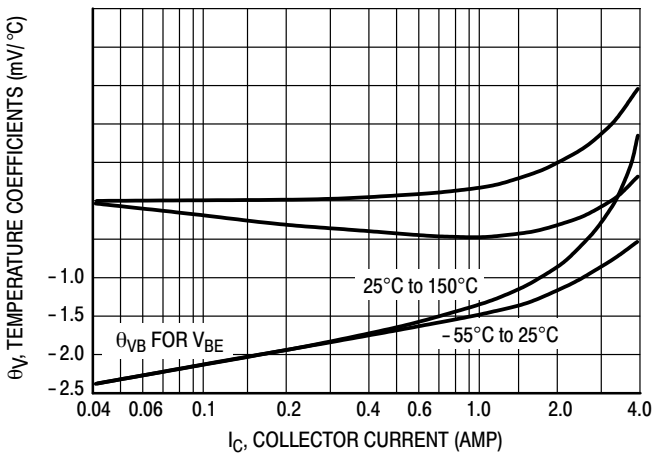




**Figure 5. "On" Voltages**



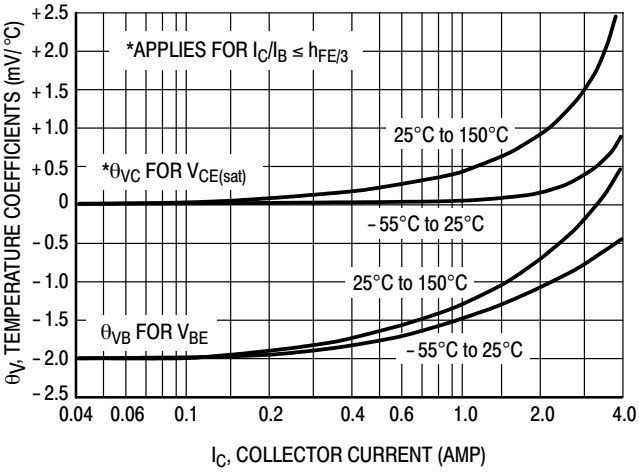
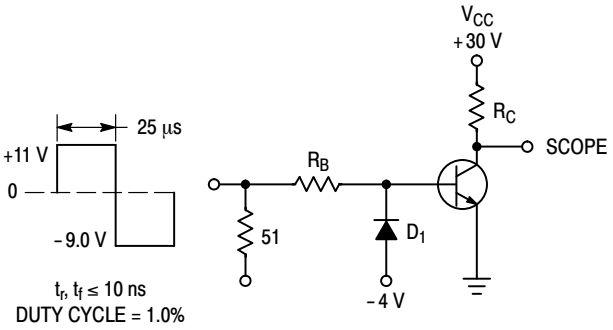




**Figure 6. Temperature Coefficients**



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$R_B$ and $R_C$ VARIED TO OBTAIN DESIRED CURRENT LEVELS
$D_1$ MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

**Figure 7. Switching Time Test Circuit**

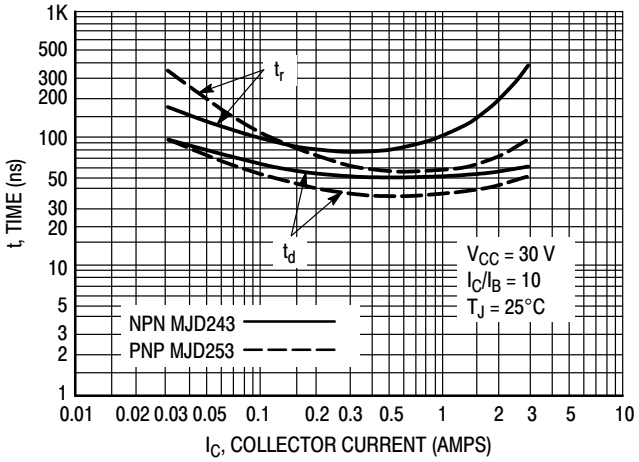



**Figure 8. Turn−On Time**

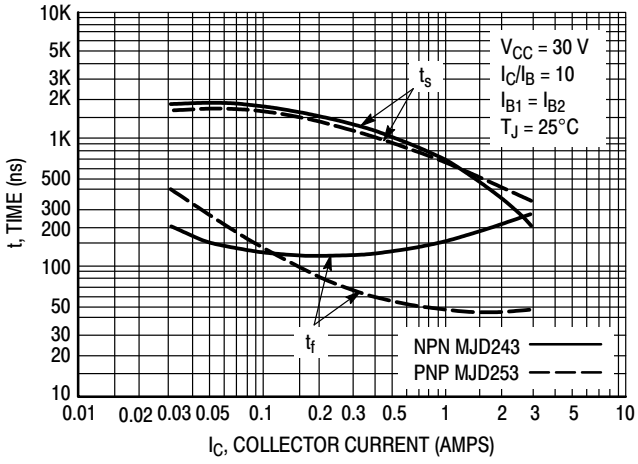



**Figure 9. Turn−Off Time**

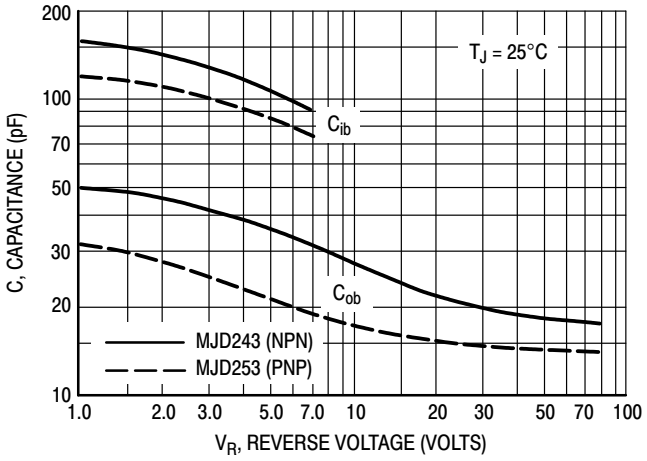



**Figure 10. Capacitance**

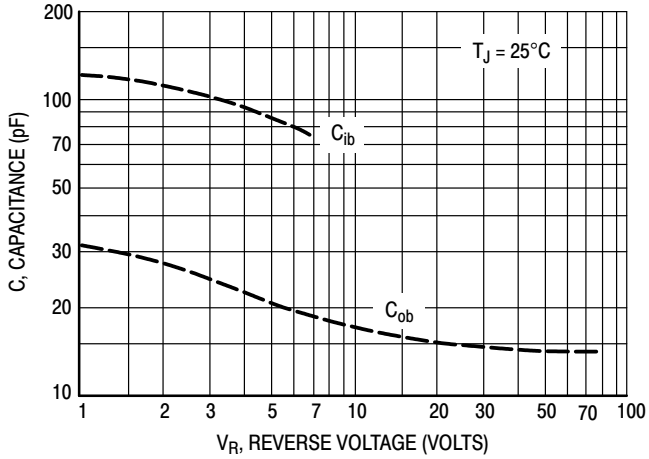



**Figure 11. Capacitance**



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## ORDERING INFORMATION

| Device | Package Type | Package | Shipping† |
|---|---|---|---|
| MJD243G | DPAK−3 (Pb−Free) | 369C | 75 Units / Rail |
| MJD243T4G | DPAK−3 (Pb−Free) | 369C | 2,500 / Tape & Reel |
| NJVMJD243T4G* | DPAK−3 (Pb−Free) | 369C | 2,500 / Tape & Reel |
| MJD253T4G | DPAK−3 (Pb−Free) | 369C | 2,500 / Tape & Reel |
| NJVMJD253T4G* | DPAK−3 (Pb−Free) | 369C | 2,500 / Tape & Reel |

**DISCONTINUED** (Note 5)

| Device | Package Type | Package | Shipping† |
|---|---|---|---|
| MJD253−1G | IPAK (Pb−Free) | 369D | 75 Units / Rail |

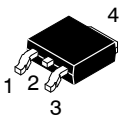
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable



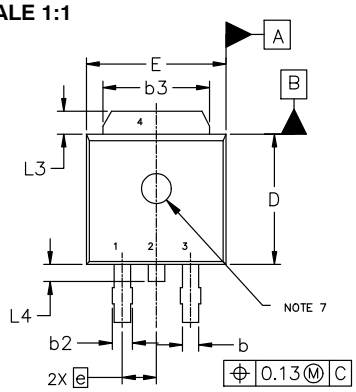
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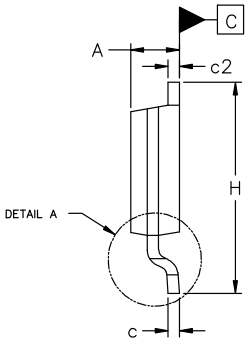

**SCALE 1:1**

**DPAK3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE J

DATE 12 AUG 2025

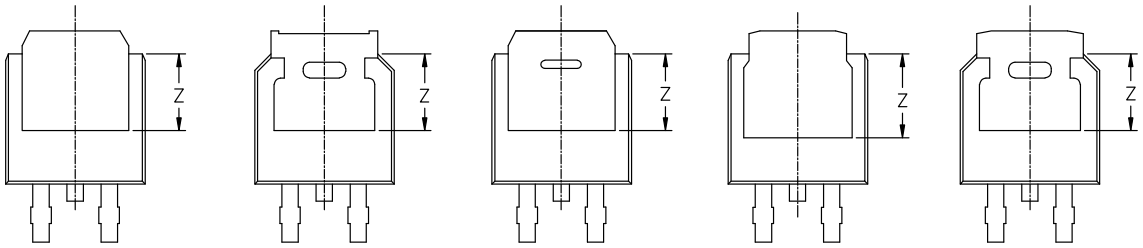



TOP VIEW




SIDE VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 2.18 | 2.28 | 2.38 |
| A1 | 0.00 | --- | 0.13 |
| b | 0.63 | 0.76 | 0.89 |
| b2 | 0.72 | 0.93 | 1.14 |
| b3 | 4.57 | 5.02 | 5.46 |
| c | 0.46 | 0.54 | 0.61 |
| c2 | 0.46 | 0.54 | 0.61 |
| D | 5.97 | 6.10 | 6.22 |
| E | 6.35 | 6.54 | 6.73 |
| e | 2.29 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | --- | 1.27 |
| L4 | --- | --- | 1.01 |
| Z | 3.93 | --- | --- |

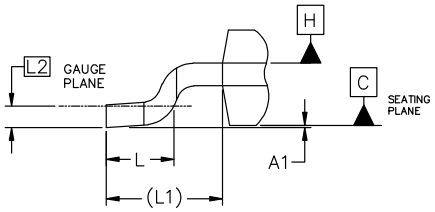



BOTTOM VIEW

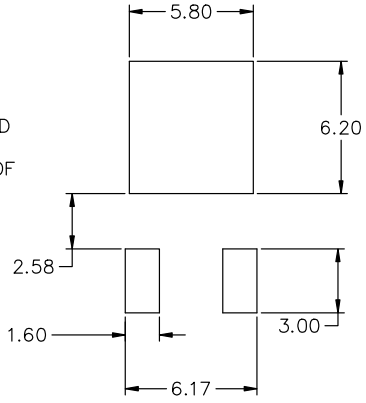
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.




DETAIL A
ROTATED 90° CW




RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

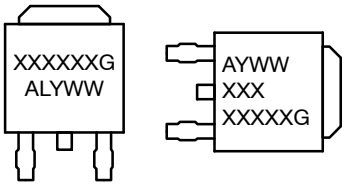
| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON10527D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **DPAK3 6.10x6.54x2.28, 2.29P** | **PAGE 1 OF 2** |

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**DPAK3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE J

DATE 12 AUG 2025

## GENERIC MARKING DIAGRAM*




**IC** **Discrete**

| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

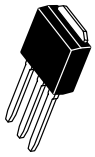



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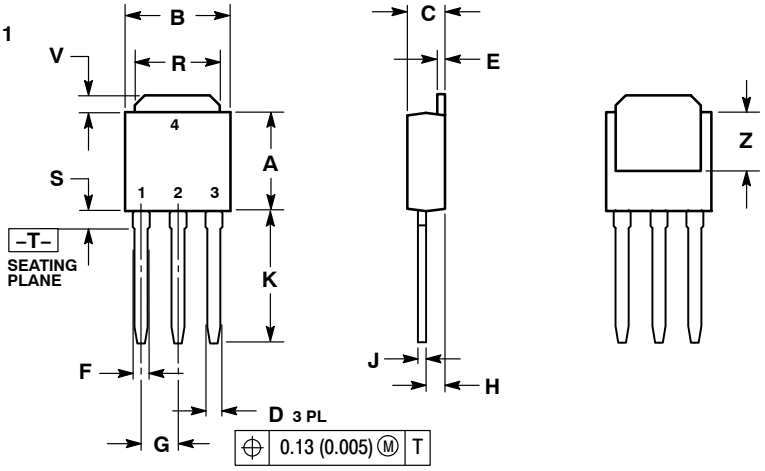
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**IPAK**
CASE 369D
ISSUE C

DATE 15 DEC 2010



SCALE 1:1




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

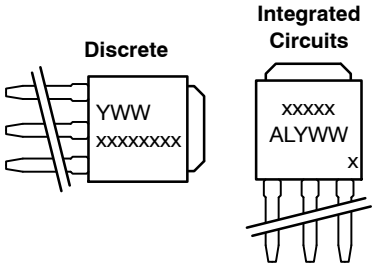
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## GENERIC MARKING DIAGRAMS




xxxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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|---|---|---|
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| **DESCRIPTION:** | **IPAK (DPAK INSERTION MOUNT)** | **PAGE 1 OF 1** |

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