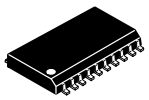
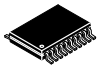
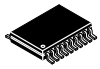
Inverting Octal 3-STATE Buffer, Octal 3-STATE Buffer

MM74HCT240, MM74HCT244


SOIC−20 WB
CASE 751D−05


TSSOP−20 WB
CASE 948E


TSSOP−20
CASE 948AQ

General Description

The MM74HCT240 and MM74HCT244 3−STATE buffers utilize advanced silicon−gate CMOS technology and are general purpose high speed inverting and non−inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. All three devices are TTL input compatible and have a fanout of 15 LS−TTL equivalent inputs.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug−in replacements for LS−TTL devices and can be used to reduce power consumption in existing designs.

The MM74HCT240 is an inverting buffer and the MM74HCT244 is a non−inverting buffer. Each device has two active low enables (1G and 2G), and each enable independently controls 4 buffers.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL Input Compatible
- Typical Propagation Delay: 14 ns
- 3−STATE Outputs for Connection to System Buses
- Low Quiescent Supply Current: 160 μA
- High Output Drive Current: 6 mA (min)
- These are Pb−Free Devices

TRUTH TABLES

MM74HCT240

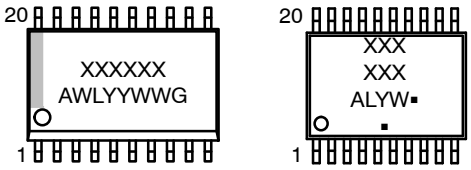
$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

MM74HCT244

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

NOTES: H = HIGH Level
L = LOW Level
Z = High Impedance

MARKING DIAGRAMS

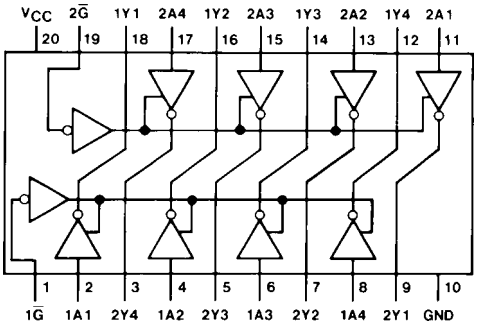


XXXXX = Specific Device Code
A = Assembly Location
L/WL = Wafer Lot
Y/YY = Year
W/WW = Work Week
▪ or G = Pb−Free Package

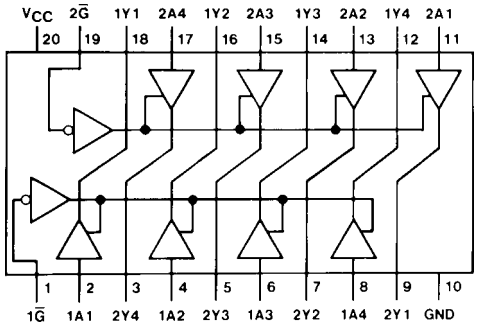
(Note: Microdot may be in either location)

CONNECTION DIAGRAMS

Pin Assignment for SOIC and TSSOP



MM74HCT240 (Top View)



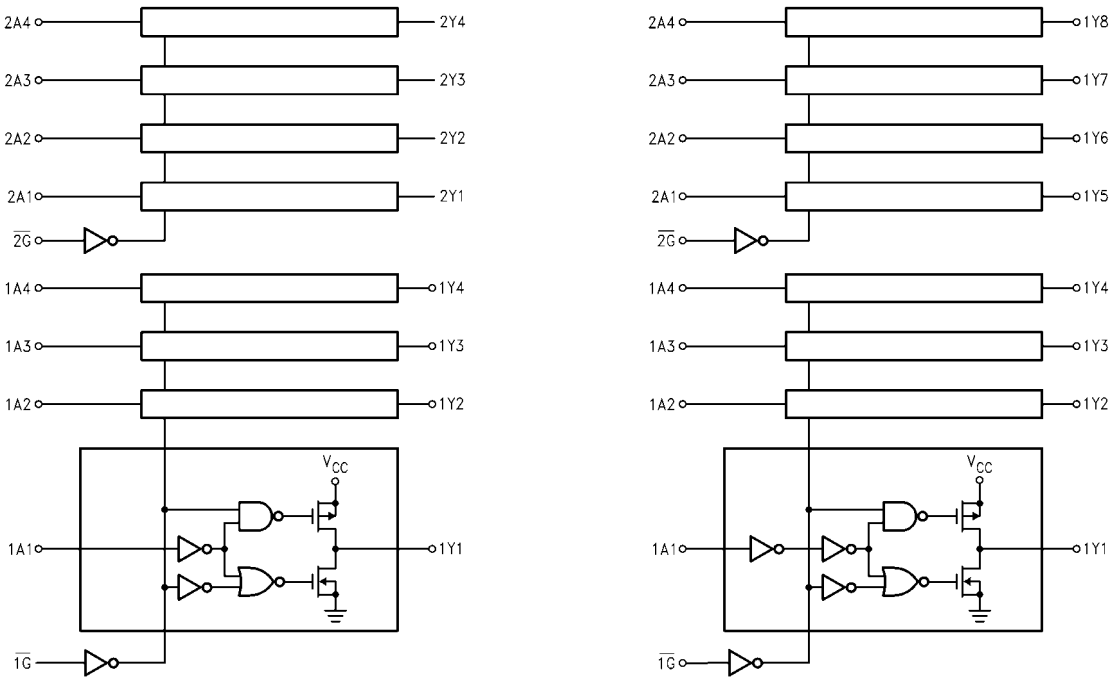
MM74HCT244 (Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 4 of this data sheet.

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Logic Diagrams



MM74HCT240 **MM74HCT244**

Figure 1. Logic Diagrams

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to +6.5	V
V_{IN}	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC V_{CC} or GND Current, per Pin	±70	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
P_D	Power Dissipation SOIC−20W TSSOP−20	 1302 833	mW
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS (Note 1)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−55	+125	°C
t_r, t_f	Input Rise or Fall Times	−	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10% unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		−	2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage		−	0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN-EE} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5 V $\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5 V	 V_{CC} 4.2 5.2	 V_{CC}−0.1 3.98 4.98	 V_{CC}−0.1 3.84 4.84	 V_{CC}−0.1 3.7 4.7	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5 V $\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5 V	 0 0.2 0.2	 0.1 0.26 0.26	 0.1 0.33 0.33	 0.1 0.4 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}	−	±0.05	±0.5	±1.0	μA
I_{OZ}	Maximum 3−STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH} G = V_{IL}	−	±0.25	±2.5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	−	4.0	40	160	μA
		V_{IN} = 2.4 V or 0.5 V (Note 2)	0.6	1.0	1.3	1.5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Measured per input. All other inputs at V_{CC} or GND.

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AC ELECTRICAL CHARACTERISTICS

(MM74HCT240, MM74HCT244 V_{CC} = 5.0 V, $t_r = t_f$ = 6 ns, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	14	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF, R_L = 1 kΩ	20	30	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF, R_L = 1 kΩ	16	25	ns

AC ELECTRICAL CHARACTERISTICS

(MM74HCT240, MM74HCT244 V_{CC} = 5.0 V ±10%, $t_r = t_f$ = 6 ns, unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40°C to 85°C		T_A = −55°C to 125°C	Unit
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF	14	20	25	30	ns
		C_L = 150 pF	20	28	35	42	
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ, C_L = 50 pF	21	30	38	45	ns
		R_L = 1 kΩ, C_L = 150 pF	26	42	53	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	16	25	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	6	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance		15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 3)	(per buffer) $\overline{G}$ = V_{CC}, G = GND $\overline{G}$ = GND, G = V_{CC}	 5 90	 – –	 – –	 – –	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \cdot V_{CC}^2 \cdot f + I_{CC} \cdot V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \cdot V_{CC} \cdot f + I_{CC}$.

ORDERING INFORMATION

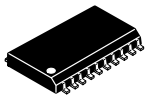
Device	Package	Shipping†
MM74HCT240MTCX	TSSOP−20, case 948AQ (Pb−Free)	2500 Units / Tape & Reel
MM74HCT244MTC	TSSOP−20 WB, case 948E (Pb−Free)	75 Units / Tube
MM74HCT244MTCX	TSSOP−20, case 948AQ (Pb−Free)	2500 Units / Tape & Reel
MM74HCT244WM	SOIC−20 WB, case 751D−05 (Pb−Free)	38 Units / Tube
MM74HCT244WMX	SOIC−20 WB, case 751D−05 (Pb−Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

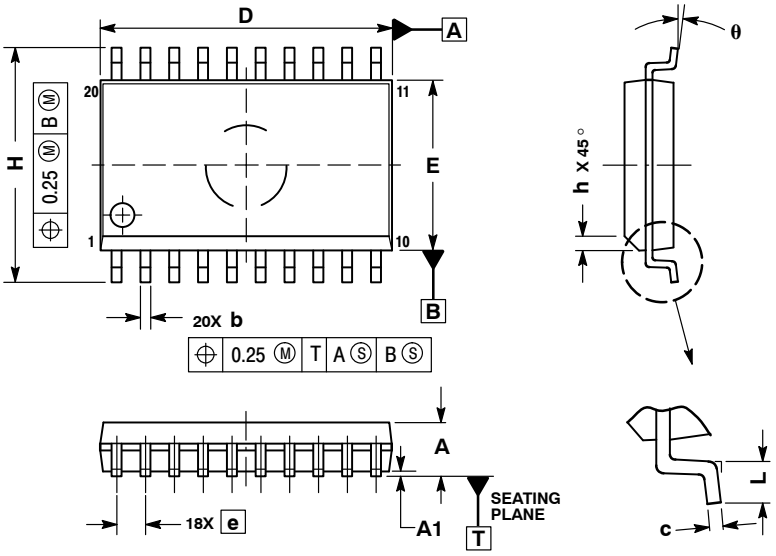
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SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



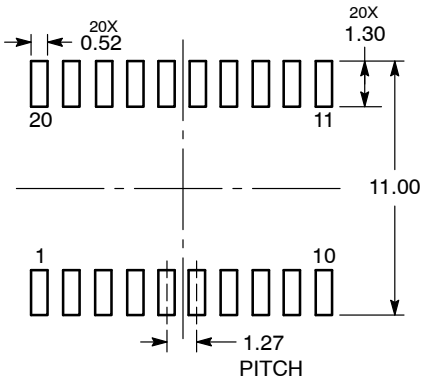
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

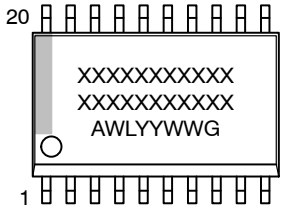
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

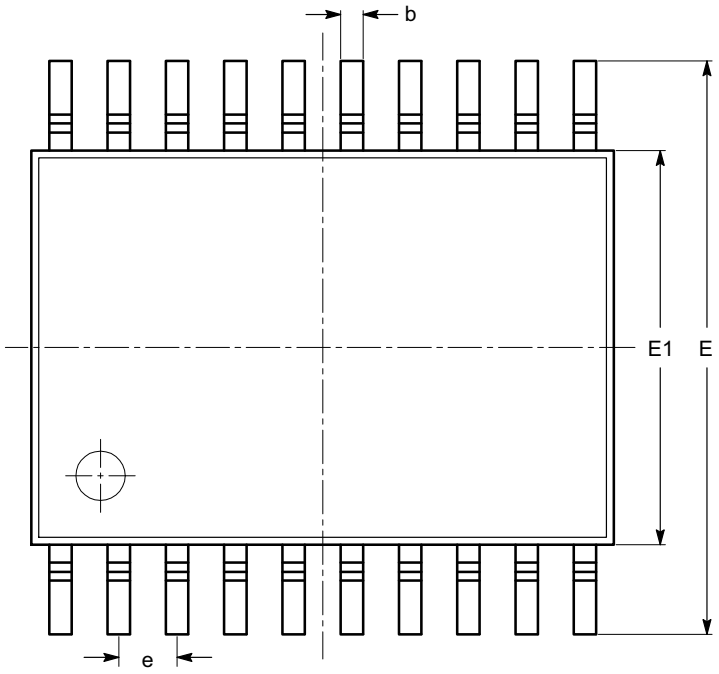
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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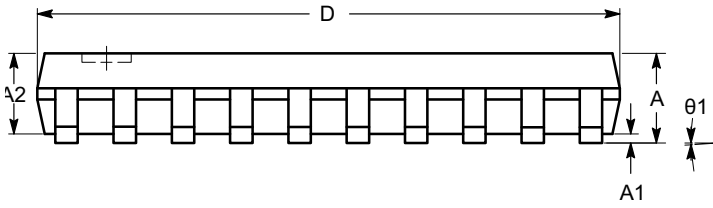
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

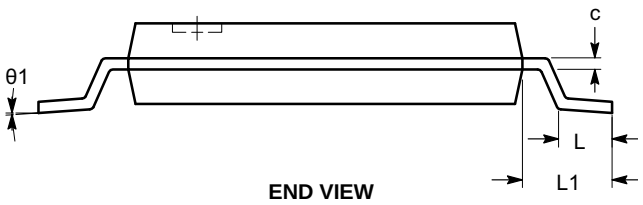


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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