High Voltage High Efficiency Power Factor Correction Controller

NCP1615

The NCP1615 is a high voltage PFC controller designed to drive PFC boost stages based on an innovative Current Controlled Frequency Foldback (CCFF) method. In this mode, the circuit operates in critical conduction mode (CrM) when the inductor current exceeds a programmable value. When the current is below this preset level, the NCP1615 linearly decays the frequency down to a minimum of about 26 kHz at the sinusoidal zero−crossing. CCFF maximizes the efficiency at both nominal and light load. In particular, the standby losses are reduced to a minimum. Innovative circuitry allows near−unity power factor even when the switching frequency is reduced.

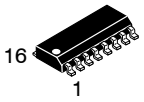
The integrated high voltage start−up circuit eliminates the need for external start−up components and consumes negligible power during normal operation. Housed in a SOIC−16 package, the NCP1615 incorporates the features necessary for robust and compact PFC stages, with few external components.

General Features

- High Voltage Start−Up Circuit with Integrated Brownout Detection
- Input to Force Controller into Standby Mode
- Restart Pin Allows Adjustment of Bulk Voltage Hysteresis in Standby Mode
- Skip Mode Near the Line Zero Crossing
- Fast Line / Load Transient Compensation
- Valley Switching for Improved Efficiency
- High Drive Capability: −500 mA/+800 mA
- Wide V_{CC} Range: from 9.5 V to 30 V
- Input Voltage Range Detection
- Line Removal Detection Circuitry
- Power Saving Mode (PSM) Enables < 30 mW No−load Power Consumption
- This is a Pb and Halogen Free Device

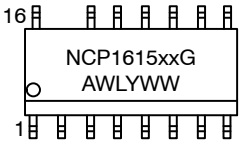
Safety Features

- Adjustable Bulk Undervoltage Detection (BUV)
- Soft Overvoltage Protection
- Overcurrent Protection
- Open Pin Protection for FB and FOVP/BUV Pins
- Internal Thermal Shutdown
- Bi−Level Latch Input for OVP and OTP
- Bypass/Boost Diode Short Circuit Protection
- Open Ground Pin Protection



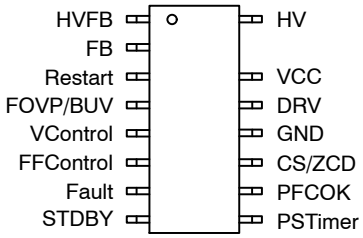
SOIC−16 NB
CASE 752AC

MARKING DIAGRAM



NCP1615xx = Specific Device Code
xx = C4 or C5
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTION



NCP1615 16 Pins (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

Typical Applications

- PC Power Supplies
- Off Line Appliances Requiring Power Factor Correction
- LED Drivers
- Flat TVs

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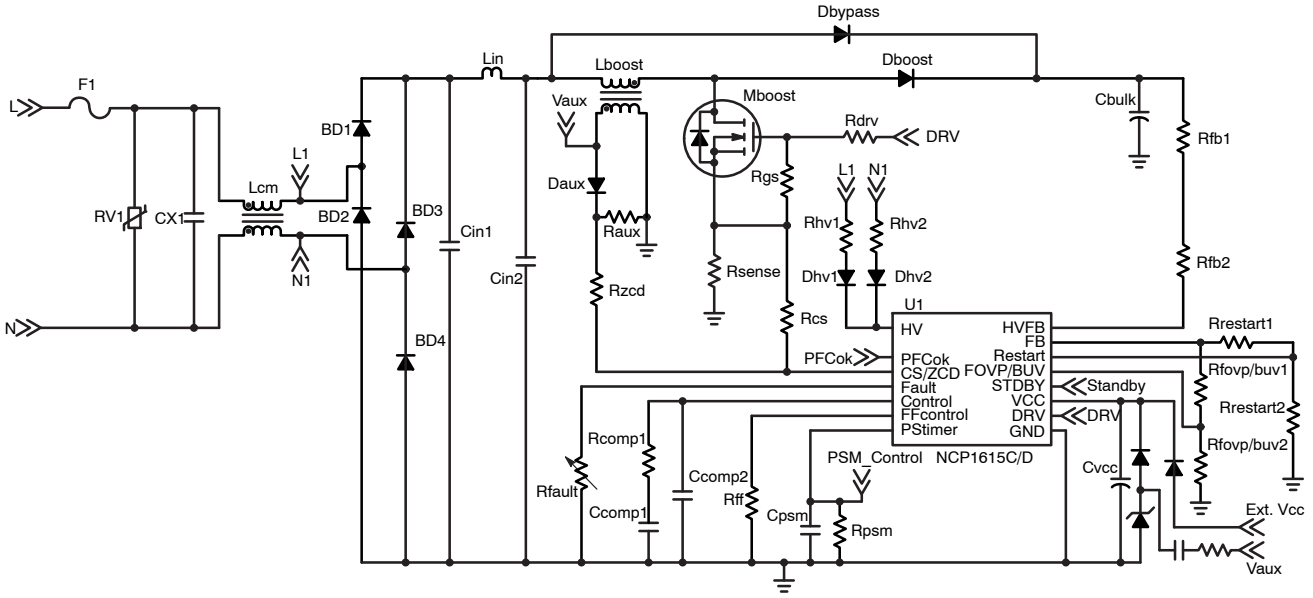


Figure 1. NCP1615 Typical Application Circuit

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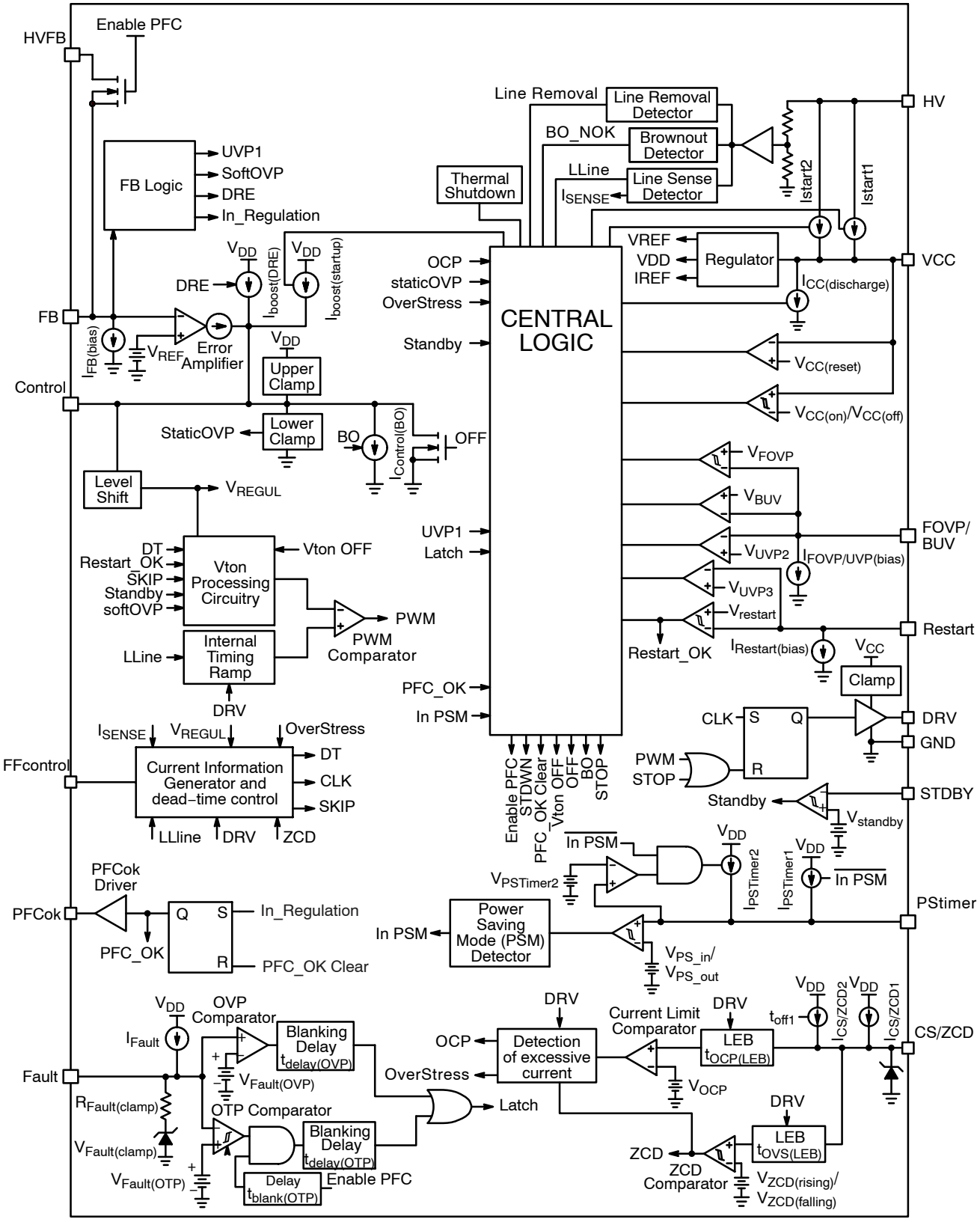


Figure 2. NCP1615 Functional Block Diagram

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Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Name	Function
1	HVFB	High voltage PFC feedback input. An external resistor divider is used to sense the PFC bulk voltage. The divider high side resistor chain from the PFC bulk voltage connects to this pin. An internal high−voltage switch disconnects the high side resistor chain from the low side resistor when the PFC is latched or in PSM in order to reduce input power.
2	FB	This pin receives a portion of the PFC output voltage for the regulation and the dynamic response enhancer (DRE) that speeds up the loop response when the output voltage drops below 95.5% of the regulation level. V_{FB} is also the input signal for the Soft−Overvoltage Comparators as well as the Undervoltage (UVP) Comparator. The UVP Comparator prevents operation as long as V_{FB} is lower than 12% of the reference voltage (V_{REF}). The Soft−Overvoltage Comparator (Soft−OVP) gradually reduces the duty ratio to zero when V_{FB} exceeds 105% of V_{REF}. A 250 nA sink current is built−in to trigger the UVP protection and disable the part if the feedback pin is accidentally open. A dedicated comparator monitors the bulk voltage and disables the controller if a line overvoltage fault is detected.
3	Restart	This pin receives a portion of the PFC output voltage for determining the restart level after entering standby mode.
4	FOVP/BUV	Input terminal for the Fast Overvoltage (Fast−OVP) and Bulk Undervoltage (BUV) Comparators. The circuit disables the driver if the $V_{FOVP/BUV}$ exceeds the V_{FOVP} threshold which is set 2% higher than the reference for the Soft−OVP comparator monitoring the FB pin. This allows the both pins to receive the same portion of the output voltage. The BUV Comparator trips when $V_{FOVP/BUV}$ falls below 76% of the reference voltage. A BUV fault disables the driver and grounds the PFCOK pin. The BUV function has no action whenever the PFCOK pin is in low state. Once the downstream converter is enabled the BUV Comparator monitors the output voltage to ensure it is high enough for proper operation of the downstream converter. A 250 nA current pulls down the pin and disable the controller if the pin is accidentally open.
5	Control	The error amplifier output is available on this pin. The network connected between this pin and ground sets the regulation loop bandwidth. It is typically set below 20 Hz to achieve high power factor ratios. This pin is grounded when the controller is disabled. The voltage on this pin gradually increases during power up to achieve a soft−start.
6	FFcontrol	This pin sources a current representative to the line current. Connect a resistor between this pin and GND to generate a voltage representative of the line current. When this voltage exceeds the internal 2.5 V reference, the circuit operates in critical conduction mode. If the pin voltage is below 2.5 V, a dead−time is generated that approximately equates [83 μs • (1 − ($V_{FFcontrol}$/V_{REF}))]. By this means, the circuit increases the deadtime when the current is smaller and decreases the deadtime as the current increases. The circuit skips cycles whenever $V_{FFcontrol}$ is below 0.65 V to prevent the PFC stage from operating near the line zero crossing where the power transfer is particularly inefficient. This does result in a slightly increased distortion of the current. If superior power factor is required, offset the voltage on this pin by more than 0.75 V to inhibit skip operation.
7	Fault	The controller enters fault mode if the voltage of this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor. Fault detection triggers a latch.
8	STDBY	This pin is used to force the controller into standby mode.
9	PSTimer	Power saving mode (PSM) timer adjust. A capacitor between this pin and GND, $C_{PSTimer}$, sets the delay time before the controller enters power saving mode. Once the controller enters power saving mode the IC is disabled and the current consumption is reduced to a maximum of 100 μA. The input filter capacitor discharge function is available while in power saving mode. The device enters PSM if the voltage on this pin exceeds the PSM threshold, V_{PS_in}. A secondary side controller optocoupler pulls down on the pin to prevent the controller from entering PSM when the load is connected to the power supply. The controller is enabled once $V_{PSTimer}$ drops below V_{PS_out}.
10	PFCOK	This pin is grounded until the PFC output has reached its nominal level. It is also grounded if the controller detects a fault. The voltage on this pin is 5 V once the controller reaches regulation.
11	CS/ZCD	This pin monitors the MOSFET current to limit its maximum current. This pin is also connected to an internal comparator for zero current detection (ZCD). This comparator is designed to monitor a signal from an auxiliary winding and to detect the core reset when this voltage drops to zero. The auxiliary winding voltage is to be applied through a diode to avoid altering the current sense information for the on time (see application schematic).
12	GND	Ground reference.
13	DRV	MOSFET driver. The high current capability of the totem pole gate drive (−0.5/ +0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
14	VCC	Supply input. This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds $V_{CC(on)}$. After start−up, the operating range is 9.5 V up to 30 V.
15		Removed for creepage distance.
16	HV	This pin is the input for the line removal detection, line level detection, and brownout detection circuits. This pin is also the input for the high voltage start−up circuit.

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Table 2. ORDERABLE PART OPTIONS

Part Number	V_{CC}	HV Start−Up	OTP Fault	PSM	V_{CC} Discharge	Start−Up I_{boost}	$V_{lineselect(HL)}$	$V_{lineselect(LL)}$	High Line Threshold
NCP1615C4DR2G	17 V	Yes	Latch	Yes	Yes	Yes	250 V	236 V	250 Vdc
NCP1615C5DR2G	17 V	Yes	Latch	Yes	Yes	Yes	236 V	222 V	236 Vdc

Table 3. ORDERING INFORMATION

Part Number	Device Marking	Package	Shipping†
NCP1615C4DR2G	NCP1615C4	SOIC−16 NB, LESS PIN 15 (Pb−Free)	2500 / Tape & Reel
NCP1615C5DR2G	NCP1615C5		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. For version C5, the line valley counter is replaced with a lockout timer.

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Table 4. MAXIMUM RATINGS (Notes 2 and 3)

Rating	Pin	Symbol	Value	Unit
High Voltage Start−Up Circuit Input Voltage	HV	V_{HV}	−0.3 to 700	V
High Voltage Feedback Input Voltage	HVFB	V_{HVFB}	−0.3 to 700	V
High Voltage Feedback Input Current	HVFB	I_{HVFB}	0.5	mA
Zero Current Detection and Current Sense Input Voltage (Note 4)	CS/ZCD	$V_{CS/ZCD}$	−0.3 to $V_{CS/ZCD(MAX)}$	V
Zero Current Detection and Current Sense Input Current	CS/ZCD	$I_{CS/ZCD}$	+5	mA
Control Input Voltage (Note 5)	Control	$V_{Control}$	−0.3 to $V_{Control(MAX)}$	V
Supply Input Voltage	VCC	$V_{CC(MAX)}$	−0.3 to 30	V
Fault Input Voltage	Fault	V_{Fault}	−0.3 to (V_{CC} + 0.6)	V
PSTimer Input Voltage	PSTimer	$V_{PSTimer}$	−0.3 to (V_{CC} + 0.6)	V
Driver Maximum Voltage (Note 6)	DRV	V_{DRV}	−0.3 to V_{DRV}	V
Driver Maximum Current	DRV	$I_{DRV(SRC)}$ $I_{DRV(SNK)}$	500 800	mA
Maximum Input Voltage (Note 7)	Other Pins	V_{MAX}	−0.3 to 7	V
Maximum Operating Junction Temperature		T_J	−40 to 150	°C
Storage Temperature Range		T_{STG}	−60 to 150	°C
Lead Temperature (Soldering, 10 s)		$T_{L(MAX)}$	300	°C
Moisture Sensitivity Level		MSL	1	−
Power Dissipation (T_A = 70°C, 1 Oz Cu, 0.155 Sq Inch Printed Circuit Copper Clad) Plastic Package SOIC−16NB		P_D	 465	mW
Thermal Resistance, (Junction to Ambient 1 Oz Cu Printed Circuit Copper Clad) Plastic Package SOIC−16NB		 $R_{\theta JA}$ $R_{\theta JC}$	 172 68	°C/W
ESD Capability Human Body Model per JEDEC Standard JESD22−A114E. Charge Device Model per JEDEC Standard JESD22−C101E.			 > 2000 > 500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.
3. Low Conductivity Board. As mounted on 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC51−1 conductivity test PCB. Test conditions were under natural convection of zero air flow.
4. $V_{CS/ZCD(MAX)}$ is the CS/ZCD pin positive clamp voltage.
5. $V_{Control(MAX)}$ is the Control pin positive clamp voltage.
6. When V_{CC} exceeds the driver clamp voltage ($V_{DRV(high)}$), V_{DRV} is equal to $V_{DRV(high)}$. Otherwise, V_{DRV} is equal to V_{CC}.
7. When the voltage applied to these pins exceeds 5.5 V, they sink a current about equal to (V_{pin} − 5.5 V) / (4 kΩ). An applied voltage of 7 V generates a sink current of approximately 0.375 mA.

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Table 5. ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{HV} = 120 V, V_{FB} = 2.4 V, R_{HVFB} = 200 kΩ, V_{HVFB} = 20 V, $C_{VControl}$ = 10 nF, $V_{FFcontrol}$ = 2.6 V, $V_{ZCD/CS}$ = 0 V, $R_{ZCD/CS}$ = 3 kΩ, $V_{FOVPBUV}$ = 2.4 V, V_{STDBY} = 1 V, $V_{Restart}$ = 1 V, $V_{PSTimer}$ = 0 V, V_{Fault} = open, V_{PFCOK} = open, C_{DRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
START−UP AND SUPPLY CIRCUITS						
Start−Up Threshold	V_{CC} increasing	$V_{CC(on)}$	16.0	17.0	18.0	V
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	8.5	9.0	9.5	V
V_{CC} Hysteresis	$V_{CC(on)} - V_{CC(off)}$	$V_{CC(HYS)}$	7.0	8.0	–	V
Internal Latch / Logic Reset Level	V_{CC} decreasing	$V_{CC(reset)}$	7.3	7.8	8.3	V
Difference Between $V_{CC(off)}$ and $V_{CC(reset)}$	$V_{CC(off)} - V_{CC(reset)}$	$\Delta V_{CC(reset)}$	0.5	–	–	V
Regulation Level in Power Saving Mode		$V_{CC(PS_on)}$	–	11	–	V
Transition from I_{start1} to I_{start2}	V_{CC} increasing, I_{HV} = 650 μA	$V_{CC(inhibit)}$	–	0.8	–	V
Start−Up Time	C_{VCC} = 0.47 μF, V_{CC} = 0 V to $V_{CC(on)}$	$t_{start-up}$	–	–	2.5	ms
Inhibit Current Sourced from V_{CC} Pin	V_{CC} = 0 V, V_{HV} = 100 V	I_{start1}	0.375	0.5	0.87	mA
Start−Up Current Sourced from V_{CC} Pin	$V_{CC} = V_{CC(on)} - 0.5$ V, V_{HV} = 100 V	I_{start2}	6.5	12	16.5	mA
Start−Up Circuit Off−State Leakage Current	V_{HV} = 400 V V_{HV} = 700 V	$I_{HV(off1)}$ $I_{HV(off2)}$	– –	– –	70 75	μA
Minimum Voltage for Start−Up Circuit						V
Start−Up	I_{start2} = 6.5 mA, $V_{CC} = V_{CC(on)} - 0.5$ V	$V_{HV(MIN)}$	–	–	38	
During PSM	I_{start2} = 6.5 mA, $V_{CC} = V_{CC(PS_on)} - 0.5$ V	$V_{HV(MIN_PSM)}$	–	–	30	
Supply Current						mA
In Power Saving Mode	$V_{CC} = V_{CC(PS_on)}$	I_{CC1}	–	–	0.1	
Latch	V_{Fault} = 4 V	I_{CC2}	–	0.6	1.0	
Standby Mode	$V_{standby}$ = 0 V, $V_{Restart}$ = 3 V	I_{CC3}	–	–	1.0	
No Switching	V_{FB} = 2.55 V	I_{CC4}	–	–	2.8	
Operating Current	f = 50 kHz, C_{DRV} = open, $V_{Control}$ = 2.5 V, V_{FB} = 2.45 V	I_{CC5}	–	2.0	3.5	
LINE REMOVAL						
Line Voltage Removal Detection Timer		$t_{line(removal)}$	60	100	165	ms
Upslope Detection Reset Timer	HV increasing	$t_{HV(up)}$	–	14	–	ms
Downslope Detection Reset Timer	HV decreasing	$t_{HV(down)}$	–	1	–	ms
Slope Detection Limit		S_{HV}	–	3.5	–	V/ms
Discharge Current	$V_{CC} = V_{CC(off)}$ + 200 mV $V_{CC} = V_{CC(discharge)}$ + 200 mV	$I_{CC(discharge)}$	20 10	25 16.5	30 30	mA
HV Discharge Current		$I_{HV(discharge)}$	–	4	–	mA
HV Discharge Level		$V_{HV(discharge)}$	–	–	40	V
V_{CC} Discharge Level		$V_{CC(discharge)}$	3.8	4.5	5.4	V
LINE DETECTION						
High Line Level Detection Threshold C4 Version C5 Version	V_{HV} increasing	$V_{lineselect(HL)}$	 232 220	 250 236	 267 252	V
Low Line Level Detection Threshold C4 Version C5 Version	V_{HV} decreasing	$V_{lineselect(LL)}$	 220 207	 236 222	 252 237	V
Line Select Hysteresis	V_{HV} increasing	$V_{lineselect(HYS)}$	10	–	–	V

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Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
LINE DETECTION						
High to Low Line Mode Selector Timer C5 Version C4 Version	V_{HV} decreasing	t_{line}	 20 43	 25 54	 30 65	ms
Low to High Line Mode Selector Timer	V_{HV} increasing	$t_{delay(line)}$	200	300	400	μs
Line Valley Lockout Counter C4 Version	After t_{line} expires	n_{LL}	 –	 8	 –	
Line Level Lockout Timer C5 Version	After t_{line} expires	$t_{line(lockout)}$	 120	 150	 180	ms
POWER SAVING MODE						
PSM Enable Threshold	$V_{PSTimer}$ increasing	V_{PS_in}	3.325	3.500	3.675	V
PSM Disable Threshold	$V_{PSTimer}$ decreasing	V_{PS_out}	0.45	0.50	0.55	V
PSTimer Pull Up Current Source	$V_{PSTimer}$ = 0.9 V	$I_{PSTimer1}$	4.5	5.9	7.3	μA
PSTimer Fast Pull Up Current Source	$V_{PSTimer}$ = 3.4 V	$I_{PSTimer2}$	800	1000	1200	μA
PSTimer Leakage Current	$V_{PSTimer}$ = 4 V	$I_{PSTimer(bias)}$	–	–	100	nA
$I_{PSTimer2}$ Enable Threshold		$V_{PSTimer2}$	0.95	1.00	1.05	V
Filter Delay Before Entering PSM	$V_{PSTimer}$ > V_{PS_in}	$t_{delay(PS_in)}$	–	40	–	μs
Detection Delay Before Exiting PSM and Turning On Start−Up Circuit	$V_{PSTimer}$ < V_{PS_out}	$t_{delay(PS_out)}$	–	–	100	μs
PSTimer Discharge Current	$V_{PSTimer}$ = $V_{PSTimer(off)}$ + 10 mV	$I_{PSTimer(DIS)}$	160	–	–	μA
PSTimer Discharge Turn Off Threshold	$V_{PSTimer}$ decreasing	$V_{PSTimer(off)}$	0.05	0.10	0.15	V
PFC FB SWITCH						
PFC Off−State Leakage Current	$V_{PSTimer}$ = 4 V, V_{HVFB} = 500 V	$I_{HVFB(off)}$	–	0.1	3	μA
PFC Feedback Switch On Resistance	V_{HVFB} = 2.75 V, I_{HVFB} = 100 μA	$R_{FBswitch(on)}$	–	–	10	kΩ
ON−TIME CONTROL						
Maximum On Time − Low Line	V_{HV} = 162.5 V, $V_{Control}$ = $V_{Control(MAX)}$ V_{HV} = 162.5 V, $V_{Control}$ = 2.5 V	 $t_{on(LL)}$ $t_{on(LL)2}$	 20.5 9.5	 23.7 11.0	 27.5 13.0	μs
Maximum On Time − High Line	V_{HV} = 325 V, $V_{Control}$ = $V_{Control(MAX)}$	$t_{on(HL)}$	6.8	8.1	9.2	μs
Minimum On−Time	V_{HV} = 162 V V_{HV} = 325 V	$t_{onLL(MIN)}$ $t_{onHL(MIN)}$	– –	– –	200 100	ns
CURRENT SENSE						
Current Limit Threshold		V_{ILIM}	0.46	0.50	0.54	V
Leading Edge Blanking Duration		$t_{OCP(LEB)}$	100	200	350	ns
Current Limit Propagation Delay	Step $V_{CS/ZCD}$ > V_{ILIM} to DRV falling edge	$t_{OCP(delay)}$	–	40	200	ns
Overstress Leading Edge Blanking Duration		$t_{OVS(LEB)}$	50	100	170	ns
Over Stress Detection Propagation Delay	$V_{CS/ZCD}$ > $V_{ZCD(rising)}$ to DRV falling edge	$t_{OVS(delay)}$	–	40	200	ns
REGULATION BLOCK						
Reference Voltage	T_J = 25°C T_J = −40 to 125°C	V_{REF} V_{REF}	2.475 2.445	2.500 2.500	2.525 2.550	V
Error Amplifier Current Source Sink	V_{FB} = 2.4 V, $V_{VControl}$ = 2 V V_{FB} = 2.6 V, $V_{VControl}$ = 2 V	$I_{EA(SRC)}$ $I_{EA(SNK)}$	16 16	20 20	24 24	μA

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Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
REGULATION BLOCK						
Open Loop Error Amplifier Transconductance	V_{FB} = V_{REF} +/− 100 mV	g_m	180	210	245	μS
Maximum Control Voltage	V_{FB} = 2 V	$V_{Control(MAX)}$	–	4.5	–	V
Minimum Control Voltage	V_{FB} = 2.6 V	$V_{Control(MIN)}$	–	0.5	–	V
EA Output Control Voltage Range	$V_{Control(MAX)}$ − $V_{Control(MIN)}$	$\Delta V_{Control}$	3.9	4.0	4.1	V
DRE Detect Threshold	V_{FB} decreasing	V_{DRE}	–	2.388	–	V
DRE Threshold Hysteresis	V_{FB} increasing	$V_{DRE(HYS)}$	–	–	25	mV
Ratio between the DRE Detect Threshold and the Regulation Level	V_{FB} decreasing, V_{DRE} / V_{REF}	K_{DRE}	95.0	95.5	96.0	%
Control Pin Source Current During Start−Up	PFCOK = Low, $V_{VControl}$ = 2 V	$I_{Control(start-up)}$	80	100	113	μA
EA Boost Current During Start−Up		$I_{boost(start-up)}$	–	80	–	μA
Control Pin Source Current During DRE	$V_{VControl}$ = 2 V	$I_{Control(DRE)}$	180	220	250	μA
EA Boost Current During DRE		$I_{boost(DRE)}$	–	200	–	μA
PFC GATE DRIVE						
Rise Time (10−90%)	V_{DRV} from 10 to 90% of V_{DRV}	$t_{DRV(rise)}$	–	40	80	ns
Fall Time (90−10%)	90 to 10% of V_{DRV}	$t_{DRV(fall)}$	–	20	60	ns
Source Current Capability	V_{DRV} = 0 V	$I_{DRV(SRC)}$	–	500	–	mA
Sink Current Capability	V_{DRV} = 12 V	$I_{DRV(SNK)}$	–	800	–	mA
High State Voltage	V_{CC} = $V_{CC(off)}$ + 0.2 V, R_{DRV} = 10 kΩ V_{CC} = 28 V, R_{DRV} = 10 kΩ	$V_{DRV(high1)}$ $V_{DRV(high2)}$	8 10	– 12	– 14	V
Low Stage Voltage	V_{STDBY} = 0 V	$V_{DRV(low)}$	–	–	0.25	V
ZERO CURRENT DETECTION						
Zero Current Detection Threshold	$V_{CS/ZCD}$ rising $V_{CS/ZCD}$ falling	$V_{ZCD(rising)}$ $V_{ZCD(falling)}$	675 200	750 250	825 300	mV
ZCD and Current Sense Ratio	$V_{ZCD(rising)}$/V_{ILIM}	$K_{ZCD/ILIM}$	1.4	1.5	1.6	–
Positive Clamp Voltage	$I_{CS/ZCD}$ = 0.75 mA $I_{CS/ZCD}$ = 5 mA	$V_{CS/ZCD(MAX1)}$ $V_{CS/ZCD(MAX2)}$	7.1 15.4	7.4 15.8	7.8 16.1	V
CS/ZCD Input Bias Current	$V_{CS/ZCD}$ = $V_{ZCD(rising)}$ $V_{CS/ZCD}$ = $V_{ZCD(falling)}$	$I_{CS/ZCD(bias1)}$ $I_{CS/ZCD(bias2)}$	0.5 0.5	– –	2.0 2.0	μA
ZCD Propagation Delay	Measured from $V_{CS/ZCD}$ = $V_{ZCD(falling)}$ to DRV rising	t_{ZCD}	–	60	200	ns
Minimum detectable ZCD Pulse Width	Measured from $V_{ZCD(rising)}$ to $V_{ZCD(falling)}$	t_{SYNC}	–	110	200	ns
Maximum Off−Time (Watchdog Timer)	 $V_{CS/ZCD}$ > $V_{ZCD(rising)}$	t_{off1} t_{off2}	80 700	200 1000	320 1300	μs
Missing Valley Timeout Timer	Measured after last ZCD transition	t_{tout}	20	30	50	μs
Pull−Up Current Source	Detects open pin fault.	$I_{CS/ZCD1}$	–	1	–	μA
Source Current for CS/ZCD Impedance Testing	Pulls up at the end of t_{off1}	$I_{CS/ZCD2}$	–	250	–	μA
CURRENT CONTROLLED FREQUENCY FOLDBACK						
Minimum Dead Time	$V_{FFCntrol}$ = 2.6 V	t_{DT1}	–	–	0	μs
Median Dead Time	$V_{FFCntrol}$ = 1.75 V	t_{DT2}	4.5	6.5	7.5	μs

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Table 5. ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{HV} = 120 V, V_{FB} = 2.4 V, R_{HVFB} = 200 kΩ, V_{HVFB} = 20 V, $C_{VControl}$ = 10 nF, $V_{FFcontrol}$ = 2.6 V, $V_{ZCD/CS}$ = 0 V, $R_{ZCD/CS}$ = 3 kΩ, $V_{FOVPBUV}$ = 2.4 V, V_{STDBY} = 1 V, $V_{Restart}$ = 1 V, $V_{PSTimer}$ = 0 V, V_{Fault} = open, V_{PFCOK} = open, C_{DRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
CURRENT CONTROLLED FREQUENCY FOLDBACK						
Maximum Dead Time	$V_{FFCntrol}$ = 1.0 V	t_{DT3}	11	13	15	μs
FFcontrol Pin Current − Low Line	V_{HV} = 162.5V, $V_{Control}$ = $V_{Control(MAX)}$	I_{DT1}	180	200	220	μA
FFcontrol Pin Current − High Line	V_{HV} = 325 V, $V_{Control}$ = $V_{Control(MAX)}$	I_{DT2}	116	135	148	μA
FFcontrol Skip Level	$V_{FFCntrol}$ = increasing $V_{FFCntrol}$ = decreasing	$V_{skip(out)}$ $V_{skip(in)}$	– 0.55	0.75 0.65	0.85 –	V
FFcontrol Skip Hysteresis		$V_{SKIP(HYS)}$	50	–	–	mV
Minimum Operating Frequency		f_{MIN}	–	26	–	kHz
FEEDBACK OVER AND UNDERVOLTAGE PROTECTION						
Soft−OVP to V_{REF} Ratio	V_{FB} = increasing, V_{SOVP}/V_{REF}	$K_{SOVP/VREF}$	104	105	106	%
Soft−OVP Threshold	V_{FB} = increasing	V_{SOVP}	–	2.625	–	V
Soft−OVP Hysteresis	V_{FB} = decreasing	$V_{SOVP(HYS)}$	35	50	65	mV
Static OVP Minimum Duty Ratio	V_{FB} = 2.55 V, $V_{Control}$ = open	D_{MIN}	–	–	0	%
Undervoltage to V_{REF} Ratio	V_{FB} = increasing, V_{UVP1}/V_{REF}	$K_{UVP1/VREF}$	8	12	16	%
Undervoltage Threshold	V_{FB} = decreasing	V_{UVP1}	–	300	–	mV
Undervoltage to V_{REF} Hysteresis Ratio	V_{FB} = increasing	$V_{UVP1(HYS)}$	–	–	25	mV
Feedback Input Sink Current	V_{FB} = V_{SOVP}, HVFB = open V_{FB} = V_{UVP1}, HVFB = open	$I_{FB(SNK1)}$ $I_{FB(SNK2)}$	50 50	200 200	500 450	nA
FAST OVERVOLTAGE AND BULK UNDERVOLTAGE PROTECTION (FOVP and BUV)						
Fast OVP Threshold	$V_{FOVP/BUV}$ increasing	V_{FOVP}	–	2.675	–	V
Fast OVP Hysteresis	$V_{FOVP/BUV}$ decreasing	$V_{FOVP(HYS)}$	15	30	60	mV
Ratio Between Fast and Soft OVP Levels	$K_{FOVP/SOVP}$ = V_{FOVP}/ V_{SOVP}	$K_{FOVP/SOVP}$	101.5	102.0	102.5	%
Ratio Between Fast OVP and V_{REF}	$K_{FOVP/VREF}$ = V_{FOVP}/ V_{REF}	$K_{FOVP/VREF}$	106	107	108	%
Bulk Undervoltage Threshold	$V_{FOVP/BUV}$ decreasing	V_{BUV}	–	1.9	–	V
Undervoltage Protection Threshold to V_{REF} Ratio	$V_{FOVP/BUV}$ decreasing, V_{BUV}/V_{REF}	$K_{BUV/VREF}$	74	76	78	%
Open Pin Detection Threshold	$V_{FOVP/BUV}$ decreasing	V_{UVP2}	0.2	0.3	0.4	V
Open Pin Detection Hysteresis	$V_{FOVP/BUV}$ increasing	$V_{UVP2(HYS)}$	–	10	–	mV
Pull−Down Current Source	$V_{FOVP/BUV}$ = V_{BUV} $V_{FOVP/ BUV}$ = V_{UVP2}	$I_{FOVP/BUV(bias1)}$ $I_{FOVP/BUV(bias2)}$	50 50	200 200	450 450	nA
STANDBY INPUT						
Standby Input Threshold	V_{STDBY} decreasing	$V_{standby}$	285	300	315	mV
Standby Input Blanking Duration		$t_{blank(STDBY)}$	0.8	1	1.2	ms
RESTART						
Restart Threshold Ratio	$V_{Restart}/V_{REF}$	$K_{restart}$	97.5	98.0	98.5	%
Restart Threshold		$V_{restart}$	–	2.45	–	V
Restart Input Pull Down Current	$V_{Restart}$ = V_{UVP3}	$I_{restart(bias)}$	50	200	450	nA
Open Pin Detection Threshold		V_{UVP3}	0.2	0.3	0.4	V
Open Pin Detection Hysteresis		$V_{UVP3(HYS)}$	–	10	–	mV

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Table 5. ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{HV} = 120 V, V_{FB} = 2.4 V, R_{HVFB} = 200 kΩ, V_{HVFB} = 20 V, $C_{VControl}$ = 10 nF, $V_{FFcontrol}$ = 2.6 V, $V_{ZCD/CS}$ = 0 V, $R_{ZCD/CS}$ = 3 kΩ, $V_{FOVPBUV}$ = 2.4 V, V_{STDBY} = 1 V, $V_{Restart}$ = 1 V, $V_{PSTimer}$ = 0 V, V_{Fault} = open, V_{PFCOK} = open, C_{DRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
BROWNOUT DETECTION						
System Start−Up Threshold	V_{HV} increasing	$V_{BO(start)}$	102	111	118	V
System Shutdown Threshold	V_{HV} decreasing	$V_{BO(stop)}$	92	100	108	V
Hysteresis	V_{HV} increasing	$V_{BO(HYS)}$	7	11	–	V
Brownout Detection Blanking Time	V_{HV} decreasing, delay from $V_{BO(stop)}$ to drive disable	$t_{BO(stop)}$	43	54	65	ms
Control Pin Sink Current in Brownout	$t_{BO(stop)}$ expires	$I_{Control(BO)}$	40	50	60	μA
FAULT INPUT						
Overvoltage Protection (OVP) Threshold	V_{Fault} increasing	$V_{Fault(OVP)}$	2.79	3.00	3.21	V
Delay Before Fault Confirmation						μs
Used for OVP Detection	V_{Fault} increasing	$t_{delay(OVP)}$	22.5	30.0	37.5	
Used for OTP Detection	V_{Fault} decreasing	$t_{delay(OTP)}$	22.5	30.0	37.5	
Overtemperature Protection (OTP) Threshold	V_{Fault} decreasing	$V_{Fault(OTP_in)}$	0.38	0.40	0.42	V
OTP Blanking Delay During Start−Up		$t_{blank(OTP)}$	4	5	6	ms
OTP Pull−Up Current Source	V_{Fault} = $V_{Fault(OTP_in)}$ + 0.2 V	$I_{Fault(OTP)}$	43	46	49	μA
Fault Input Clamp Voltage	V_{Fault} = open	$V_{Fault(clamp)}$	1.15	1.7	2.25	V
Fault Input Clamp Series Resistor		$R_{Fault(clamp)}$	1.32	1.55	1.78	kΩ
PFCOK SIGNAL						
PFCOK Output Voltage	I_{PFCOK} = −5 mA	V_{PFCOK}	4.75	5.00	5.25	V
PFCOK Low State Output Voltage	I_{PFCOK} = 5 mA	$V_{PFCOK(low)}$	–	–	250	mV
THERMAL SHUTDOWN						
Thermal Shutdown	Temperature increasing	T_{SHDN}	–	150	–	°C
Thermal Shutdown Hysteresis	Temperature decreasing	$T_{SHDN(HYS)}$	–	50	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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DETAILED OPERATING DESCRIPTION

INTRODUCTION

The NCP1615 is designed to optimize the efficiency of your PFC stage throughout the load range. In addition, it incorporates protection features for rugged operation. More generally, the NCP1615 is ideal in systems where cost effectiveness, reliability, low standby power and high efficiency are the key requirements:

- Current Controlled Frequency Foldback: the NCP1615 operates in Current Controlled Frequency Foldback (CCFF). In this mode, the circuit operates in classical Critical conduction Mode (CrM) when the inductor current exceeds a programmable value. When the current falls below this preset level, the NCP1615 linearly reduces the operating frequency down to a minimum of about 26 kHz when the input current reaches zero. CCFF maximizes the efficiency at both nominal and light load. In particular, standby losses are reduced to a minimum. Similar to frequency clamped CrM controllers, internal circuitry allows near−unity power factor at lower output power.
- Skip Mode: to further optimize the efficiency, the circuit skips cycles near the line zero crossing when the current is very low. This is to avoid circuit operation when the power transfer is particularly inefficient at the cost of input current distortion. When superior power factor is required, this function can be inhibited by offsetting the FFcontrol pin by 0.75 V.
- Integrated High Voltage Start−Up Circuit: Eliminates the need of external start−up components. It is also used to discharge the input filter capacitors when the line is removed.
- Line Removal Detection Circuitry: reduces input power by eliminating external resistors for discharging the input filter capacitor.
- PFCOK signal: the PFCOK pin is used to disable/enable the downstream converter. This pin is internally grounded when a fault is detected or when the PFC output voltage is below its regulation level.
- Fast Line / Load Transient Compensation (Dynamic Response Enhancer): since PFC stages exhibit low loop bandwidth, abrupt changes in the load or input voltage (e.g. at start−up) may cause an excessive over or undervoltage condition. This circuit limits possible deviations from the regulation level as follows:
  - The soft and fast Overvoltage Protections accurately limit the PFC stage maximum output voltage.
  - The NCP1615 dramatically speeds up the regulation loop when the output voltage falls below 95.5% of its regulation level. This function is disabled during power up to achieve a soft−start.
- Power Saving Mode: disables the controller and reduces the input power consumption of the system enabling very low input power applications.
- Standby Mode Input: allows the downstream converter to inhibit the PFC drive pulses when the load is reduced.
- Safety Protections: the NCP1615 permanently monitors the input and output voltages, the MOSFET current and the die temperature to protect the system during fault conditions making the PFC stage extremely robust and reliable. In addition to the bulk overvoltage protection, the NCP1615 include:
  - Maximum Current Limit: the circuit senses the MOSFET current and turns off the power switch if the maximum current limit is exceeded. In addition, the circuit enters a low duty−ratio operation mode when the current reaches 150% of the current limit as a result of inductor saturation or a short of the bypass/boost diode.
  - Undervoltage Protection (UVP): this circuit turns off when it detects that the output voltage is below 12% of the voltage reference (typically). This feature protects the PFC stage if the ac line is too low or if there is a failure in the feedback network (e.g., bad connection).
  - Bulk Undervoltage Detection (BUV): the circuit monitors the output voltage to detect when the PFC stage cannot regulate the bulk voltage (BUV fault). When the BUV fault is detected, the control pin is gradually discharged followed by the grounding of the PFCOK pin, to disable the downstream converter.
  - Brownout Detection: the circuit detects low ac line conditions and stops operation thus protecting the PFC stage from excessive stress.
  - Thermal Shutdown: an internal thermal circuitry disables the gate drive when the junction temperature exceeds the thermal shutdown threshold.
  - A latch fault input can be used to disable the controller if a fault is detected (i.e. supply overvoltage, overtemperature)
- Output Stage Totem Pole Driver: the NCP1615 incorporates a 0.5 A source / 0.8 A sink gate driver to efficiently drive most medium to high power MOSFETs.

HIGH VOLTAGE START−UP CIRCUIT

The NCP1615 integrate a high voltage start−up circuit accessible by the HV pin. The start−up circuit is rated at a maximum voltage of 700 V.

A start−up regulator consists of a constant current source that supplies current from a high voltage rail to the supply capacitor on the V_{CC} pin (C_{VCC}). The start−up circuit current (I_{start2}) is typically 12 mA. I_{start2} is disabled if the V_{CC} pin is below $V_{CC(inhibit)}$. In this condition the start−up current is reduced to I_{start1}, typically 0.5 mA. The internal high voltage start−up circuit eliminates the need for external

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start−up components. In addition, this regulator reduces no load power and increase the system efficiency as it uses negligible power in the normal operation mode

Once C_{VCC} is charged to the start−up threshold, $V_{CC(on)}$, typically 17 V, the start−up regulator is disabled and the controller is enabled. The start−up regulator remains disabled until V_{CC} falls below the lower supply threshold, $V_{CC(off)}$, typically 9.0 V, is reached. Once reached, the PFC controller is disabled reducing the bias current consumption of the IC.

The controller is disabled once a fault is detected. The controller will restart next time V_{CC} reaches $V_{CC(on)}$ or after all non−latching faults are removed.

The supply capacitor provides power to the controller during power up. The capacitor must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is building up. Otherwise, V_{CC} will collapse and the controller will turn off. The operating IC bias current, I_{CC5}, and gate charge load at the drive outputs must be considered to correctly size C_{VCC}. The increase in current consumption due to external gate charge is calculated using Equation 1.

$$I_{CC(gatecharge)} = f \cdot Q_G \qquad \text{(eq. 1)}$$

where f is the operating frequency and Q_G is the gate charge of the external MOSFETs.

OPERATING MODE

The NCP1615 PFC controller achieves power factor correction using the novel Current Controlled Frequency Foldback (CCFF) topology. In CCFF the circuit operates in the classical critical conduction mode (CrM) when the inductor current exceeds a programmable value. Once the current falls below this preset level, the frequency is linearly reduced, reaching about 26 kHz when the current is zero.

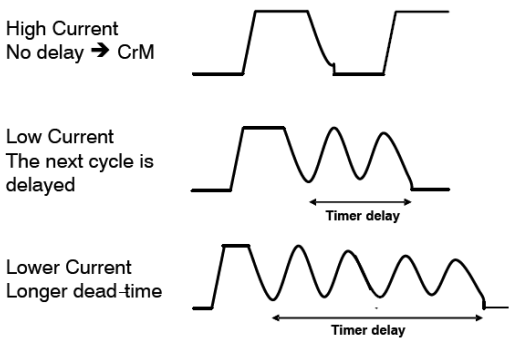


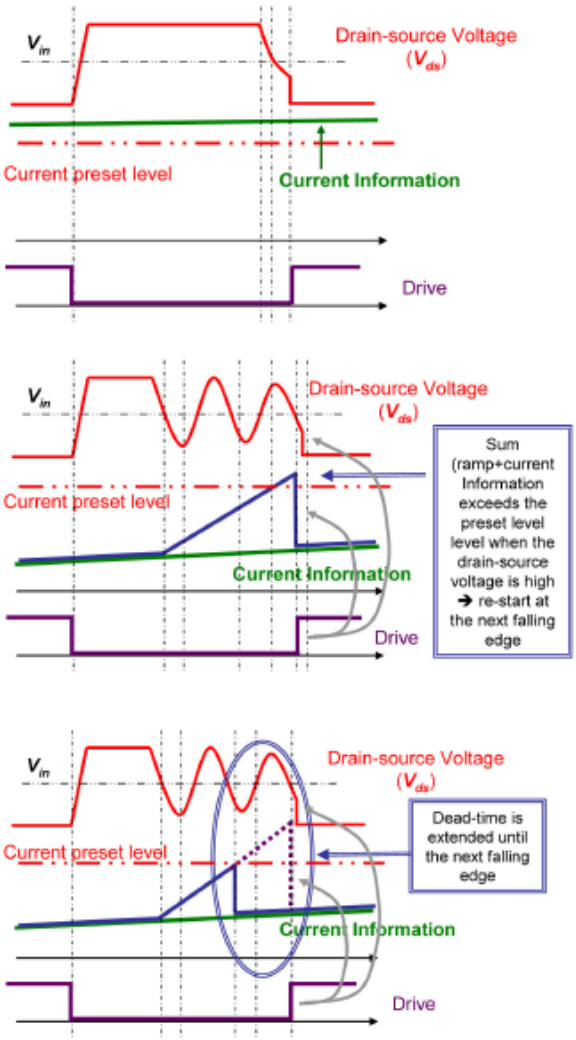
Figure 3. CCFF Operation

As illustrated in the top waveform in Figure 3, at high load, the boost stage operates in CrM. As the load decreases, the controller operates in a controlled frequency discontinuous mode.

Figure 4 details CCFF operation. A voltage representative of the input current (“current information”) is generated. If this signal is higher than a 2.5 V internal reference (named “Dead−Time Ramp Threshold”), there is no deadtime and the circuit operates in CrM. If the current information signal is lower than the 2.5 V threshold, deadtime is added. The deadtime is the time necessary for the internal ramp to reach 2.5 V from the current information floor. Hence, the lower the current information is, the longer the deadtime. When the current information is 0.75 V, the deadtime is 15 μs.

To further reduce the losses, the MOSFET turn on is further delayed until its drain−source voltage is at its valley. As illustrated in Figure 4, the ramp is synchronized to the drain−source ringing. If the ramp exceeds the 2.5 V threshold while the drain−source voltage is below V_{in}, the ramp is extended until it oscillates above V_{in} so that the drive will turn on at the next valley.

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Top: CrM operation when the current information exceeds the preset level during the demagnetization phase
Middle: the circuit re−starts at the next valley if the sum (ramp + current information) exceeds the preset level during the dead−time, while the drain−source voltage is high
Bottom: the sum (ramp + current information) exceeds the preset level while during the dead−time, the drain−source voltage is low. The circuit skips the current valley and re−starts at the following one.

Figure 4. Dead−Time Generation

CURRENT INFORMATION GENERATION

The FFcontrol pin sources a current that is representative of the input current. In practice, $I_{FFcontrol}$ is built by multiplying the internal control signal (V_{REGUL}, i.e., the internal signal that controls the on time) by the internal sense voltage (V_{SENSE}) that is proportional to the input voltage seen on the HV pin (see Figure 5).

The multiplier gain (*Km* of Figure 5) is four times less in high line conditions (that is when the "LLine" signal from the brownout block is in low state) so that $I_{FFcontrol}$ provides a voltage representative of the input current across resistor R_{FF} placed between the FFcontrol pin and ground. The FFcontrol voltage, $V_{FFcontrol}$, is representative of the current information.

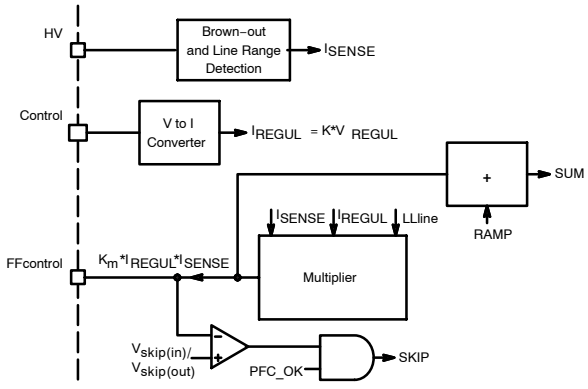


Figure 5. Generation of the Current Information in the NCP1615

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SKIP MODE

As illustrated in Figure 5 the circuit also skips cycles near the line zero crossing where the current is very low and subsequently the voltage across RFF is low. A comparator monitors $V_{FFcontrol}$ and inhibits the switching operation when $V_{FFcontrol}$ falls below the skip level, $V_{skip(in)}$, typically 0.65 V. Switching resumes when $V_{FFcontrol}$ exceeds the skip exit threshold, $V_{skip(out)}$, typically 0.75 V (100 mV hysteresis). This function disables the driver to reduce power dissipation when the power transfer is particularly inefficient at the expense of slightly increased input current distortion. When superior power factor is needed, this function can be inhibited offsetting the FFcontrol pin by 0.75 V. The skip mode capability is disabled whenever the PFC stage is not in nominal operation represented by the PFCOK signal.

The circuit does not abruptly interrupt the switching when $V_{FFcontrol}$ falls below $V_{skip(in)}$. Instead, the signal V_{TON} that controls the on time is gradually decreased by grounding the V_{REGUL} signal applied to the V_{TON} processing block shown in Figure 10. Doing so, the on time smoothly decays to zero in 3 to 4 switching periods typically. Figure 6 shows the practical implementation of the FFcontrol circuitry.

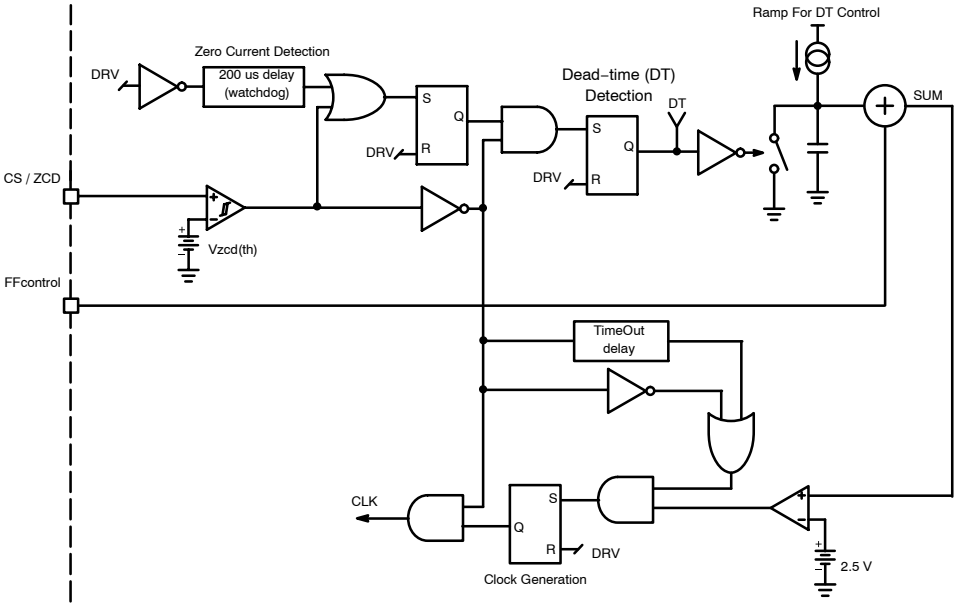


Figure 6. CCFF Practical Implementation

CCFF maximizes the efficiency at both nominal and light load. In particular, the standby losses are reduced to a minimum. Also, this method avoids that the system stalls or jumps between drain voltage valleys. Instead, the circuit acts so that the PFC stage transitions from the n valley to (n + 1) valley or vice versa from the n valley to (n − 1) cleanly as illustrated by Figure 7.

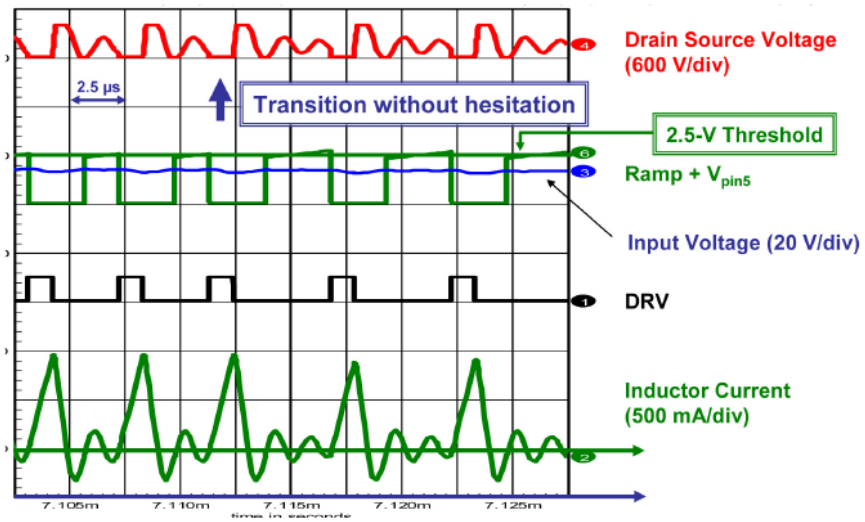


Figure 7. Valley Transitions Without Valley Jumping

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ON TIME MODULATION

Let's analyze the ac line current absorbed by the PFC boost stage. The initial inductor current at the beginning of each switching cycle is always zero. The coil current ramps up when the MOSFET is on. The slope is (Vin/L) where L is the coil inductance. At the end of the on time period (t_1), the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is (t_2). In some cases, the system enters then the dead−time (t_3) that lasts until the next clock is generated.

One can show that the ac line current is given by:

$$I_{in} = V_{in}\left[\frac{t_1(t_1 + t_2)}{2TL}\right] \qquad \text{(eq. 2)}$$

Where $T = (t_1 + t_2 + t_3)$ is the switching period and V_{in} is the ac line rectified voltage.

In light of this equation, we immediately note that I_{in} is proportional to V_{in} if $[t_1*(t_1 + t_2)/T]$ is a constant.

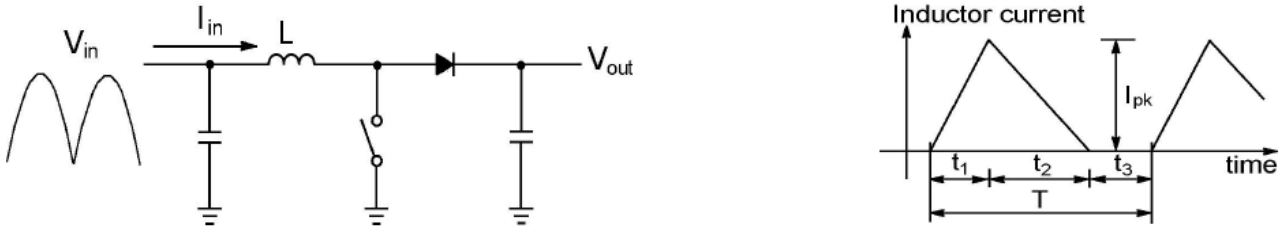


Figure 8. PFC Boost Converter (left) and Inductor Current in DCM (right)

The NCP1615 operates in voltage mode. As portrayed by Figure 9, t_1 is controlled by the signal V_{TON} generated by the regulation block and an internal ramp as follows:

$$t_1 = \frac{C_{ramp} \cdot V_{TON}}{I_{ch}} \qquad \text{(eq. 3)}$$

The charge current is constant at a given input voltage (as mentioned, it is four times higher at high line compared to its value at low line). C_{ramp} is an internal timing capacitor.

The output of the regulation block, $V_{Control}$, is linearly transformed into the signal V_{REGUL} varying between 0 and 1.5 V. V_{REGUL} is the voltage that is injected into the PWM section to modulate the MOSFET duty ratio. The NCP1615 includes circuitry that processes V_{REGUL} to generate the V_{TON} signal that is used in the PWM section (see Figure 10). It is modulated in response to the deadtime sensed during the precedent current cycles, that is, for a proper shaping of the ac line current. This modulation leads to:

$$V_{TON} = \frac{T \cdot V_{REGUL}}{t_1 + t_2} \qquad \text{(eq. 4)}$$

or

$$V_{TON} \cdot \frac{(t_1 + t_2)}{T} = V_{REGUL}$$

Given the low regulation bandwidth of the PFC systems, $V_{Control}$ and thus V_{REGUL} are slow varying signals. Hence, the $(V_{ton}*(t_1 + t_2)/T)$ term is substantially constant. Provided that during t_1 it is proportional to V_{TON}, Equation 2 leads to:

$$I_{in} = k \cdot V_{in},$$

where k is a constant.

$$k = \text{constant} = \left[\frac{1}{2L} \cdot \frac{V_{REGUL}}{V_{REGUL(MAX)}} \cdot t_{on(MAX)}\right]$$

Where $t_{on(MAX)}$ is the maximum on time obtained when V_{REGUL} is at its maximum level, $V_{REGUL(MAX)}$. The parametric table shows that $t_{on(MAX)}$ is equal to 25 μs ($t_{ON(LL)}$) at low line and to 8.1 μs ($t_{on(HL)}$) at high line. Hence, we can rewrite the above equation as follows:

$$I_{in} = \frac{V_{in} \cdot t_{on(LL)}}{2 \cdot L} \cdot \frac{V_{REGUL}}{V_{REGUL(MAX)}}$$

at low line.

$$I_{in} = \frac{V_{in} \cdot t_{on(HL)}}{2 \cdot L} \cdot \frac{V_{REGUL}}{V_{REGUL(MAX)}}$$

From these equations, we can deduce the expression of the average input power at low line as shown below:

$$P_{in(ave)} = \frac{V_{in,rms}^{\ 2} \cdot t_{on(LL)} \cdot V_{REGUL}}{2 \cdot L \cdot V_{REGUL(MAX)}}$$

The input power at high line is shown below:

$$P_{in(ave)} = \frac{V_{in,rms}^{\ 2} \cdot t_{on(HL)} \cdot V_{REGUL}}{2 \cdot L \cdot V_{REGUL(MAX)}}$$

Hence, the maximum power that can be delivered by the PFC stage at low line is given by equation below:

$$P_{in(MAX)} = \frac{V_{in,rms}^{\ 2} \cdot t_{on(LL)}}{2 \cdot L}$$

The maximum power at high line is given by the equation below:

$$P_{in(MAX)} = \frac{V_{in,rms}^{\ 2} \cdot t_{on(HL)}}{2 \cdot L}$$

The input current is then proportional to the input voltage resulting in a properly shaped ac line current.

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One can note that this analysis is also valid in CrM operation. This condition is just a particular case of this functioning where (t_3 = 0), which leads to (t_1 + t_2 = T) and (V_{TON} = V_{REGUL}). That is why the NCP1615 automatically adapts to the conditions and transitions from DCM to CrM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

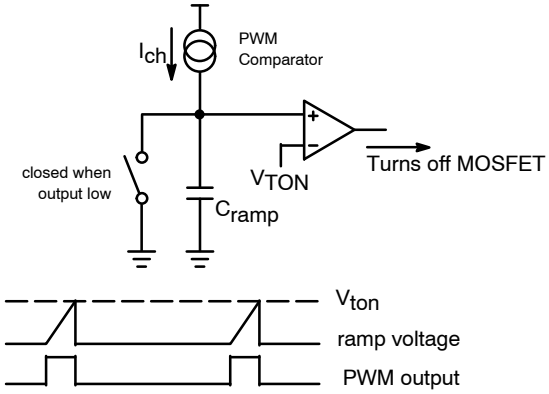


Figure 9. PWM Circuit and Timing Diagram

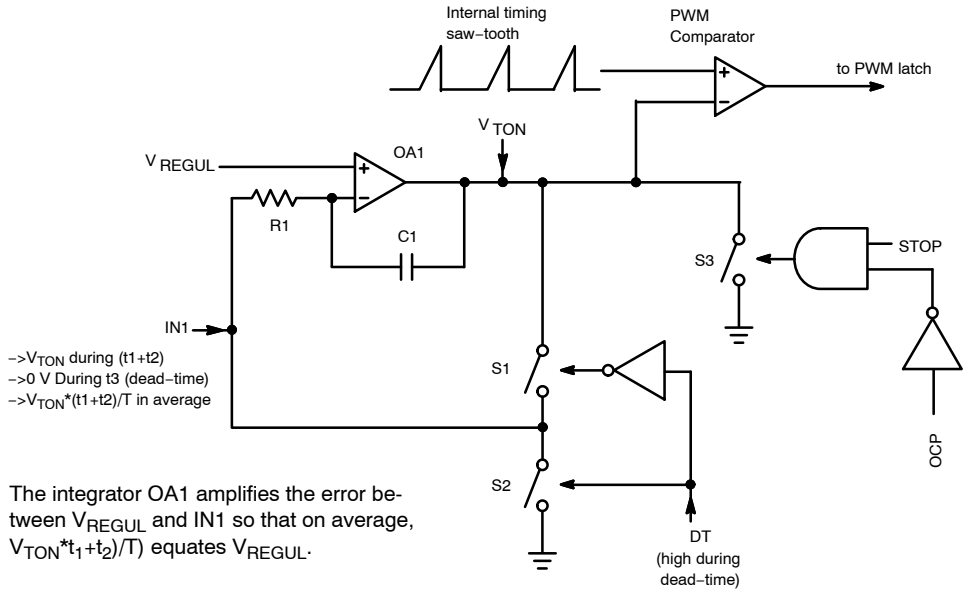


Figure 10. V_{TON} Processing Circuit

It is important to note that the "VTON processing circuit" compensates for long interruption of the driver activity by grounding the V_{TON} signal as shown in Figure 10. Long driver interruptions are represented by the STOP signal. Such faults (excluding OCP) are BUV_fault, OVP, BONOK, OverStress, SKIP, staticOVP, Fast−OVP, RestartNOK and OFF mode. Otherwise, a long off time will be interpreted as normal deadtime and the circuit would over dimension V_{TON} to compensate it. Grounding the V_{TON} signal leads to a short soft−start period due to ramp up of V_{TON}. This helps reduce the risk of acoustic noise.

VOLTAGE REFERENCE

A transconductance error amplifier regulates the PFC output voltage, V_{bulk}, by comparing the PFC feedback signal to an internal reference voltage, V_{REF}. The feedback signal is applied to the inverting input and the reference is connected to the non−inverting input of the error amplifier. A resistor divider scales down V_{bulk} to generate the PFC feedback signal. V_{REF} is trimmed during manufacturing to achieve an accuracy of ± 2.4%.

REGULATION BLOCK AND LOW OUTPUT VOLTAGE DETECTION

A transconductance error amplifier (OTA) with access to the inverting input and output is provided. Access to the inverting input is provided by the FB pin and the output is accessible through the Control pin. The OTA features a typical transconductance gain, g_m, of 210 μS. The amplifier source and sink currents, $I_{EA(SRC)}$ and $I_{EA(SNK)}$, are typically 20 μA.

The output voltage of the PFC stage is typically scaled down by a resistors divider and fed into the FB pin. The pin input bias current is minimized (less than 500 nA) to allow the use of a high impedance feedback network. At the same time, the bias current is enough to effectively ground the FB if the pin is open or floating.

The output of the error amplifier is brought to the Control pin for external loop compensation. The compensation network on the Control pin is selected to filter the bulk voltage ripple such that a constant control voltage is maintained across the ac line cycle and provide adequate phase boost. Typically a type 2 network is used, to set the

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regulation bandwidth below about 20 Hz and to provide a decent phase boost.

The minimum control voltage, $V_{Control(MIN)}$ is typically 0.5 V and it is set by an internal diode drop or V_F. maximum control voltage, $V_{Control(MAX)}$ is typically 4.5 V. Therefore, the $V_{Control}$ swing is 4 V. $V_{Control}$ is offset down by a V_F and scaled down by a resistor divider before it connects to the "V_{TON} processing block" and the PWM section as shown in Figure 11. The output of the regulation block is a signal ("V_{REGUL}" of the block diagram) that varies between 0 and a maximum value corresponding to the maximum on−time.

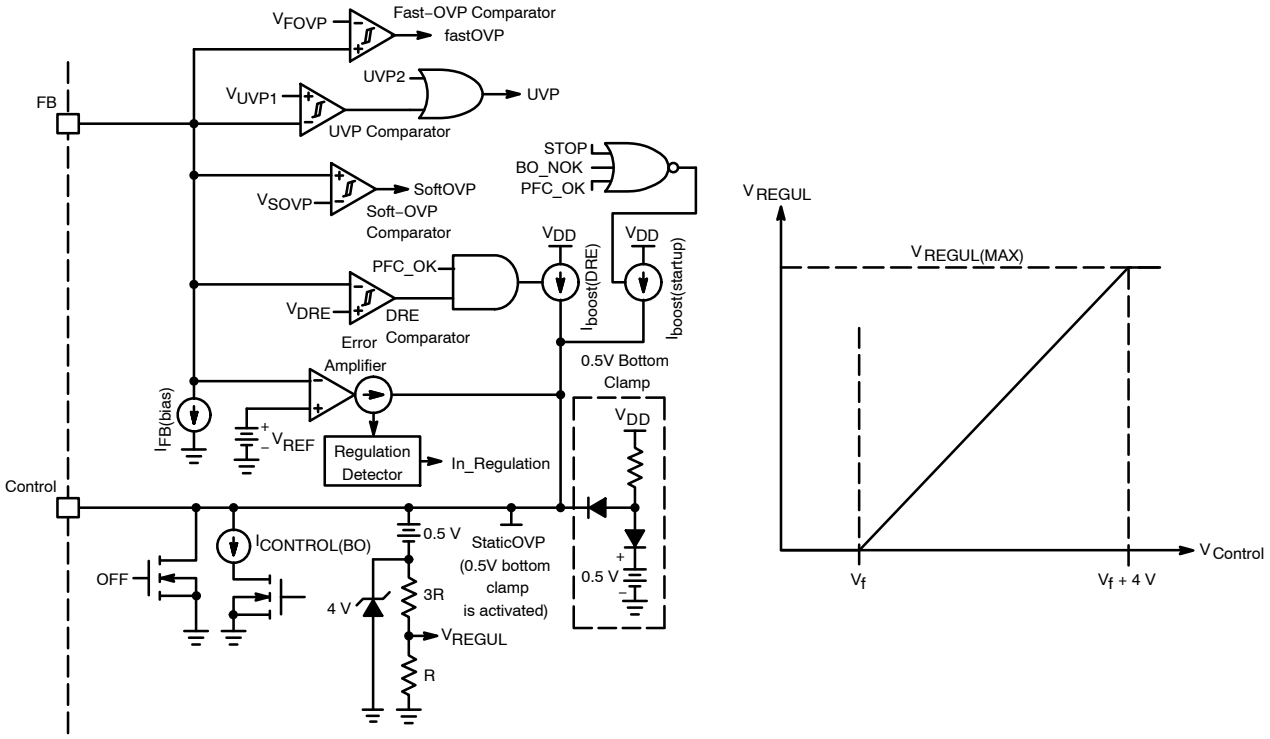


Figure 11. Regulation Block Diagram (left) Correspondence Between $V_{control}$ and V_{REGUL} (right)

Given the low bandwidth of the regulation loop, abrupt variations of the load, may result in excessive over or undershoots.

The NCP1615 embeds a "dynamic response enhancer" circuitry (DRE) that limits output voltage undershoots. An internal comparator monitors the FB pin and if its voltage falls below 95.5% of its nominal value, it enables a pull−up current source, $I_{boost(DRE)}$, to increase the Control voltage by charging the compensation network and bring the system into regulation. The total current sourced from the Control Pin during DRE, $I_{Control(DRE)}$, is typically 220 μA. This effectively appears as a 10x increase in the loop gain.

A reduced current source, $I_{boost(start−up)}$ (typically 80 μA), is enabled to speed up the start−up sequence and achieve a faster start−up time. $I_{boost(start−up)}$ is disabled when faults (i.e. Brownout) are detected.

Voltage overshoots are limited by the Soft Overvoltage Protection (SOVP) connected to the FB pin. The circuit reduces the power delivery when the output voltage exceeds 105% of its desired level. The NCP1615 does not abruptly interrupt the switching. Instead, the V_{TON} signal that controls the on time is gradually decreased by grounding the V_{REGUL} signal applied to the V_{TON} processing block as shown in Figure 10. Doing so, the on time smoothly decays to zero in 3 to 4 cycles. If the output voltage keeps increasing, the Fast Overvoltage Protection (FOVP) comparator immediately disables the driver when the output voltage exceeds 107% of its desired level.

The Undervoltage (UVP) Comparator monitors the FB voltage and disables the PFC stage if the bulk voltage falls below 12% of its regulation level. Once an undervoltage fault is detected, the PFCOK signal goes low to disable the downstream converter and the control capacitor is grounded.

The Bulk Undervoltage Comparator (BUV) monitors the bulk voltage and disables the controller if the BUV voltage falls below the BUV threshold. The BUV threshold is a ratio of V_{REF} and it is given by $K_{BUV/VREF}$, typically 76% of V_{REF}. Once a BUV fault is detected the controller is disabled and the PFCOK signal goes low. The Control capacitor is slowly discharged until it falls below the skip level. The discharge delay forces a minimum off time for the downstream converter. Once the discharge phase is complete the circuit may attempt to restart if V_{CC} is above $V_{CC(on)}$. Otherwise, it will restart at the next $V_{CC(on)}$. The BUV fault is blanked while the PFCOK signal is low (i.e. during start−up) to allow a correct start−up sequence.

The input to the Error Amplifier, the soft-OVP, UVP and DRE Comparators is the FB pin. The table below shows the relationship between the nominal output voltage, $V_{out(NOM)}$, and the DRE, soft-OVP, Fast-OVP and UVP levels.

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Parameter	Symbol/Value
Nominal Output Voltage	$V_{out(NOM)}$
DRE Threshold	$V_{out(NOM)}$*95.5%
Soft−OVP	$V_{out(NOM)}$*105%
UVP	$V_{out(NOM)}$*12%
Fast−OVP	$V_{out(NOM)}$*107%

CURRENT SENSE AND ZERO CURRENT DETECTION

The NCP1615 combines the PFC current sense and zero current detectors (ZCD) in a single input terminal, CS/ZCD. Figure 12 shows the circuit schematic of the current sense and ZCD detectors.

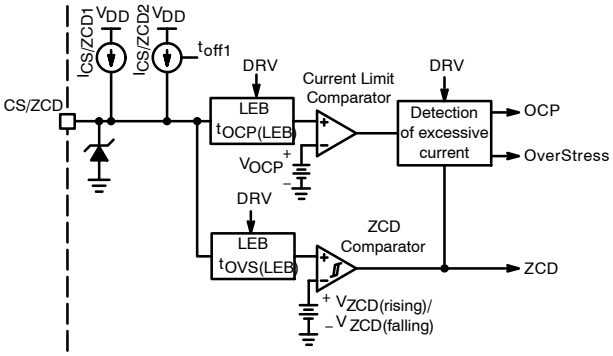


Figure 12. PFC Current Sense and ZCD Detectors Schematic

Current Sense

The PFC Switch current is sensed across a sense resistor, R_{sense}, and the resulting voltage ramp is applied to the CS/ZCD pin. The current signal is blanked by a leading edge blanking (LEB) circuit. The blanking period eliminates the leading edge spike and high frequency noise during the switch turn−on event. The LEB period, $t_{OCP(LEB)}$, is typically 200 ns. The Current Limit Comparator disables the driver once the current sense signal exceeds the overcurrent threshold, V_{OCP}, typically 0.5 V.

PFC Zero Current Detection

The CS pin is also designed to receive a signal from an auxiliary winding to detect the inductor demagnetization or for zero current detection (ZCD). This winding is commonly known as a zero crossing detector (ZCD) winding. This winding provides a scaled version of the inductor voltage. Figure 13 shows the ZCD winding arrangement.

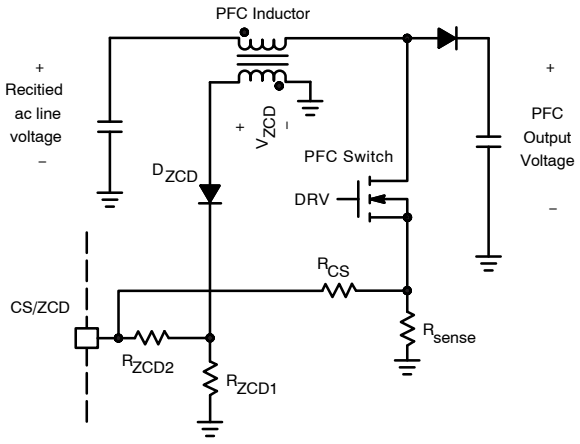


Figure 13. ZCD Winding Implementation

The ZCD winding voltage, V_{ZCD}, is positive while the PFC Switch is off and the inductor current decays to zero. V_{ZCD} drops to and rings around zero volts once the inductor is demagnetized. The ZCD winding voltage is applied through a diode, D_{ZCD}, to prevent this signal from distorting the current sense information during the on time. Therefore, the overcurrent protection is not impacted by the ZCD sensing circuitry.

As illustrated in Figure 12, an internal ZCD Comparator monitors the CS/ZCD voltage, $V_{CS/ZCD}$. The start of the demagnetization phase is detected (signal ZCD is high) once $V_{CS/ZCD}$ exceeds the ZCD arming threshold, $V_{ZCD(rising)}$, typically 750 mV. This comparator is able to detect ZCD pulses with a duration longer than 200 ns. When $V_{CS/ZCD}$ drops below the lower or trigger ZCD threshold, $V_{ZCD(falling)}$, the end of the demagnetization phase is detected and the driver goes high within 200 ns.

When a ZCD signal is not detected during start−up or during the off time, an internal watchdog timer, t_{off1}, initiates the next drive pulse. The watchdog timer duration is typically 200 μs. Once the watchdog timer expires the circuit senses the impedance at the CS/ZCD pin to detect if the pin is shorted and disable the controller. The CS/ZCD external components must be selected to avoid false fault detection. The recommended minimum impedance connected to the CS/ZCD pin is 3.9 kΩ. Practically, R_{CS} in Figure 13 must be higher than 3.9 kΩ.

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POWER SAVING MODE

The NCP1615 has a low current consumption mode known as power saving mode (PSM). The supply current consumption in this mode is below 100 μA. PSM operation is controlled by an external control signal. This signal is typically generated on the secondary side of the power supply and fed via an optocoupler.

The NCP1615 enters PSM in the absence of the control signal. The control signal is applied to the PSTimer pin. The block diagram is shown in Figure 14. Power saving mode operating waveforms are shown in Figure 15.

The NCP1615 controller starts once V_{CC} reaches $V_{CC(on)}$ and no faults are present. The PSTimer pin is held at ground until the PFCOK signal goes high. This ensures the time to enter PSM is always constant.

Once the PFCOK signal goes high, the current source on the PSTimer pin, $I_{PSTimer1}$, is enabled. $I_{PSTimer1}$ is typically 5.9 μA. The current source charges the capacitor connected from this pin to ground. Once $V_{PSTimer}$ reaches $V_{PSTimer2}$ a 2nd current source, $I_{PSTimer2}$, is enabled to speed up the charge of C_{PSM}. $V_{PSTimer2}$ and $I_{PSTimer2}$ are typically 1 V and 1 mA, respectively. The controller enters PSM if the voltage on this exceeds, V_{PS_in}, typically 3.5 V. An external optocoupler or switch needs to pull down on this pin before its voltage reaches V_{PS_in} to prevent entering PSM. $I_{PSTimer}$ is disabled once the controller enters PSM. A resistor between this pin and ground discharges the PSTimer capacitor. The controller exits PSM once $V_{PSTimer}$ drops below V_{PS_out}, typically 0.5 V. At this time the start−up circuit is enabled to charge V_{CC} up to $V_{CC(on)}$. Once V_{CC} charges to $V_{CC(on)}$ the capacitor on the PSTimer pin is discharged with an internal pull down transistor. The transistor is disabled once the PFCOK signal goes high. The time to enter PSM mode is calculated using Equations 3 through 7. The time to exit PSM mode is calculated using Equation 8.

$$t_{PSM(in)} = t_{PSM(in1)} + t_{PSM(in2)} \quad \text{(eq. 5)}$$

$$t_{PSM(in1)} \approx -R_{PSM}C_{PSM} \cdot \ln\left(1 - \frac{V_{PSTimer2}}{I_{PSTimer1} * R_{PSM}}\right) \quad \text{(eq. 6)}$$

$$t_{PSM(in2)} \approx -R_{PSM}C_{PSM} \cdot \ln\left(1 - \frac{V_{PS_in} - V_{PSTimer2}}{I_{PSTimer2} * R_{PSM}}\right) \quad \text{(eq. 7)}$$

$$t_{PSM(out)} = -R_{PSM}C_{PSM} \cdot \ln\left(\frac{V_{PS_out}}{V_{PS_in}}\right) \quad \text{(eq. 8)}$$

During PSM, the start−up circuit on the HV pin maintains V_{CC} above $V_{CC(off)}$. The input filter capacitor discharge circuitry continues operation in PSM. The supply voltage is maintained in PSM by enabling the HV pin start−up circuit once V_{CC} falls below $V_{CC(PS_on)}$ (typically 11 V) and V_{HV} is at its minimum value as detected by the valley detection circuitry. The start−up circuit current in PSM is increased to I_{start2}, typically 12 mA, to reduce the time the start−up circuit is on and thus a lower voltage on the HV pin.

The start−up circuit is disabled once V_{CC} exceeds $V_{CC(PS_on)}$. A voltage offset is observed on V_{CC} while the start−up circuit is enabled due to the capacitor ESR. This will cause the start−up circuit to turn off because V_{CC} exceeds $V_{CC(PS_on)}$. Internal circuitry prevents the start−up circuit from turning on multiple times on the same ac line half−cycle. The start−up circuit will turn on the next half−cycle. Eventually, V_{CC} will be regulated several millivolts below $V_{CC(PS_on)}$. The offset is dependent on the capacitor ESR.

This architecture enables the start−up circuit for the exact amount of time needed to regulate V_{CC}. This results in a significant reduction in power dissipation because the average input voltage during which the start−up circuit is on is greatly reduced. Figure 15 shows operating waveforms while in PSM.

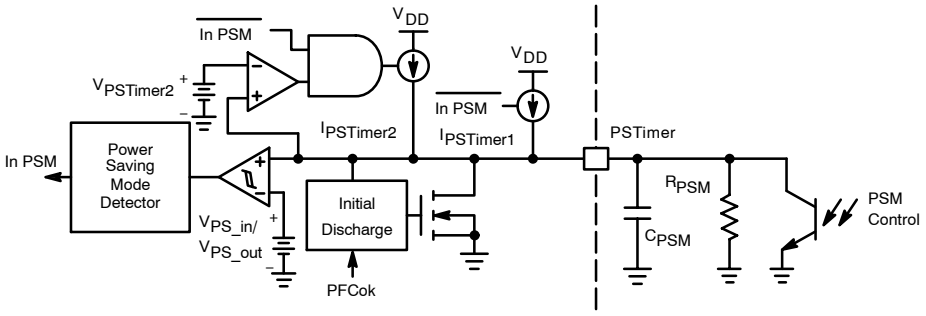


Figure 14. NCP1615 Power Saving Mode Control Block Diagram

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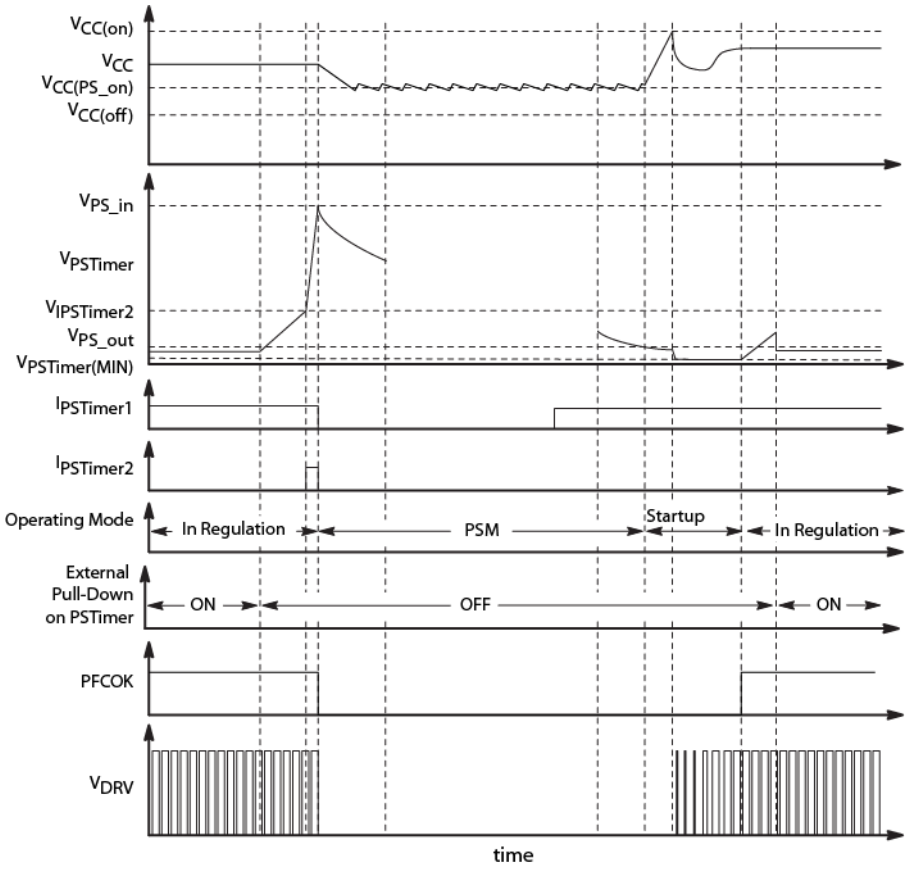


Figure 15. Power Saving Mode Operating Waveforms

Since the NCP1615 maintains the V_{CC} pin at $V_{CC(PS_on)}$ during PSM, the current consumption of the downstream converter can have an undesirable impact to power consumption. A simple mechanism to disconnect the supply voltage to the downstream converter during PSM is shown in Figure 16.

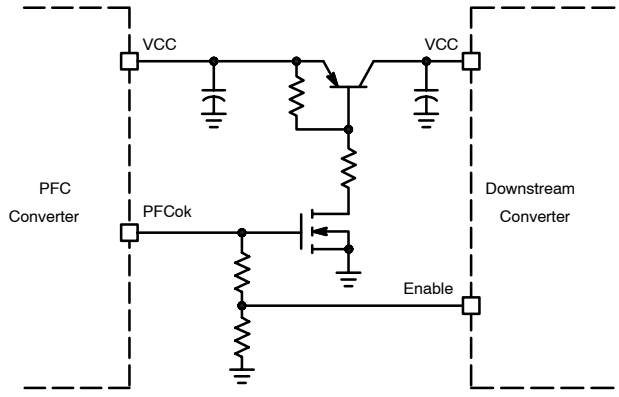


Figure 16. Downstream Converter Supply Removal Circuit

BYPASS/BOOST DIODE SHORT CIRCUIT AND INRUSH CURRENT PROTECTION

It may be possible to turn on the MOSFET while a high current flows through the inductor. Examples of this condition include start−up when large inrush current is present to charge the bulk capacitor. Traditionally, a bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current. If this diode is accidentally shorted or damaged, the MOSFET will operate at a minimum on time but the current can be very high causing a significant temperature increase.

The NCP1615 operates in a very low duty ratio to reduce the MOSFET temperature and protect the system in this “Over Stress” condition. This is achieved by disabling the drive signal if the $V_{ZCD(rising)}$ threshold is reached during the MOSFET conduction time. In this condition, a latch is set and the “OverStress” signal goes high. The driver is then disabled for a period determined by the overstress watchdog timer, t_{off2}, typically 1 ms. This longer delay leads to a very low duty−ratio operation to reduce the risk of overheating. This operation also protects the system in the event of a boost diode short.

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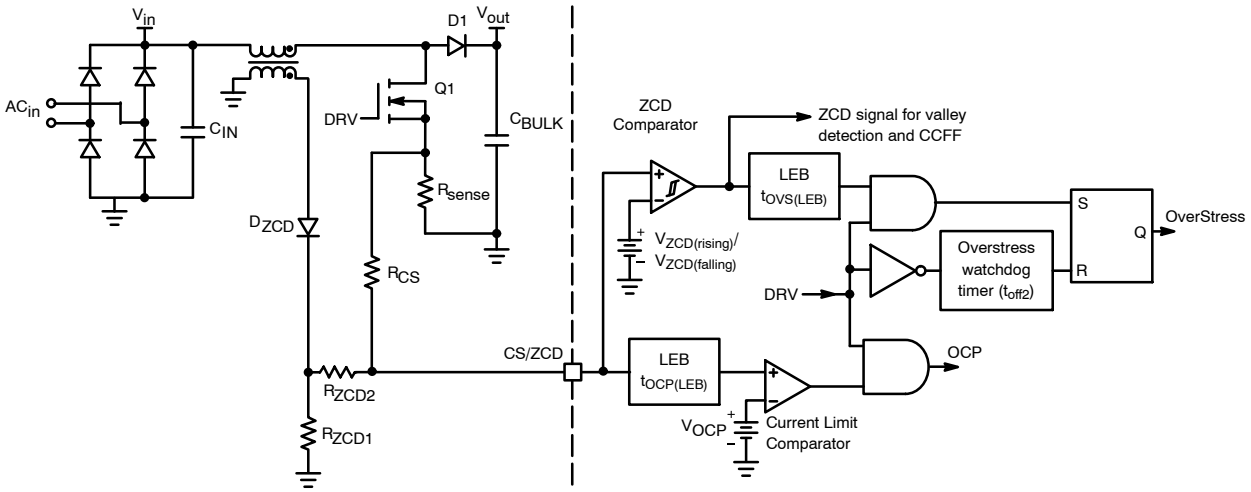


Figure 17. Current Sense and Zero Current Detection Blocks

PFCOK SIGNAL

The PFCOK pin provides a dedicated 5 V reference when the PFC stage is in regulation. The pin is internally grounded during the following conditions:

- During Start−Up: It remains low until the output voltage achieves regulation and the voltage stabilizes at the right level.
- Low Output Voltage: If the PFC stage output voltage is below the bulk undervoltage (BUV_Fault) level, this is indicative of a fault. The PFCOK signal then provides a means to disable and protect the downstream converter.
- Brownout fault is detected (after discharge of control capacitor).
- Low supply voltage: V_{CC} falls below $V_{CC(off)}$.
- Feedback undervoltage fault.
- Fault condition: A fault detected through the Fault pin.
- Open FB pin.
- Thermal Shutdown.
- Line voltage removal.

The circuit schematic of the PFCOK block is shown Figure 18.

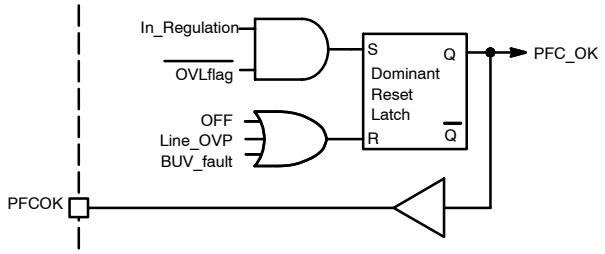


Figure 18. PFCOK Circuit Schematic

The PFCOK circuit monitors the current sourced by the OTA. The OTA current reaches zero when the output voltage has reached its nominal level. This is represented in the block diagram by the “In_Regulation” Signal. The PFCOK signal goes high when the current reaches zero or falls below zero. The start−up phase is then complete and the PFCOK signal goes high until a fault is detected.

Another signal considered before setting the PFCOK signal is the BUV. The PFCOK signal will remain low until the bulk voltage is above the undervoltage threshold. The PFCOK signal will go low if the bulk voltage drops below its undervoltage threshold.

BROWNOUT DETECTION

The HV pin provides access to the brownout and line voltage detectors. It also provides access to the input filter capacitor discharge circuit. The brownout detector detects main interruptions and the line voltage detector determines the presence of either 110 V or 220 V ac mains. Depending on the detected input voltage range device parameters are internally adjusted to optimize the system performance.

Line and neutral are diode “ORed” before connecting to the HV pin as shown in Figure 19. The diodes prevent the pin voltage from going below ground. A low value resistor in series with the diodes can be used for protection. A low value resistor is needed to reduce the voltage offset while sensing the line voltage.

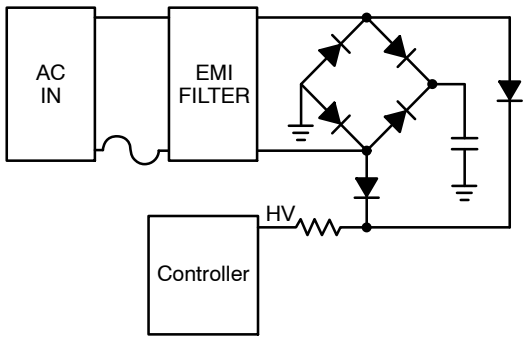


Figure 19. High−Voltage Input Connection

The controller is enabled once V_{HV} is above the brownout threshold, $V_{BO(start)}$, typically 111 V, and V_{CC} reaches $V_{CC(on)}$. Figure 20 shows typical power up waveforms.

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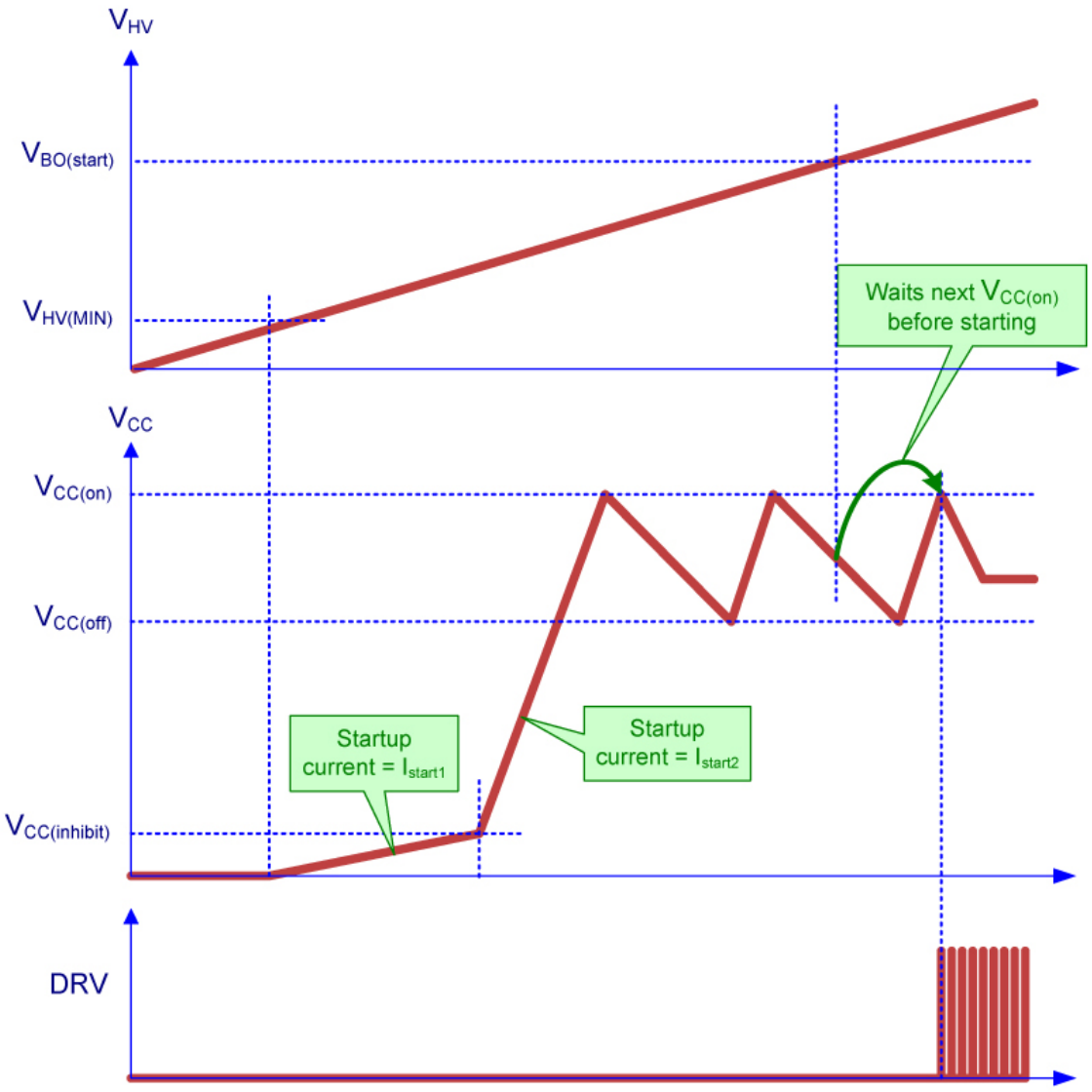


Figure 20. Start−Up Timing Diagram

A timer is enabled once V_{HV} drops below its disable threshold, $V_{BO(stop)}$, typically 100 V. The controller is disabled if V_{HV} doesn't exceed $V_{BO(stop)}$ before the brownout timer expires, t_{BO}, typically 54 ms. The timer is set long enough to ignore a single cycle dropout. The timer ramp starts charging once V_{HV} drops below $V_{BO(stop)}$. Figure 21 shows brownout detector waveforms during line dropout.

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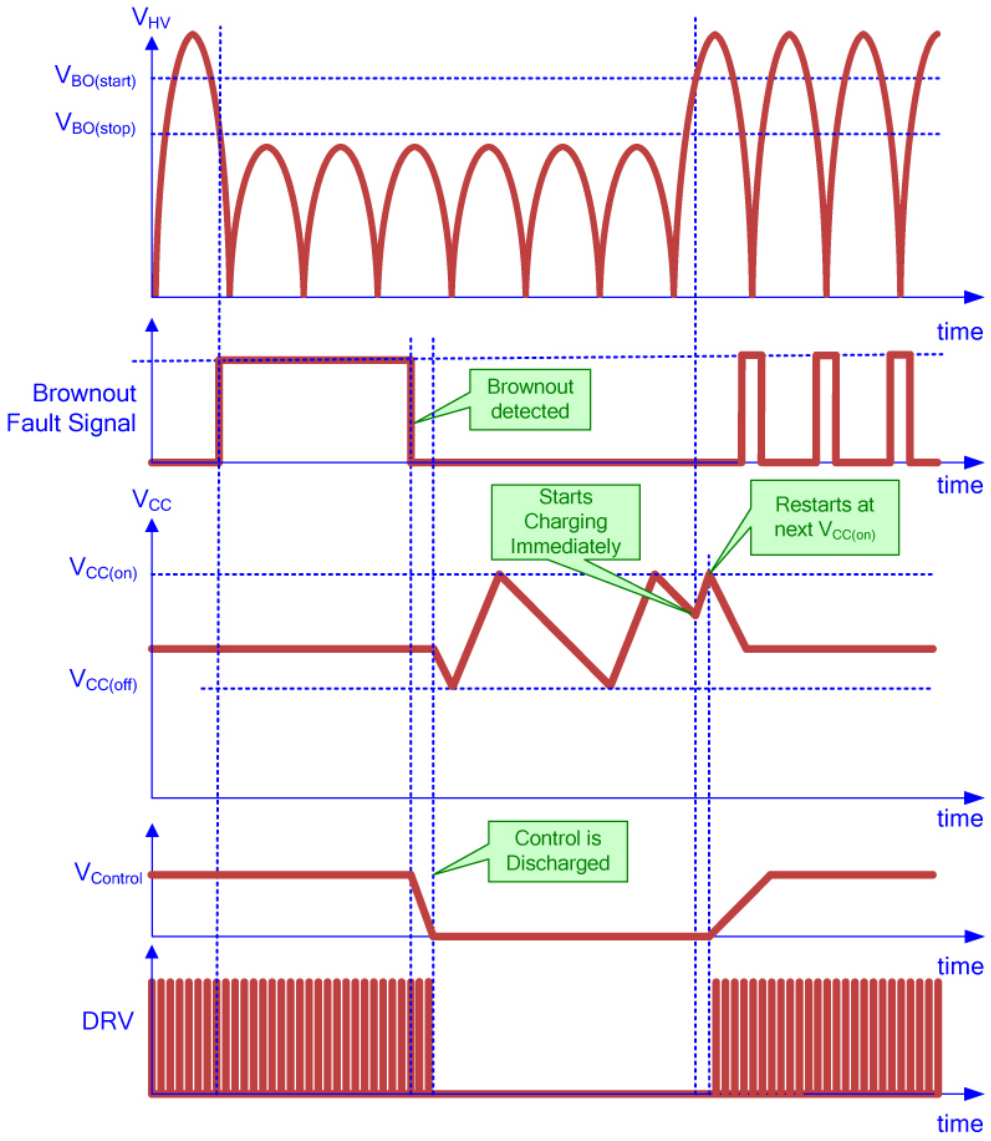


Figure 21. Brownout Operation During Line Dropout

LINE RANGE DETECTOR

The input voltage range is detected based on the peak voltage measured at the HV pin. The line range detection circuit allows more optimal loop gain control for universal (wide input mains) applications. Discrete values are selected for the PFC stage gain (feedforward) depending on the input voltage range.

The controller compares V_{HV} to the high line select threshold, $V_{lineselect(HL)}$, typically 250 V. Once V_{HV} exceeds $V_{lineselect(HL)}$, the PFC stage operates in "high line" (Europe/Asia) or "220 Vac" mode. In high line mode the loop gain is divided by four, thus the internal PWM ramp slope is four times steeper. The gain is divided by three, thus the ramp is three times steeper.

The default power−up mode of the controller is low line. The controller switches to "high line" mode if V_{HV} exceeds the high line select threshold for longer than the low to high line timer, $t_{delay(line)}$, typically 300 μs as long as it was not previously in high line mode. If the controller has switched to "low line" mode, it is prevented from switching back to "high line" mode until the valley detection circuit detects 8 valleys, even if $t_{delay(line)}$ has expired. In version C5, a lockout timer is started upon transitioning to "low line" mode. Instead of counting valleys, transition to "high line" mode is prevented until the lockout timer, $t_{line(lockout)}$ (typically 150 ms), expires. The timer and logic is included to prevent unwanted noise from toggling the operating line level.

In "high line" mode the high to low line timer, t_{line}, is enabled once V_{HV} falls below $V_{lineselect(LL)}$, typically 236 V. It is reset if V_{HV} exceeds $V_{lineselect(LL)}$. The controller switches back to "low line" mode if the high to low line timer expires. Figures 22 and 23 show operating waveforms of the line detector circuit. For Version C5, Figure 24 shows the operation of the lockout timer.

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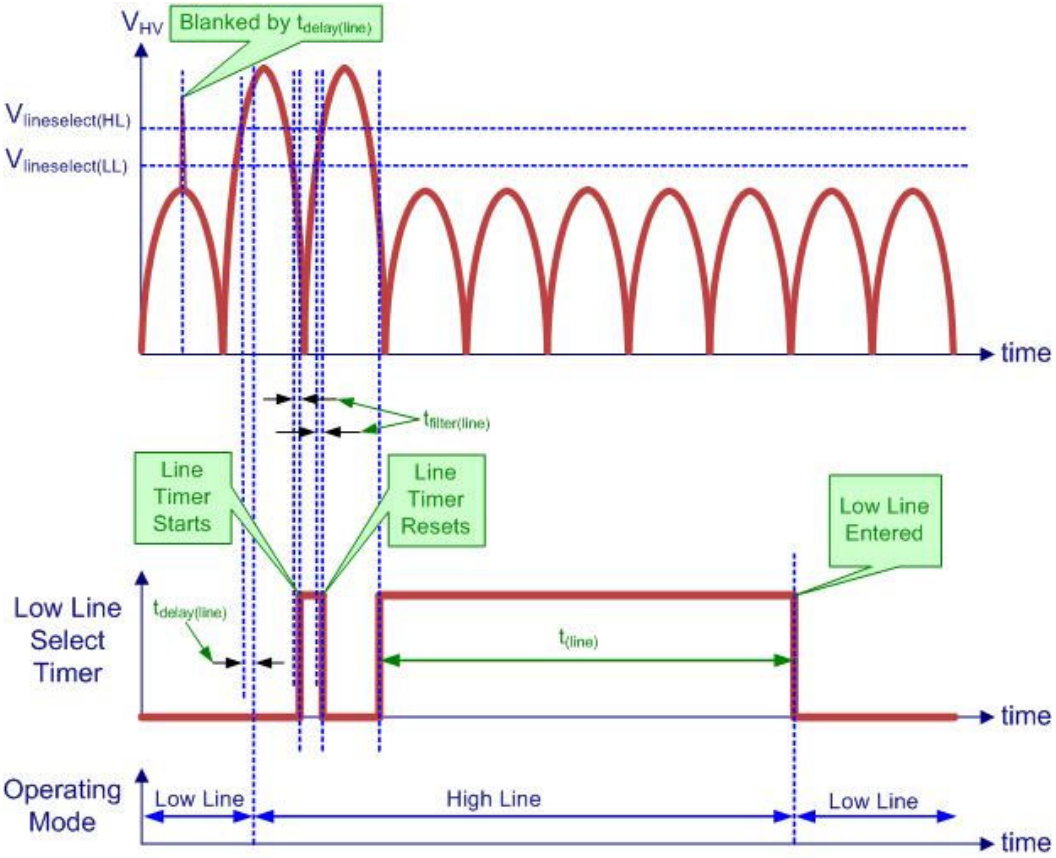


Figure 22. Line Detector Timing Waveforms

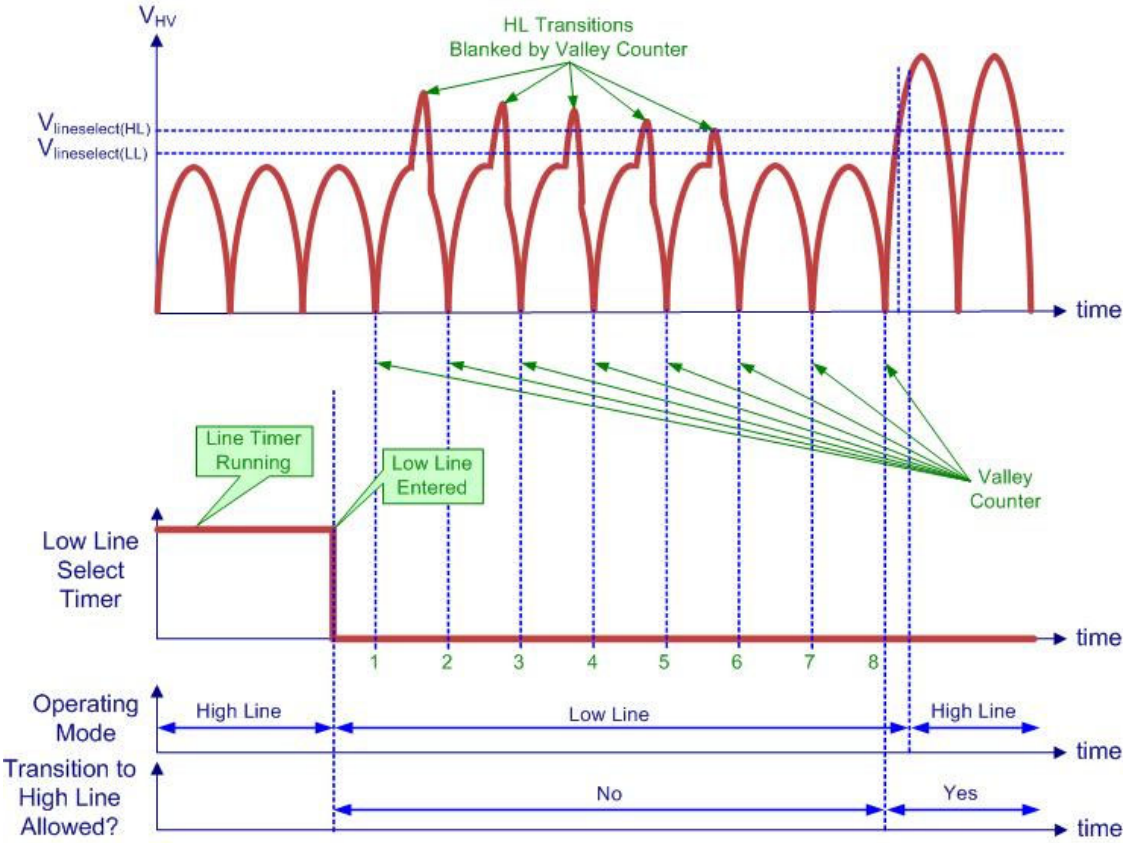


Figure 23. Valley Counter Operation (Version C4)

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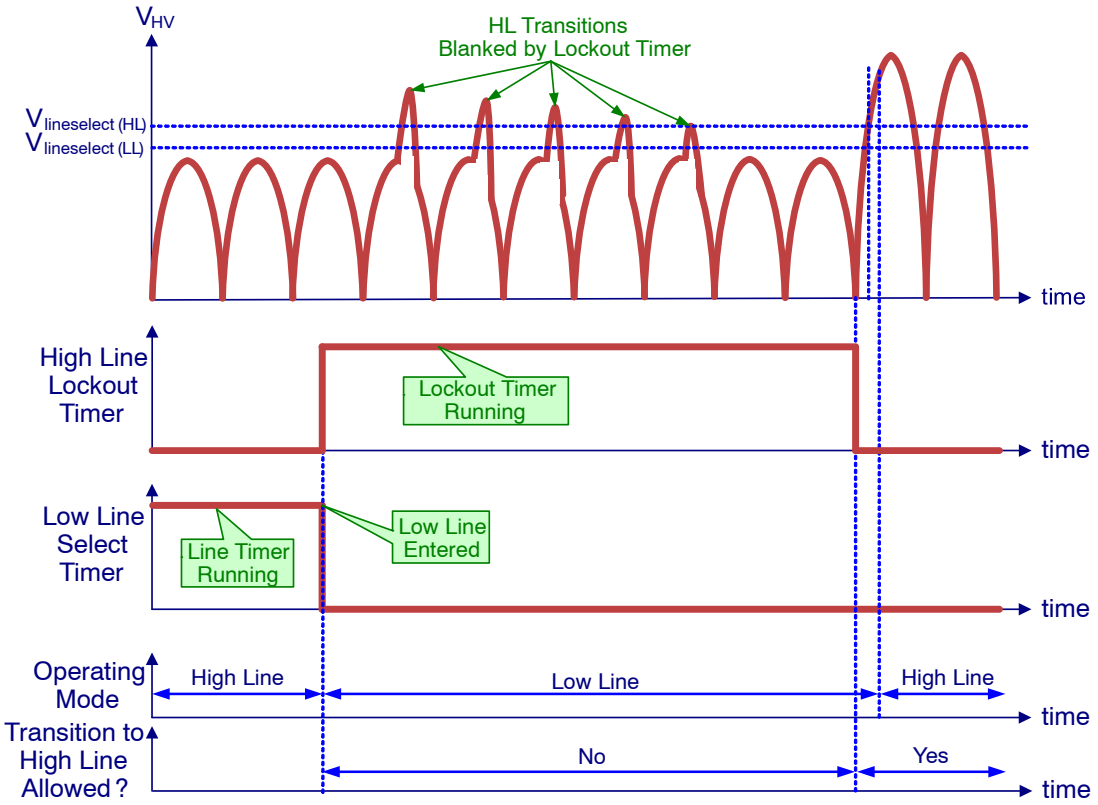


Figure 24. Lockout Timer Operation (Version C5)

OUTPUT DRIVE SECTION

The NCP1615 incorporates a large MOSFET driver. It is a totem pole optimized to minimize the cross conduction current during high frequency operation. It has a high drive current capability (−500/+800 mA) allowing the controller to effectively drive high gate charge power MOSFET.

The device maximum supply voltage, $V_{CC(MAX)}$, is 30 V. Typical high voltage MOSFETs have a maximum gate voltage rating of 20 V. The driver incorporates an active voltage clamp to limit the gate voltage on the external MOSFETs. The voltage clamp, $V_{DRV(high)}$, is typically 12 V with a maximum limit of 14 V.

The gate driver is kept in a sinking mode whenever the controller is disabled. This occurs when the Undervoltage Lockout is active or more generally whenever the controller detects a fault and enters off mode (i.e., when the "STDWN" signal of the block diagram is high).

OFF MODE

The controller is disabled and in a low current mode if any of the following faults are detected:

- Low supply input voltage. An undervoltage (or UVLO) fault is detected if V_{CC} falls below $V_{CC(off)}$.
- Thermal shutdown is activated due to high die temperature.
- A brownout fault is detected.
- The controller enters skip mode (see block diagram)
- A bulk undervoltage fault is detected.
- The controller enters latch mode.

Generally speaking, the circuit turns off when the conditions are not proper for desired operation. In this mode, the controller stops operation and most of the internal circuitry is disabled to reduce power consumption. Below is description of the IC operation in off mode:

- The driver is disabled.
- The controller maintains V_{CC} between $V_{CC(on)}$ and $V_{CC(off)}$.
- The following blocks or features remain active:
  - Brownout detector.
  - Thermal shutdown.
  - The undervoltage protection ("UVP") detector.
  - The overvoltage latch input remains active
- $V_{Control}$ is grounded to ensure a controlled start−up sequence once the fault is removed.
- The PFCOK pin is internally grounded.
- The output of the "V_{TON} processing block" is grounded.

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SYSTEM FAILURE DETECTION

When manufacturing a power supply, elements can be accidentally shorted or improperly soldered. Such failures can also occur as the system ages due to component fatigue, excessive stress, soldering faults, or external interactions. In particular, a pin can be grounded, left open, or shorted to an adjacent pin. Such open/short situations require a safe failure without smoke, fire, or loud noises. The NCP1615 integrates functions that ease meeting this requirement. Among them are:

- GND connection fault. If the GND pin is properly connected, the supply current drawn from the positive terminal of the VCC capacitor, flows out of the GND pin and returns to the negative terminal of the VCC capacitor. If the GND pin is disconnected, the internal ESD protection diodes provides a return path. An open or floating GND pin is detected if current flows in the CS/ZCD ESD diode. If current flow is detected for 200 μs, a fault is acknowledged and the controller stops operating.
- Open CS/ZCD Pin: A pull-up current source, $I_{CS/ZCD(bias1)}$, on the CS/ZCD pin allows detection of an open CS/ZCD pin. $I_{CS/ZCD1}$, is typically 1 μA. If the pin is open, the voltage on the pin will increase to the supply rail. This condition is detected and the controller is disabled.
- Grounded CS/ZCD Pin: If the CS/ZCD pin is grounded, the circuit cannot detect a ZCD transition, activating the watchdog timer (typically 200 μs). Once the watchdog timer expires, a pull-up current source, $I_{CS/ZCD2}$, sources 250 μA to pull-up the CS/ZCD pin. The driver is inhibited until the CS/ZCD pin voltage exceeds the ZCD arming threshold, $V_{ZCD(rising)}$, typically 0.75 V. Therefore, if the pin is grounded, the voltage on the pin will not exceed $V_{ZCD(rising)}$ and drive pulses will be inhibited. The external impedance should be above 3.9 kΩ to ensure correct operation.
- Boost or bypass diode short. The NCP1615 addresses the short situations of the boost and bypass diodes (a bypass diode is generally placed between the input and output high-voltage rails to divert this inrush current). Practically, the overstress protection is implemented to detect such conditions and forces a low duty ratio operation until the fault is removed.

FAULT INPUT

The NCP1615 includes a dedicated fault input accessible via the Fault pin. The controller can be latched by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.0 V. The controller is disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP_in)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 25 shows the architecture of the Fault input.

The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source $I_{Fault(OTP)}$, (typically 45.5 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP_in)}$. The 1615 latches off the controller after an overtemperature fault is detected. Figure 26 shows the typical latch−off function timing diagram.

An active clamp prevents the Fault pin voltage from reaching the upper latch threshold if the pin is open. To reach the upper threshold, the external pull-up current has to be higher than the pull-down capability of the clamp (set by $R_{Fault(clamp)}$ at $V_{Fault(clamp)}$). The upper fault threshold is intended to be used for an overvoltage fault using a Zener diode and a resistor in series from the auxiliary winding voltage, V_{AUX}. The controller is latched once V_{Fault} exceeds $V_{Fault(OVP)}$.

The Fault input signal is filtered to prevent noise from triggering the fault detectors. Upper and lower fault detector blanking delays, $t_{delay(OVP)}$ and $t_{delay(OTP)}$ are both typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay.

The controller bias current is reduced during power up by disabling most of the circuit blocks including $I_{Fault(OTP)}$. This current source is enabled once V_{CC} reaches $V_{CC(on)}$. A bypass capacitor is usually connected between the Fault and GND pins and it will take some time for V_{Fault} to reach its steady state value once $I_{Fault(OTP)}$ is enabled. To prevent false detection of an OTP fault during power up, a dedicated timer, $t_{blank(OTP)}$, blanks the OTP signal during power up. The $t_{blank(OTP)}$, duration is typically 5 ms.

Once the controller is latched, it is reset if a brownout condition is detected or if V_{CC} is cycled down to its reset level, $V_{CC(reset)}$. In the typical application these conditions occur only if the ac voltage is removed from the system. The internal latch also resets once the controller enters power saving mode. Prior to reaching $V_{CC(reset)}$ $V_{fault(clamp)}$ is set at 0 V.

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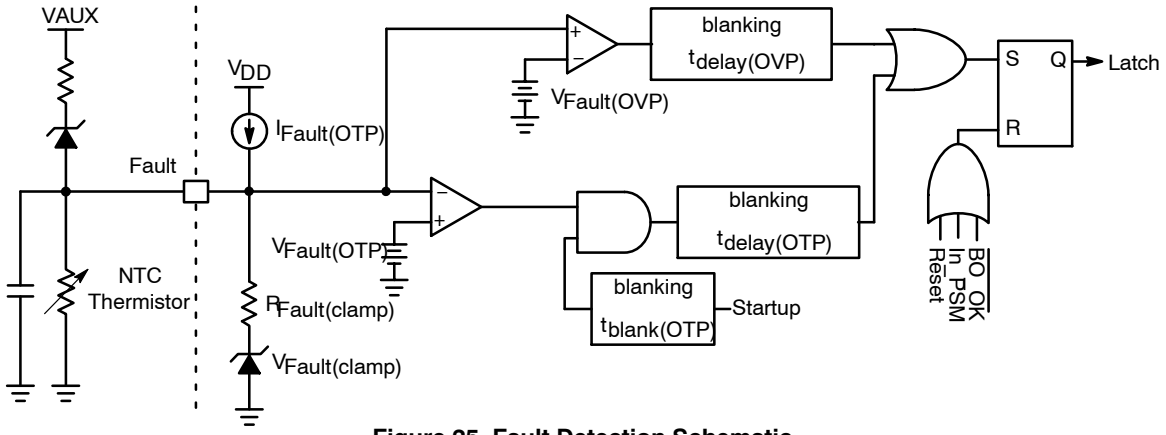


Figure 25. Fault Detection Schematic

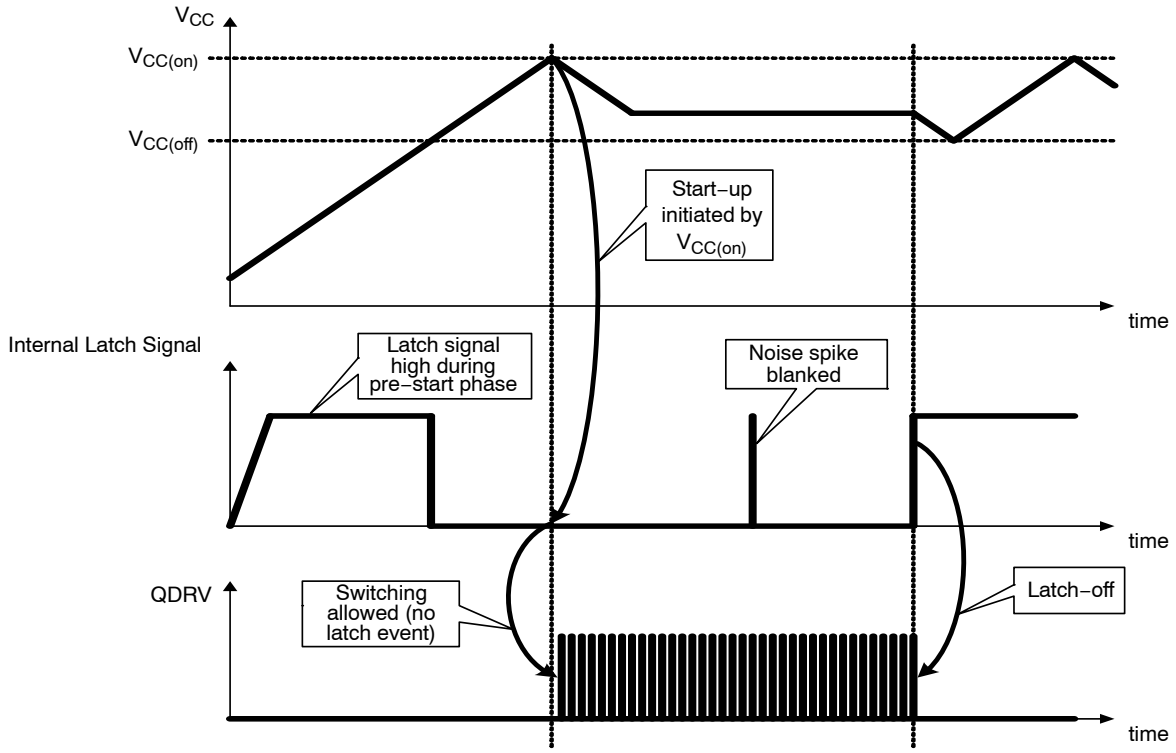


Figure 26. Latch−off Function Timing Diagram

STANDBY OPERATION

A signal proportional to the downstream converter output power is applied to the STDBY pin to enable standby mode operation. A STDBY voltage below the standby threshold, $V_{standby}$, typically 300 mV, forces the controller into a controlled burst mode, or standby mode.

In standby mode, the driver is disabled until the bulk voltage falls below the bulk restart level. At which point, the driver is re−enabled. The bulk restart level determines the minimum bulk voltage in standby mode. As long as the STBY pin voltage is below the standby threshold, the controller will operate in controlled burst mode.

The controller is not allowed to enter standby mode while the PFCOK signal is low. A dedicated timer, $t_{blank(STDBY)}$, blanks the standby signal for 1 ms (typically) right after the PFCOK signal transitions high. This ensures the signal proportional to the downstream converter output power has enough time to build up and prevent disabling the PFC while powering up the downstream converter. The standby circuit block is shown in Figure 27.

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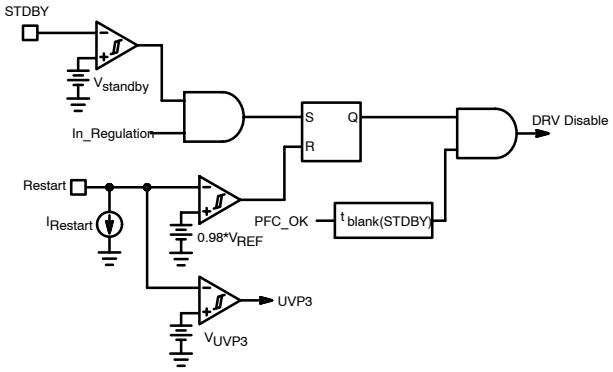


Figure 27. Standby Circuit Block

ADJUSTABLE BULK VOLTAGE HYSTERESIS

The bulk restart threshold allows the user to enable the bulk level at which the controller exits standby mode. The restart threshold is set at 2% below the internal reference, V_{REF}. The ratio between V_{REF} and the restart level is given by $K_{Restart}$. The user can set a restart level of 2% below the regulation level without using additional components as shown in Figure 28. If a different restart level is desired, a resistor network can be used as shown in Figure 29.

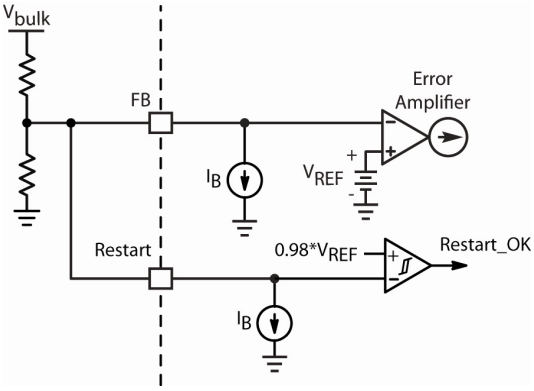


Figure 28. Minimum Restart Level Configuration

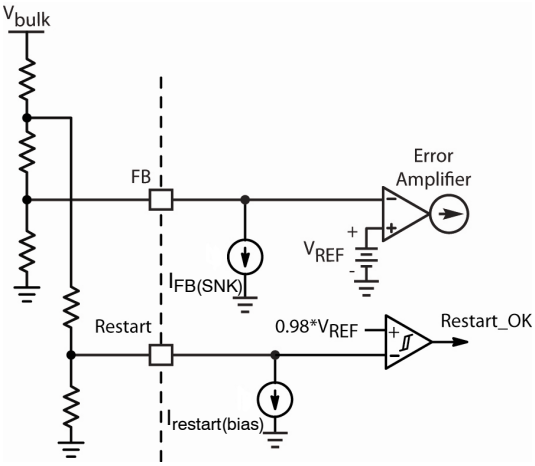


Figure 29. Restart Level Adjustment

A pull-down current source, $I_{restart(bias)}$, pulls the Restart pin down to ground if it is left open. This triggers the open pin protection and disables the controller.

LINE REMOVAL

Safety agency standards require the input filter capacitors to be discharged once the ac line voltage is removed. A resistor network is the most common method to meet this requirement. Unfortunately, the resistor network consumes power across all operating modes and it is a major contributor of input power losses during light−load and no−load conditions.

The NCP1615 eliminates the need of external discharge resistors by integrating active input filter capacitor

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discharge circuitry. A novel approach is used to reconfigure the high voltage start−up circuit to discharge the input filter capacitors upon removal of the ac line voltage. The line removal detection circuitry is always active to ensure safety compliance.

Line Removal Detection

The line removal is detected by digitally sampling the voltage present at the HV pin, and monitoring the magnitude of the slope.

A timer, $t_{line(removal)}$ (typically 100 ms), starts running when the slope magnitude of the input signal is below a minimum level. The timer is reset by the upslope detection reset timer $t_{HV(up)}$ (typically 14 ms) or the downslope detection reset timer $t_{HV(down)}$ (typically 1 ms). Once the timer expires, a line removal condition is acknowledged initiating an HV discharge cycle, and disabling the controller. This operation is depicted in Figure 30.

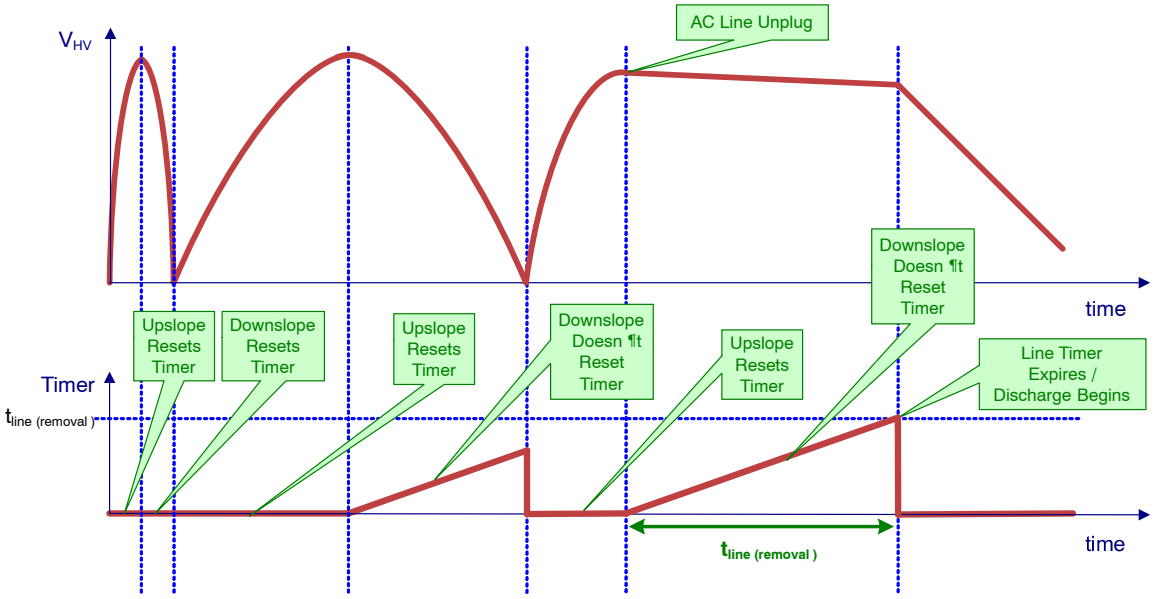


Figure 30. Line Removal Detection Timing

Capacitor Discharge

During the discharge phase, the discharge current source $I_{HV(discharge)}$ (typically 4 mA) is activated. The current source remains active and constant until V_{HV} drops to $V_{HV(discharge)}$ (typically 30 V). At this point, it begins to pinch off until the discharge phase completes. Once the discharge phase completes, a new start−up cycle commences as normal. This circuit is shown in Figure 31, while the operation is depicted in Figure 32.

It is important to note that the HV pin cannot be connected to any dc voltage due to this feature, i.e. directly to the bulk capacitor.

In the event that line voltage is reapplied during a discharge phase, the circuit will simply continue to discharge until the line zero crossing occurs, at which point V_{HV} will drop to $V_{HV(discharge)}$ and a new start−up cycle will commence.

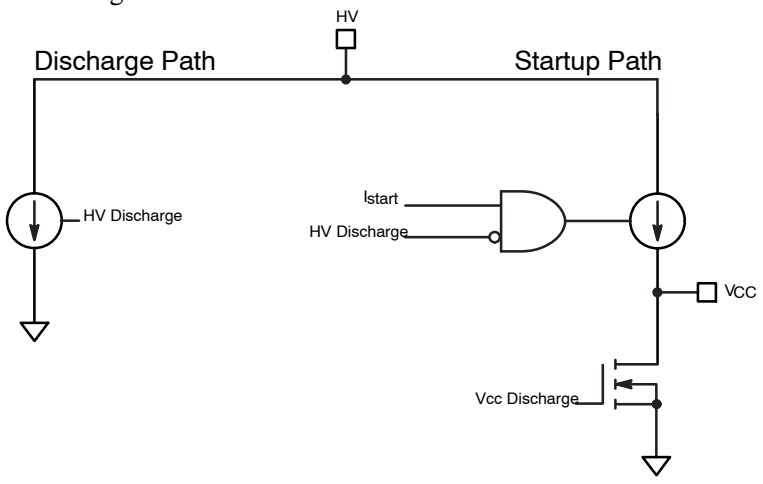


Figure 31. Discharge Block Simplified Schematic

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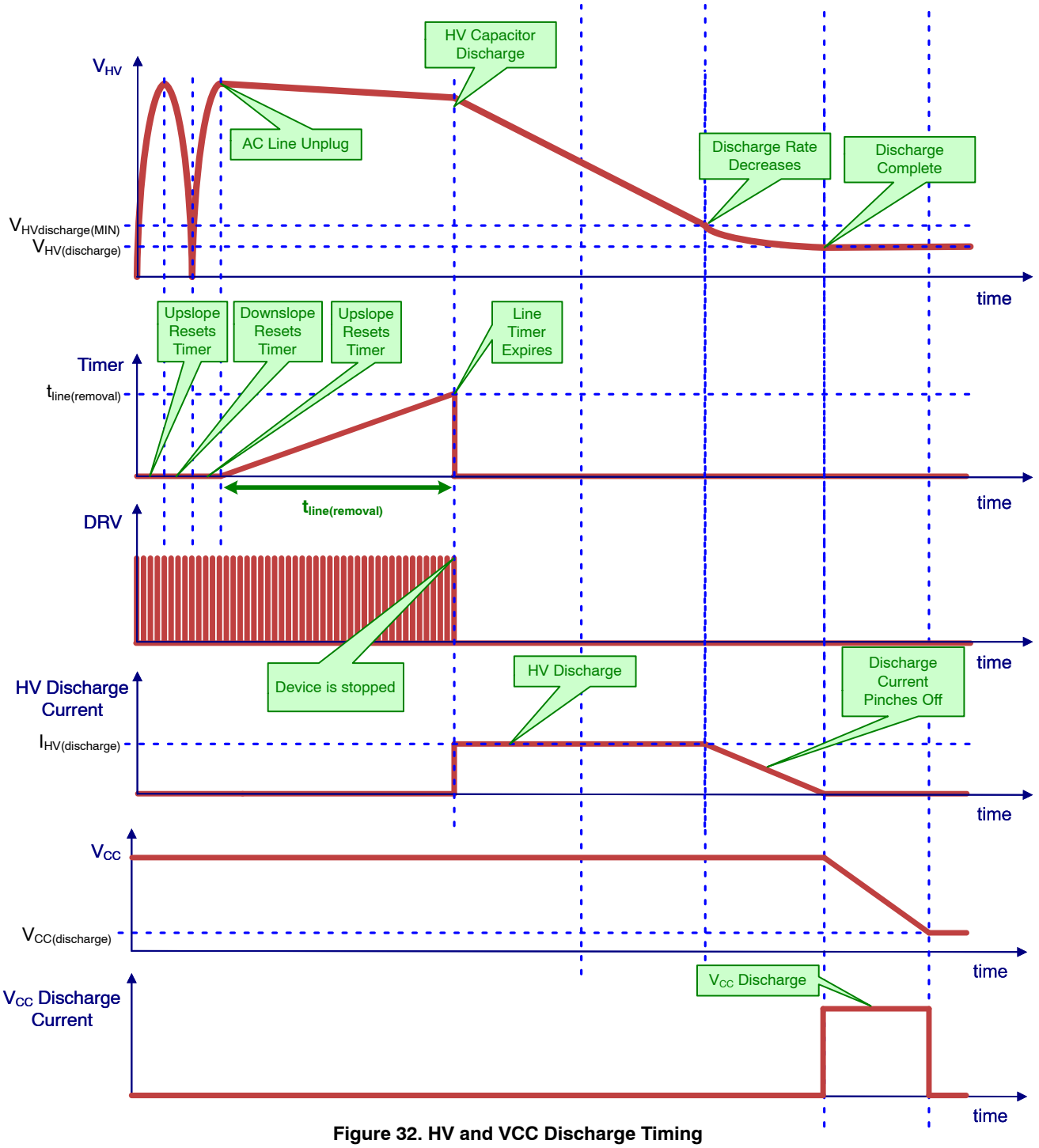


Figure 32. HV and VCC Discharge Timing

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V_{CC} DISCHARGE

If the downstream converter is latched due to a fault, it will require the supply voltage to be removed to reset the controller. Depending on the supply capacitor and current consumption, this may take a significant amount of time after the line voltage is removed. The NCP1615 uses the voltage at the HV pin to detect a line removal and discharge the V_{CC} capacitor, effectively resetting the downstream converter.

Immediately following the line removal phase, V_{CC} is discharged by a current sink, $I_{CC(discharge)}$, typically 23 mA. The current sink is disabled and the device is allowed to restart once V_{CC} to falls down to $V_{CC(discharge)}$ (5 V maximum). This operation is shown in Figure 32.

FEEDBACK DISCONNECT

The PFC output voltage is typically sensed using a resistor divider comprised of R3 and R4 as shown in Figure 33. The resistor divider consumes power when the PFC stage is disabled. The NCP1615 integrates a 700 V switch, PFC FB Switch, between the HVFB and FB pins. The PFC FB Switch connects in series between R3 and R4 to disconnect the resistors and reduce input power when the PFC stage is in PSM or latched mode.

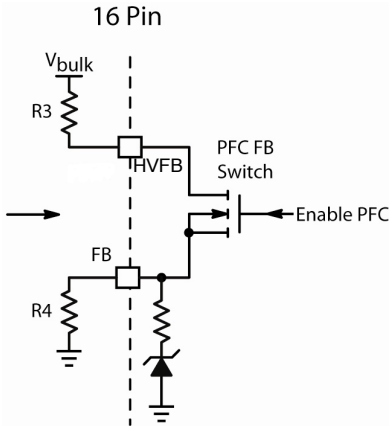


Figure 33. PFC FB Switch

The maximum on resistance of the PFC FB Switch, $R_{PFBswitch(on)}$, is 10 kΩ. Because the PFC FB Switch is in series with R3 and R3's value is several orders of magnitudes larger, the switch introduces minimal error on the regulation level. The off state leakage current of the PFC FB Switch, $I_{PFBSwitch(off)}$, is less than 3 μA.

TEMPERATURE SHUTDOWN

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN}, typically 150°C. A continuous V_{CC} hiccup is initiated after a thermal shutdown fault is detected. The controller restarts at the next $V_{CC(on)}$ once the IC temperature drops below below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 50°C.

The thermal shutdown fault is also cleared if V_{CC} drops below $V_{CC(reset)}$, or if a brownout/line removal fault is detected. A new power up sequences commences at the next $V_{CC(on)}$ once all the faults are removed.

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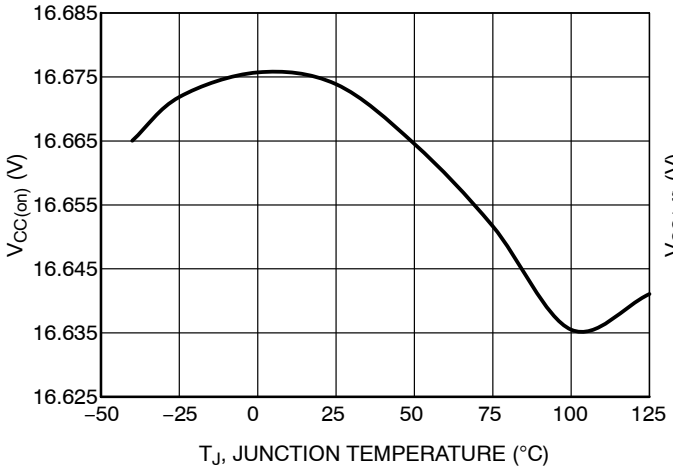


Figure 34. $V_{CC(on)}$ vs. Temperature

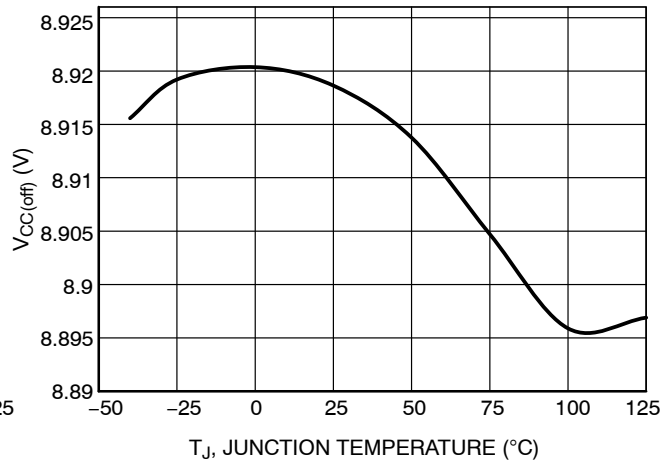


Figure 35. $V_{CC(off)}$ vs. Temperature

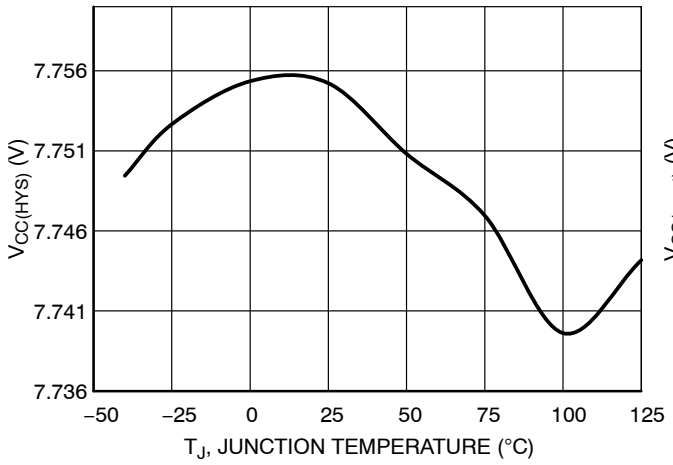


Figure 36. $V_{CC(HYS)}$ vs. Temperature

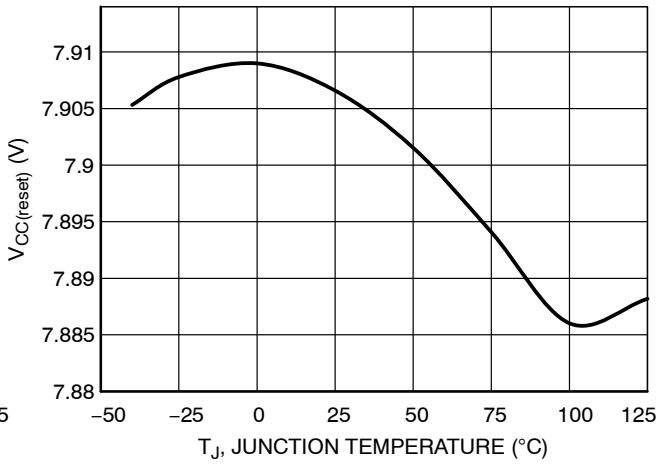


Figure 37. $V_{CC(reset)}$ vs. Temperature

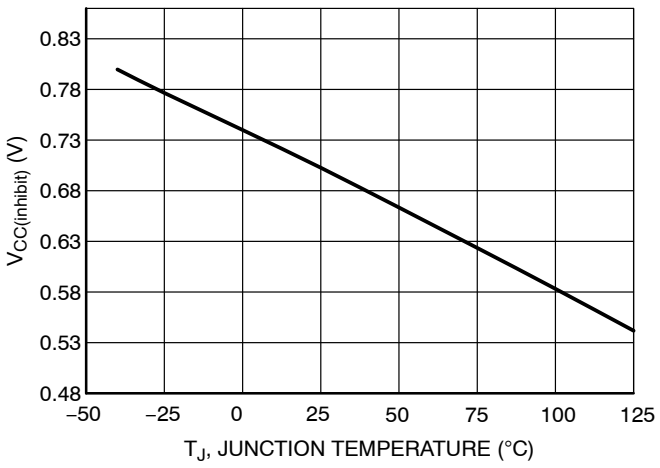


Figure 38. $V_{CC(inhibit)}$ vs. Temperature

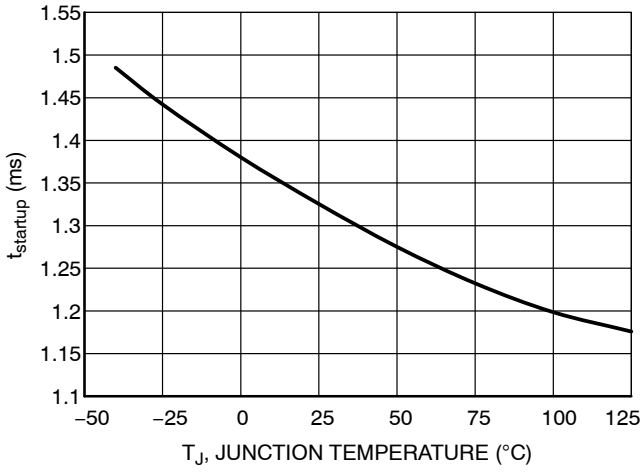


Figure 39. $t_{startup}$ vs. Temperature

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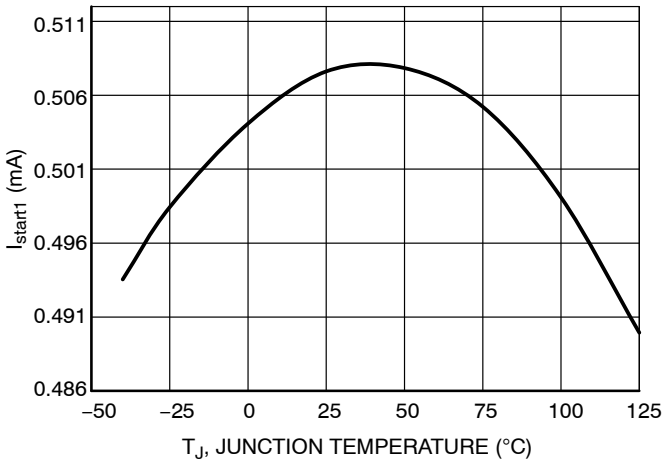


Figure 40. I_{start1} vs. Temperature

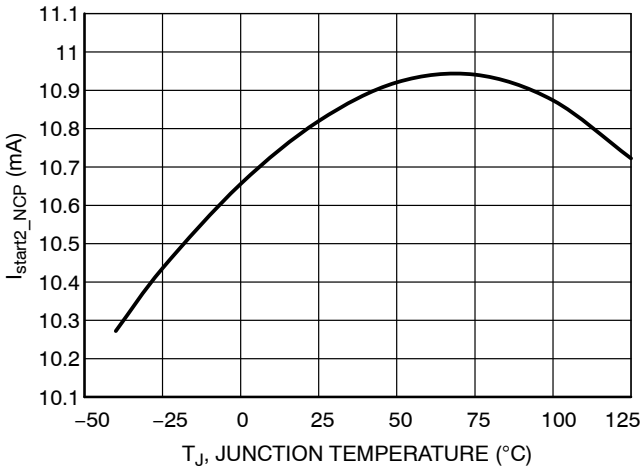


Figure 41. I_{start2} vs. Temperature

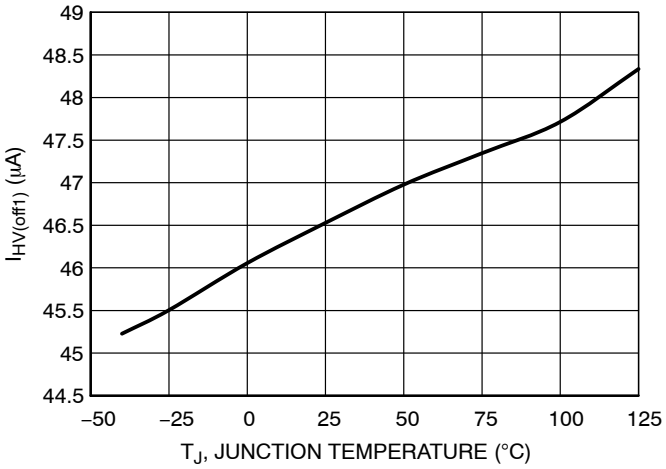


Figure 42. $I_{HV(off1)}$ vs. Temperature

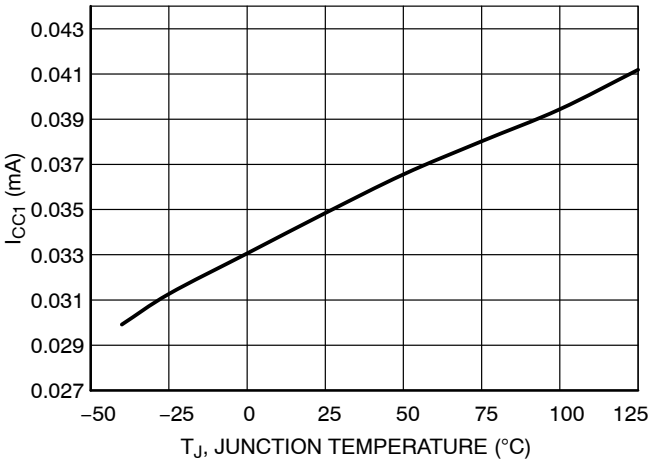


Figure 43. I_{CC1} vs. Temperature

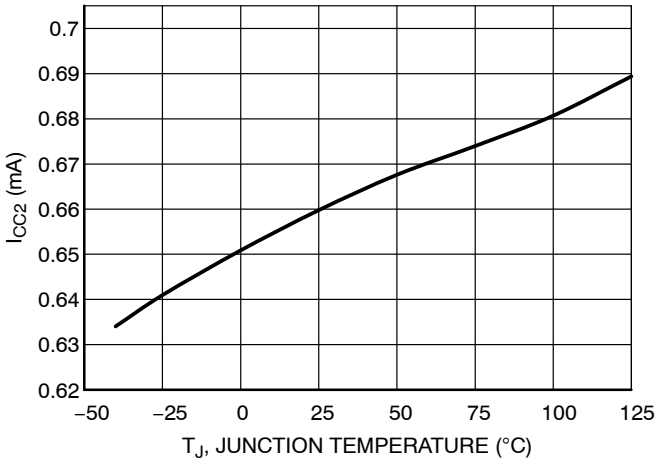


Figure 44. I_{CC2} vs. Temperature

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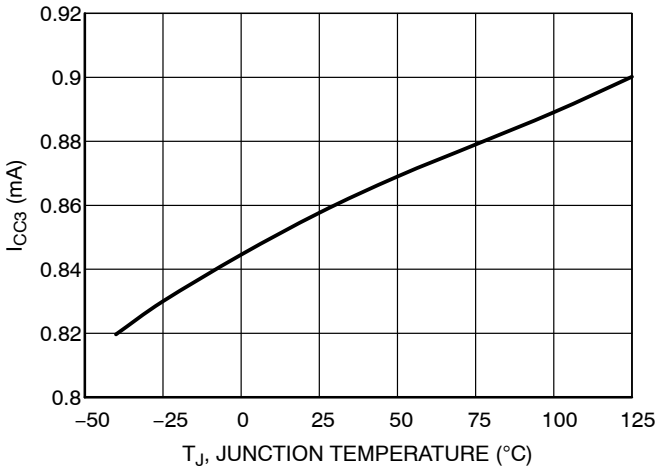


Figure 45. I_{CC3} vs. Temperature

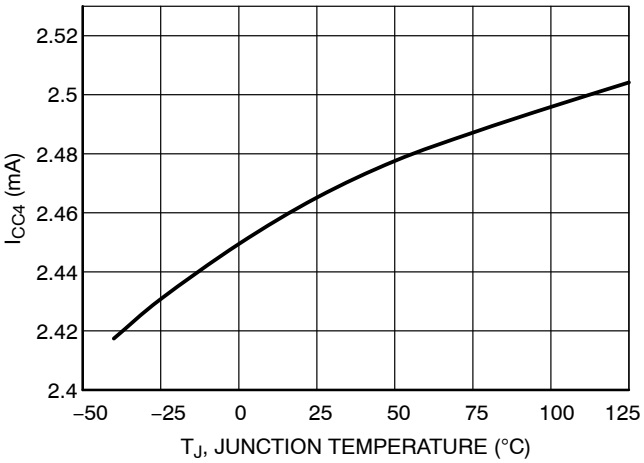


Figure 46. I_{CC4} vs. Temperature

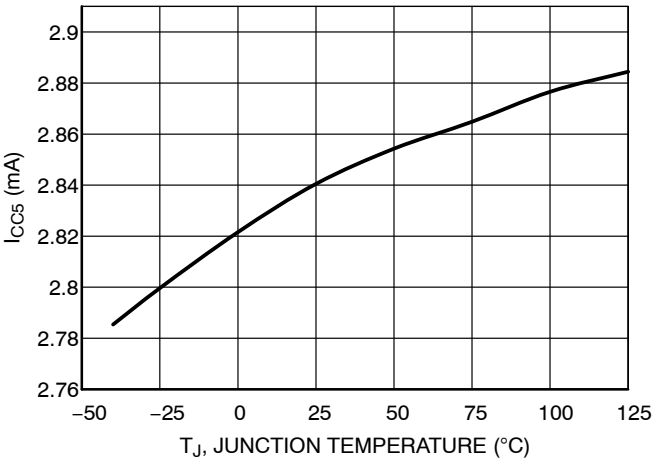


Figure 47. I_{CC5} vs. Temperature

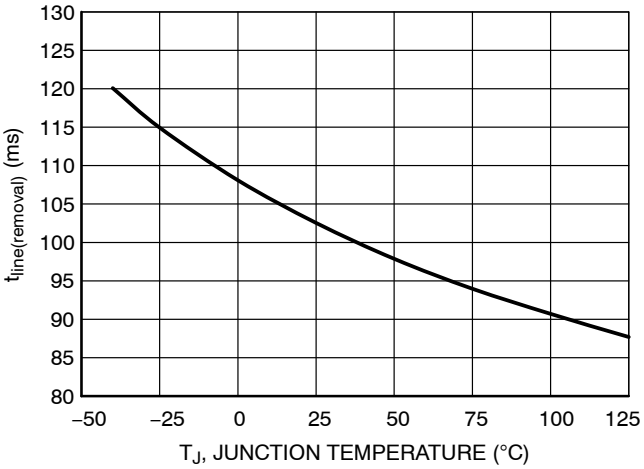


Figure 48. $t_{line(removal)}$ vs. Temperature

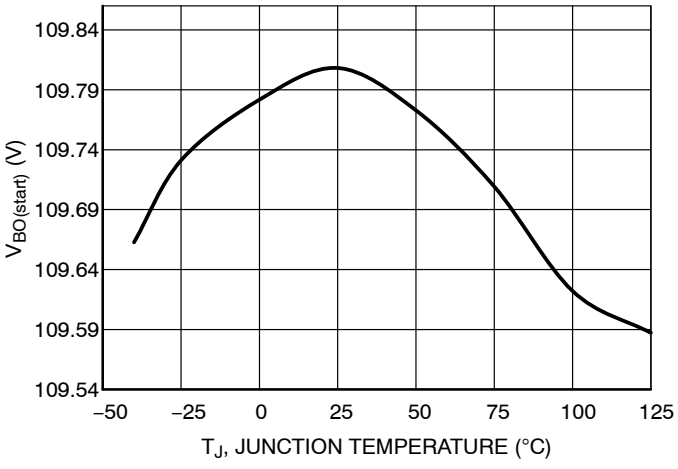


Figure 49. $V_{BO(start)}$ vs. Temperature

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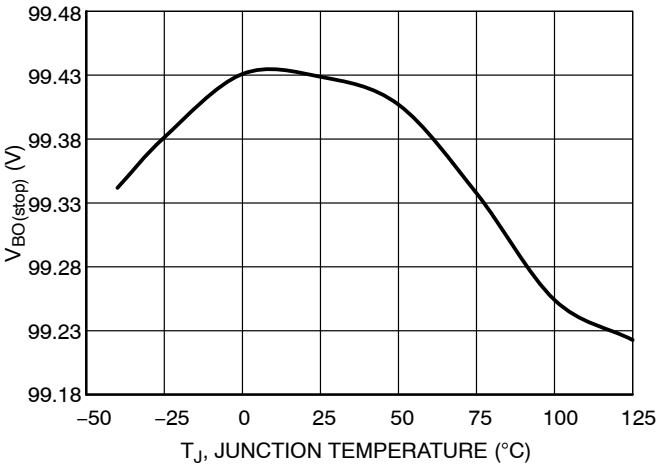


Figure 50. $V_{BO(stop)}$ vs. Temperature

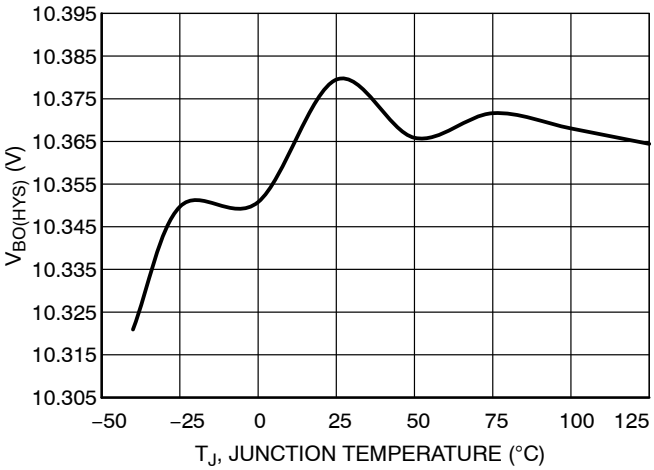


Figure 51. $V_{BO(HYS)}$ vs. Temperature

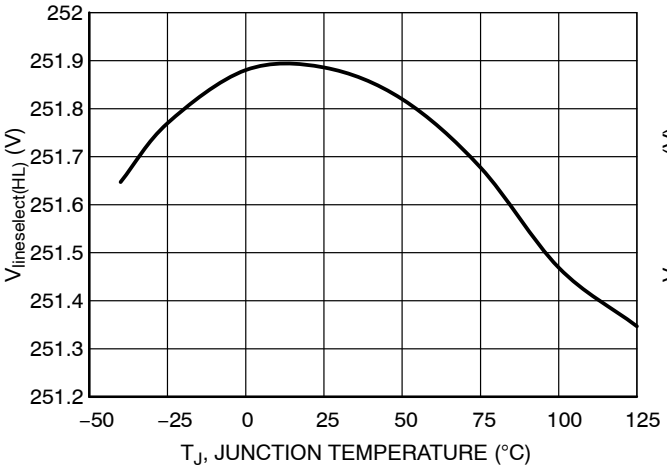


Figure 52. $V_{lineselect(HL)}$ (Version C4) vs. Temperature

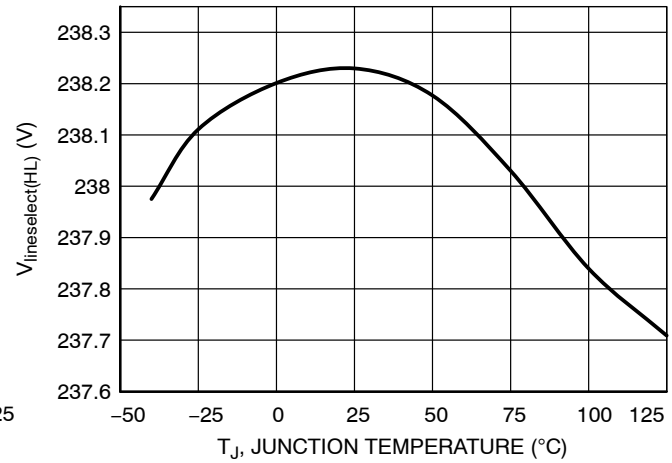


Figure 53. $V_{lineselect(HL)}$ (Version C5) vs. Temperature

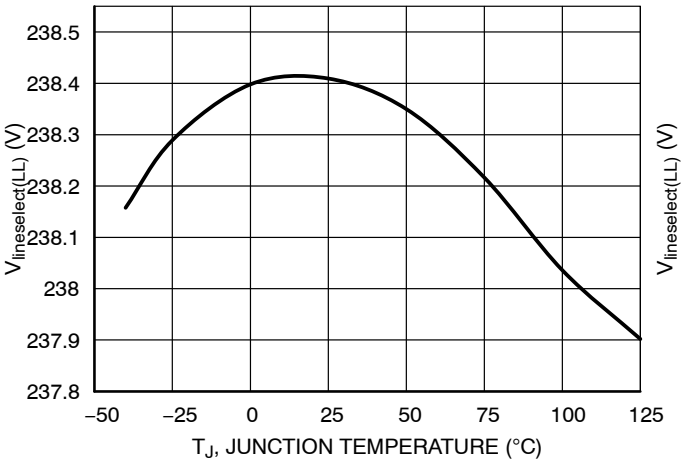


Figure 54. $V_{lineselect(LL)}$ (Version C4) vs. Temperature

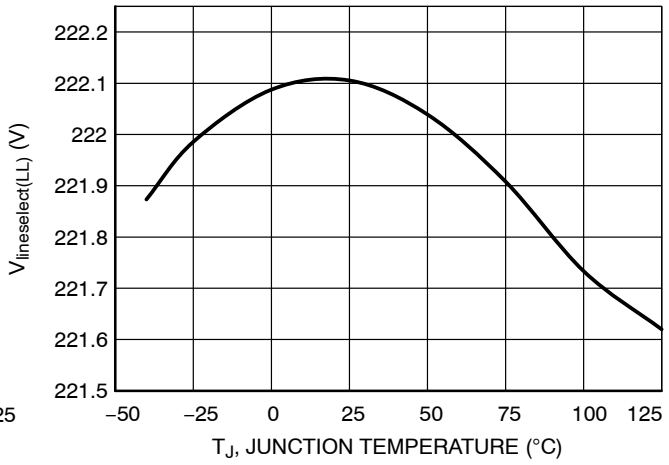


Figure 55. $V_{lineselect(LL)}$ (Version C5) vs. Temperature

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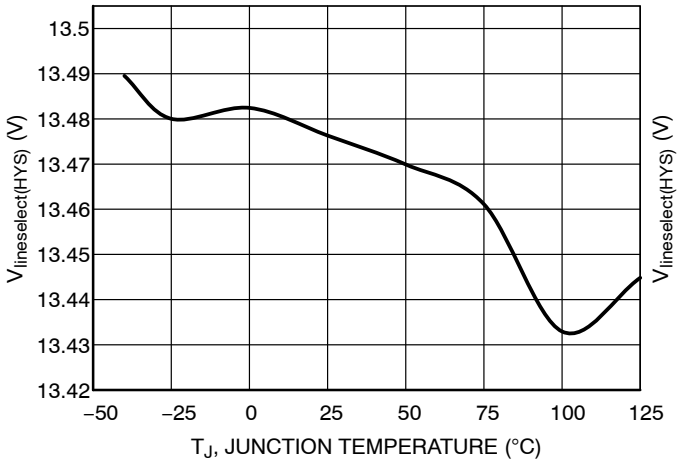


Figure 56. $V_{lineselect(HYS)}$ (Version C4) vs. Temperature

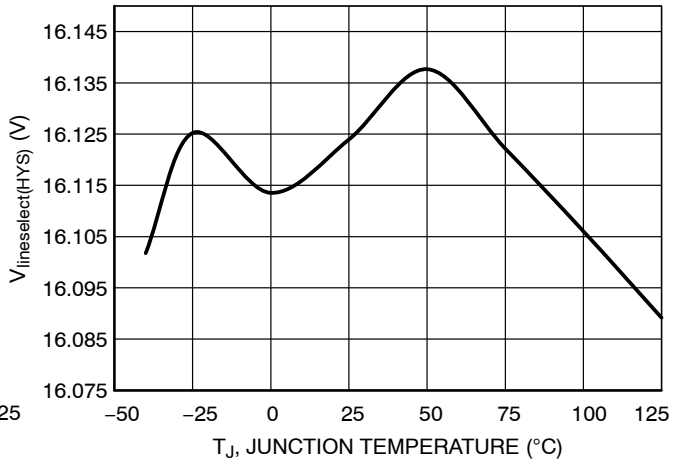


Figure 57. $V_{lineselect(HYS)}$ (Version C5) vs. Temperature

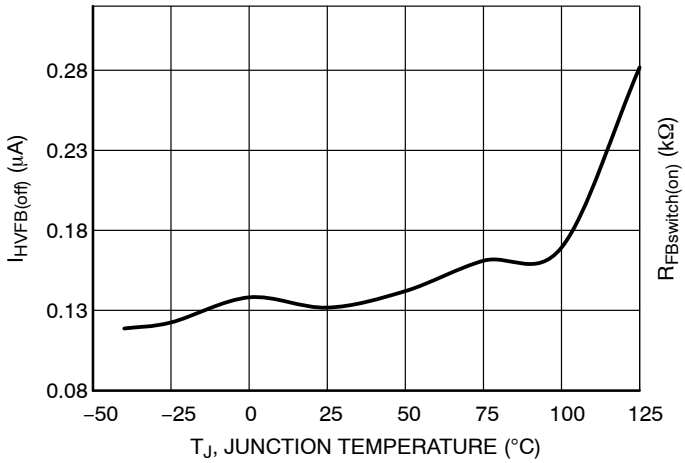


Figure 58. $I_{HVFB(off)}$ vs. Temperature

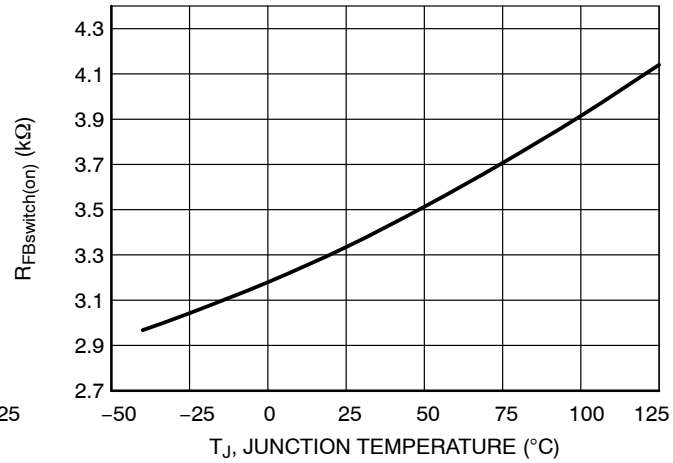


Figure 59. $R_{FBswitch(on)}$ vs. Temperature

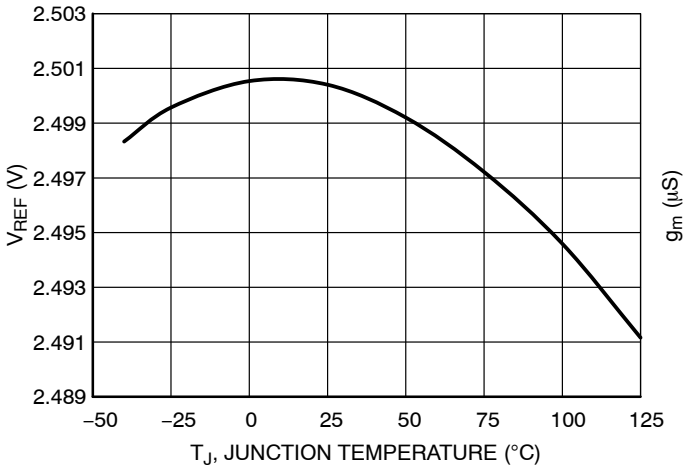


Figure 60. V_{REF} vs. Temperature

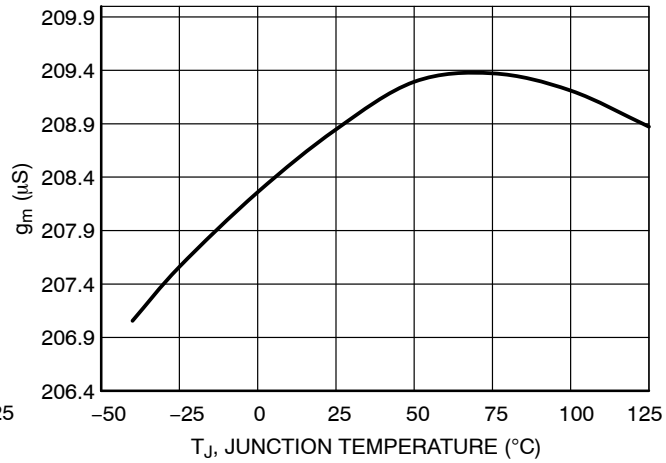


Figure 61. g_m vs. Temperature

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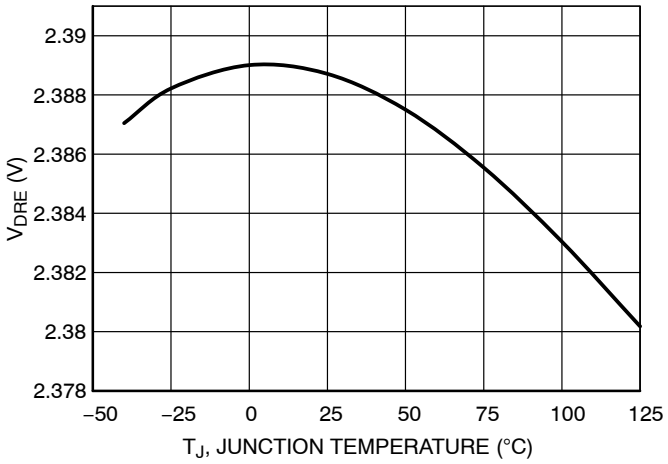


Figure 62. V_{DRE} vs. Temperature

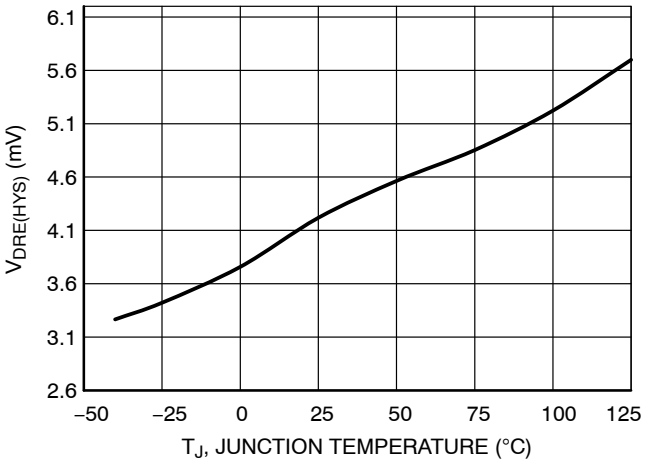


Figure 63. $V_{DRE(HYS)}$ vs. Temperature

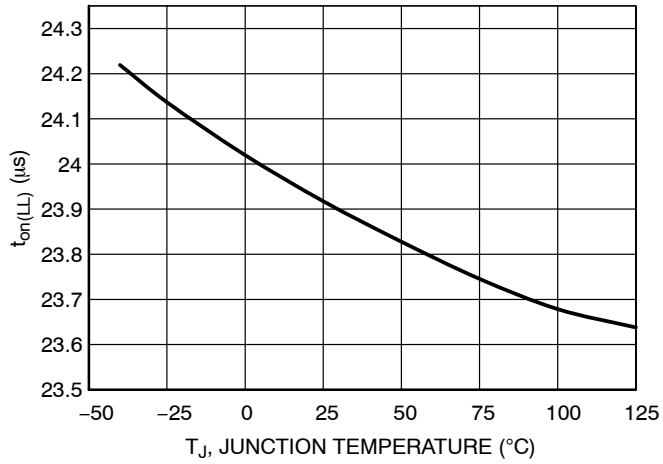


Figure 64. $t_{on(LL)}$ vs. Temperature

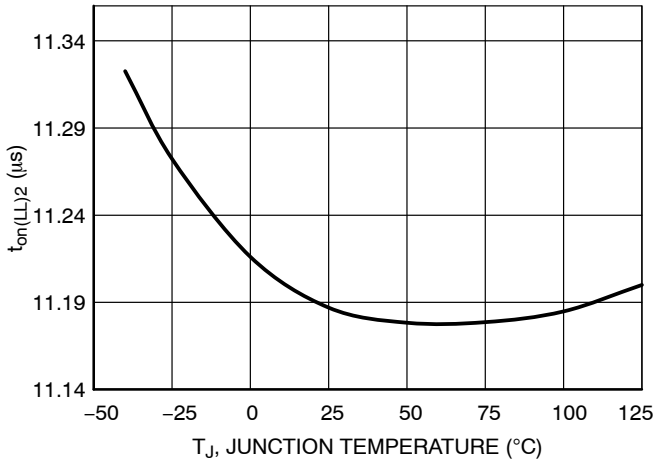


Figure 65. $t_{on(LL)2}$ vs. Temperature

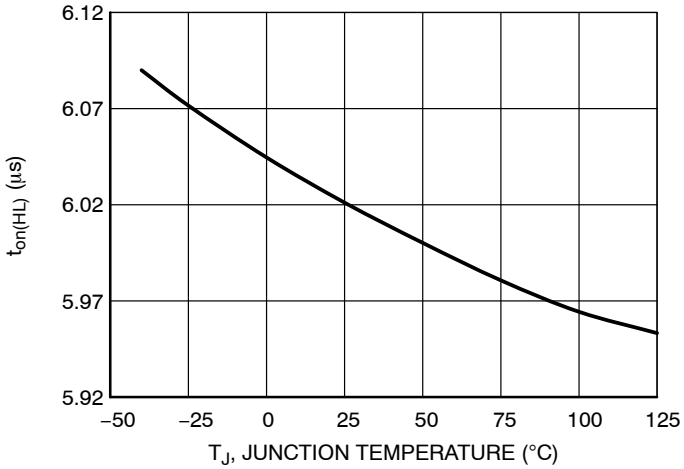


Figure 66. $t_{on(HL)}$ vs. Temperature

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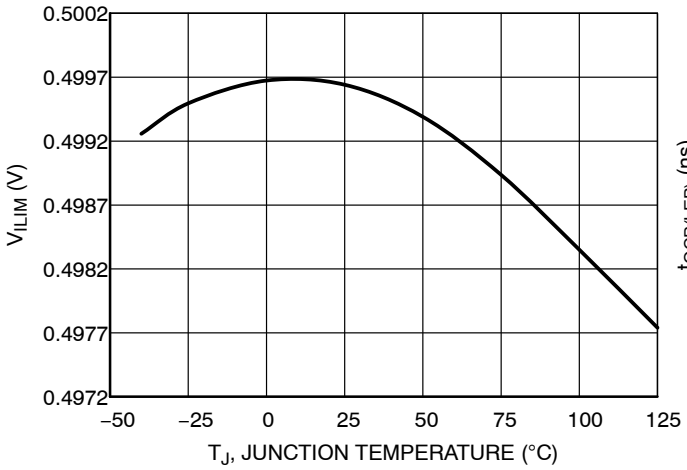


Figure 67. V_{ILIM} vs. Temperature

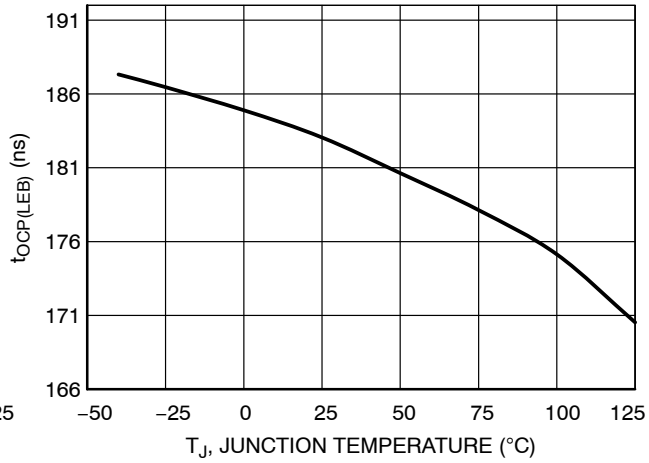


Figure 68. $t_{OCP(LEB)}$ vs. Temperature

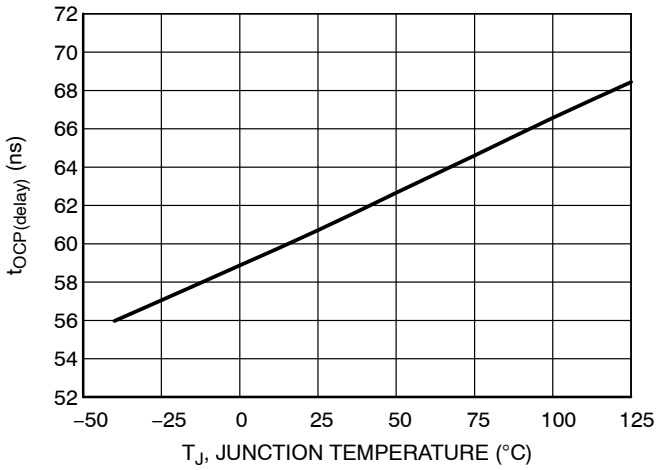


Figure 69. $t_{OCP(delay)}$ vs. Temperature

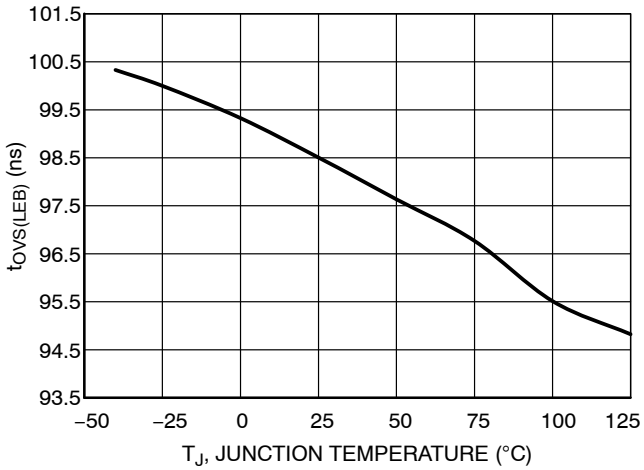


Figure 70. $t_{OVS(LEB)}$ vs. Temperature

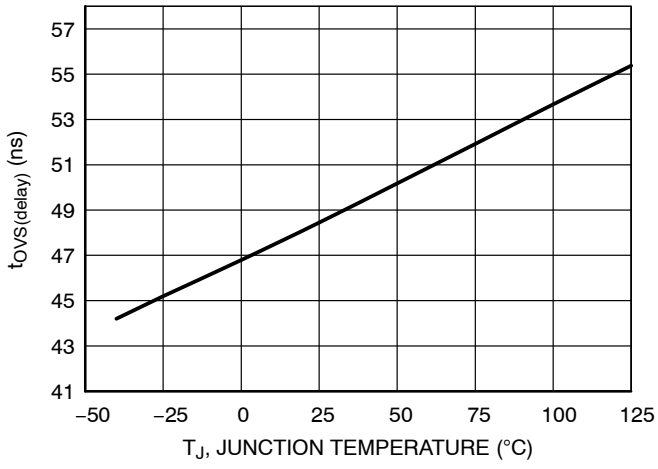


Figure 71. $t_{OVS(delay)}$ vs. Temperature

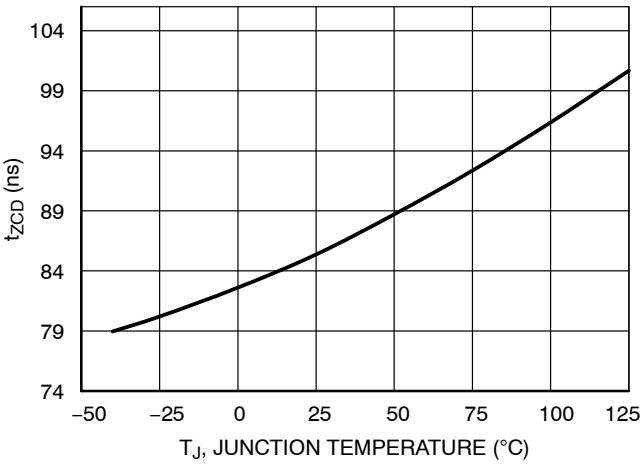


Figure 72. t_{ZCD} vs. Temperature

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TYPICAL CHARACTERISTICS

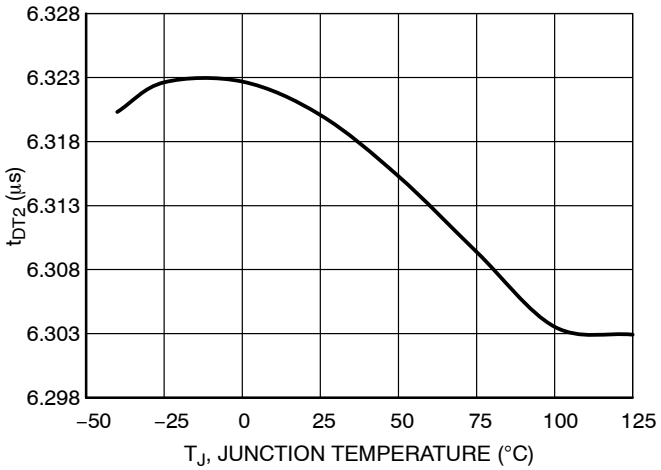


Figure 73. t_{DT2} vs. Temperature

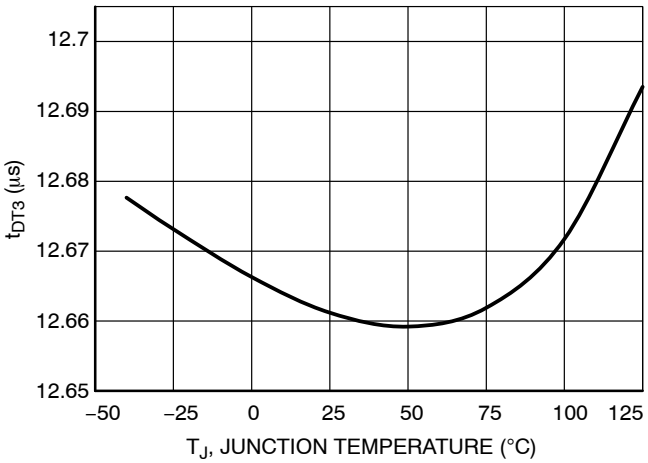


Figure 74. t_{DT3} vs. Temperature

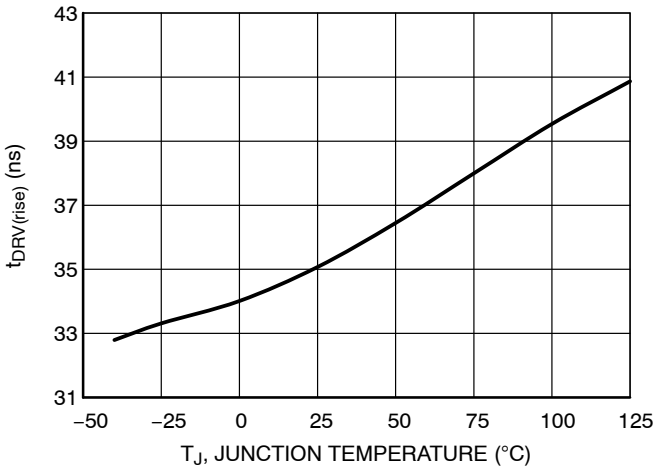


Figure 75. $t_{DRV(rise)}$ vs. Temperature

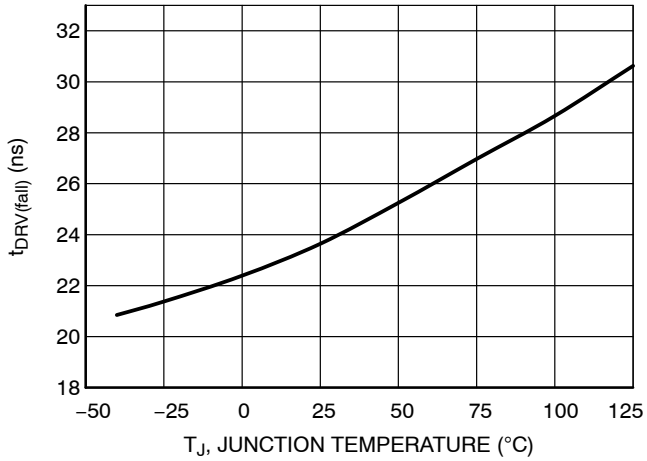


Figure 76. $t_{DRV(fall)}$ vs. Temperature

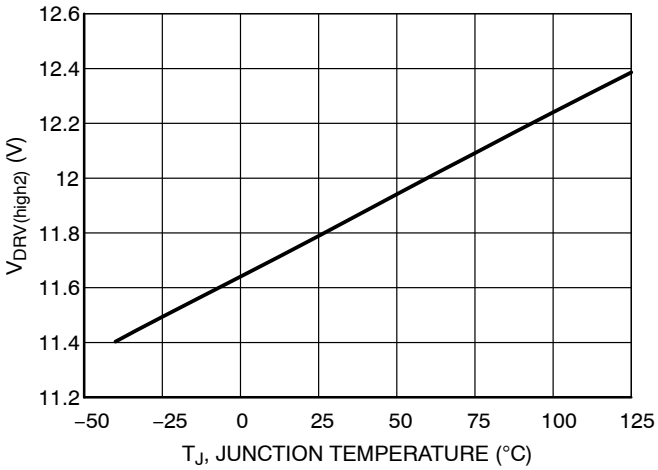


Figure 77. $V_{DRV(high2)}$ vs. Temperature

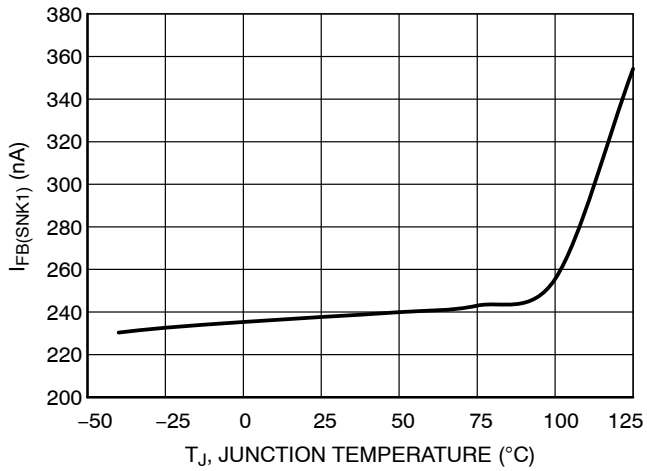


Figure 78. $I_{FB(SNK1)}$ vs. Temperature

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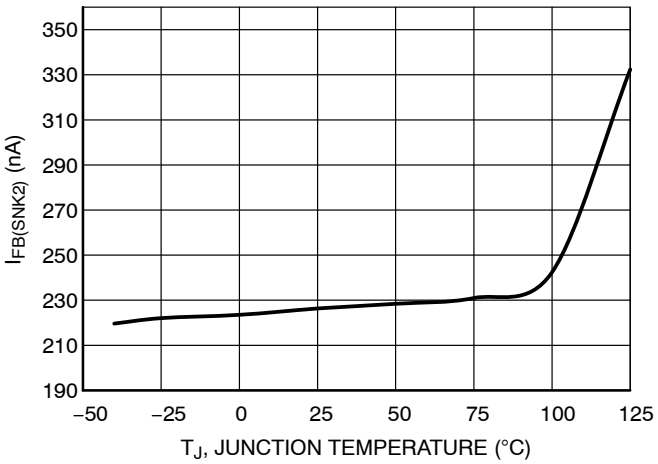


Figure 79. $I_{FB(SNK2)}$ vs. Temperature

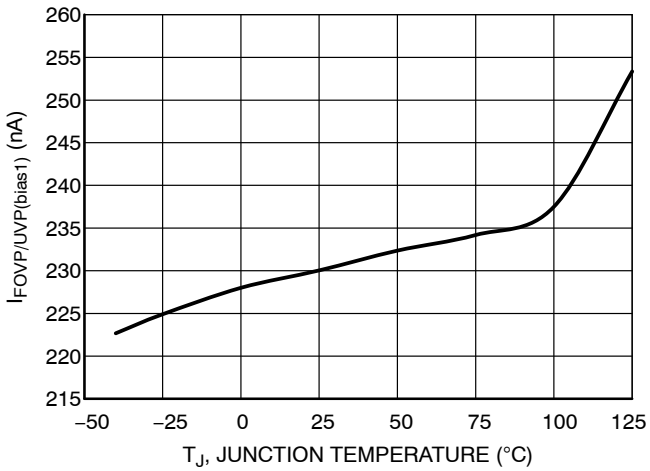
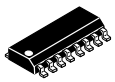


Figure 80. $I_{FOVP/UVP(bias1)}$ vs. Temperature

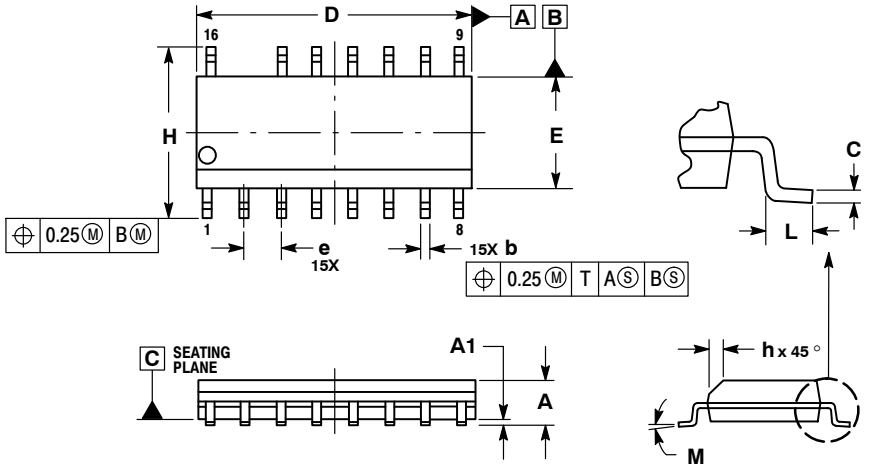
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SCALE 1:1

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CASE 752AC
ISSUE O

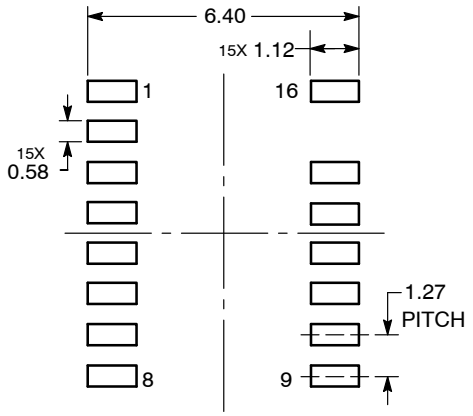
DATE 28 JAN 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

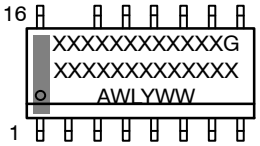
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
M	0 °	7 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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