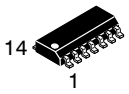
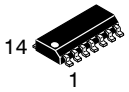
Quad 2-Input AND Gate

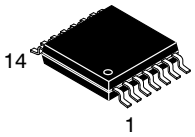
MM74HCT08



SOIC−14 NB
CASE 751A−03



SOIC14
CASE 751EF



TSSOP−14 WB
CASE 948G−01

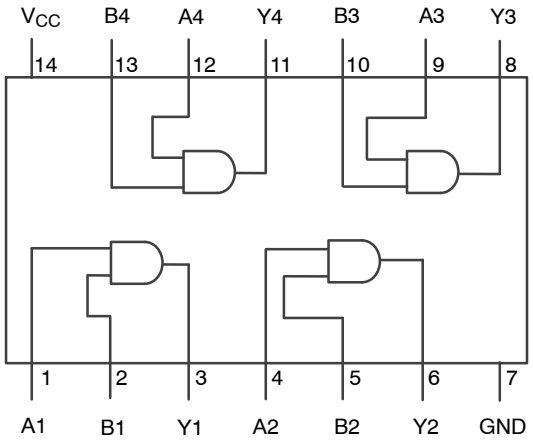
General Description

The MM74HCT08 is a logic function fabricated by using advanced silicon−gate CMOS technology which provides the inherent benefits of CMOS — low quiescent power and wide power supply range. This device is input and output characteristic and pinout compatible with standard 74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug−in replacements for LS−TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS Pin−out and Threshold Compatible
- Fast Switching: t_{PLH}, t_{PHL} = 9 ns (Typ.)
- Low Power: 10 μW at DC
- High Fan−out, 10 LS−TTL Loads
- This Device is Pb−Free and Halide Free



Pin Assignments for SOIC and TSSOP

Figure 1. Connection Diagram

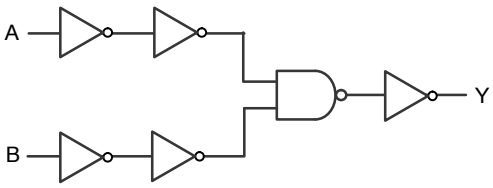
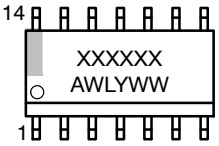


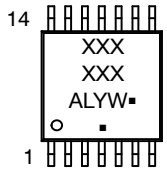
Figure 2. Logic Diagram

MARKING DIAGRAMS

SOIC−14



TSSOP−14



XXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot Number
Y = Year
WW, YW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Rating	Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	+6.5	V
V_{IN}	DC Input Voltage	−0.5	V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage	−0.5	V_{CC} + 0.5	V
I_{IK}, I_{OK}	Clamp Diode Current		±20	mA
I_{OUT}	DC Output Current, per pin		±25	mA
I_{CC}	DC V_{CC} or GND Current, per pin		±50	mA
T_{STG}	Storage Temperature Range	−65	+150	°C
P_D	Power Dissipation SOIC TSSOP		1077 833	mW
T_L	Lead Temperature (Soldering 10 second)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−55	+125	°C
t_r, t_f	Input Rise or Fall Times	–	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5 V	4.2	3.98	3.84	3.7	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5 V	5.2	4.98	4.84	4.7	
V_{OL}	Maximum LOW Level Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5 V	0.2	0.26	0.33	0.4	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5 V	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4 V or 0.5 V (Note 2)		1.2	1.4	1.5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. This is measured per input with all other inputs held at V_{CC} or ground.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, t_r = t_f = 6 ns, C_L = 15 pF, T_A = 25°C)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay		9	15	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%, t_r = t_f = 6 ns, C_L = 50 pF)

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Unit
			Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay		11	18	23	27	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		7	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 3)	38				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} $V_{CC}^2 f$ + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

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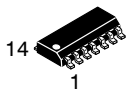
ORDERING INFORMATION

Device	Marking	Package	Shipping†
MM74HCT08M	HCT08A	SOIC−14, Case 751A	55 Units / Tube
MM74HCT08MX	HCT08A	SOIC 14, Case 751EF	2500 Units / Tape & Reel
MM74HCT08MTC	HCT 08A	TSSOP−14, Case 948G	96 Units / Tube
MM74HCT08MTCX	HCT 08A	TSSOP−14, Case 948G	2500 Units / Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: All packages are lead free per JEDEC: J−STD−020B standard.

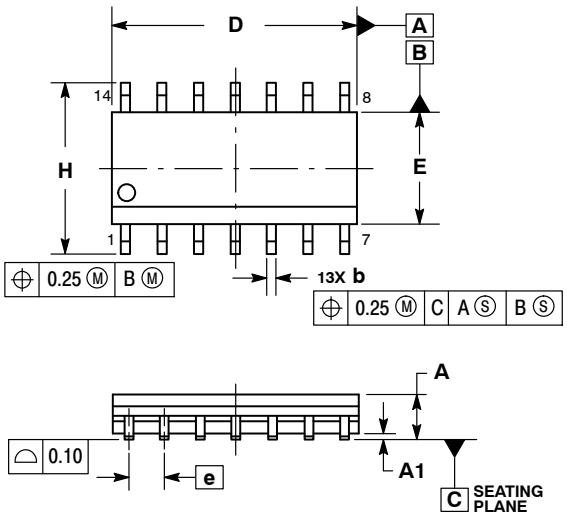
Share Feedback
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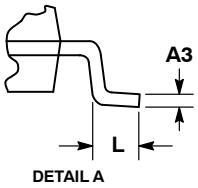


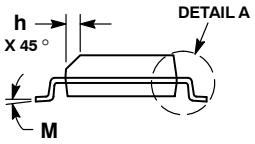
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



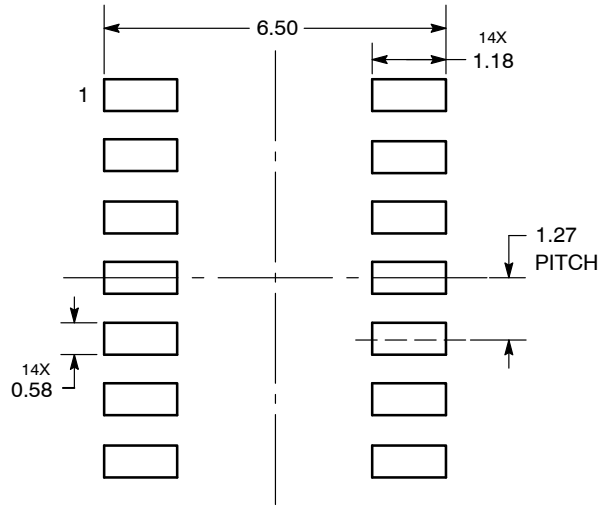




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

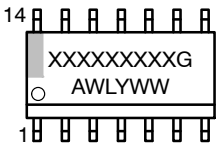
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

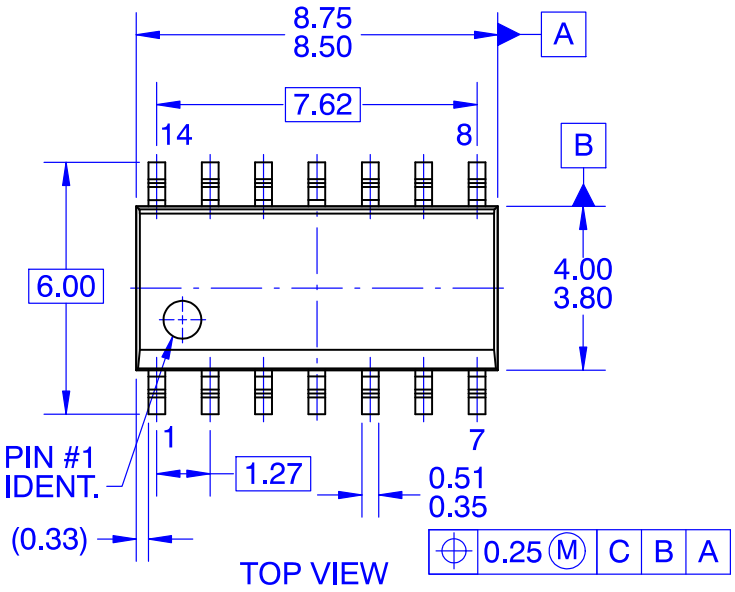
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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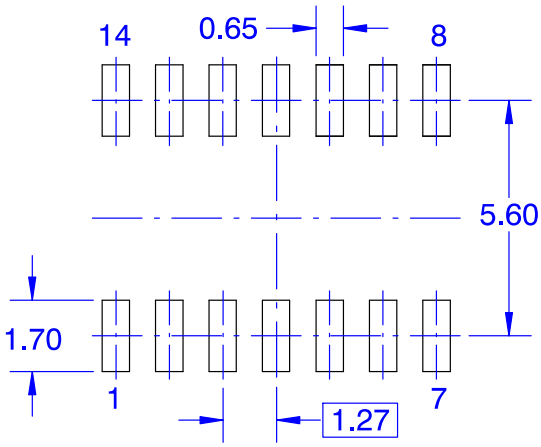
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SOIC14
CASE 751EF
ISSUE O

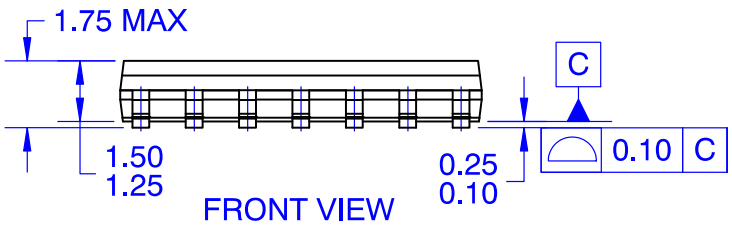
DATE 30 SEP 2016



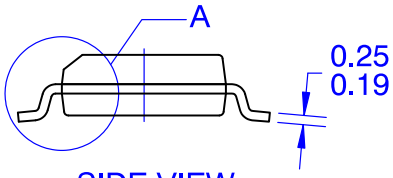
TOP VIEW



LAND PATTERN RECOMMENDATION

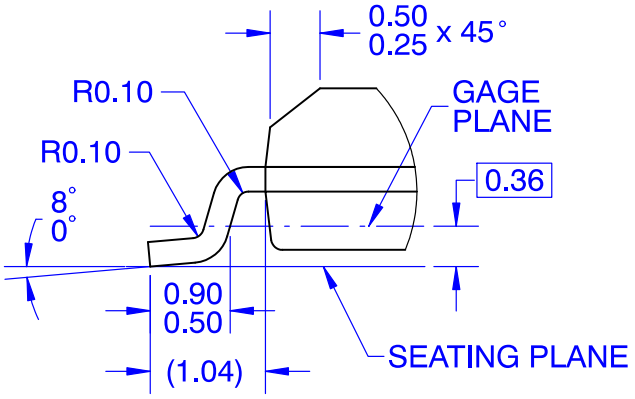


FRONT VIEW



SIDE VIEW

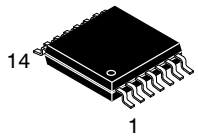
NOTES:
A. CONFORMS TO JEDEC MS−012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145−14M
E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

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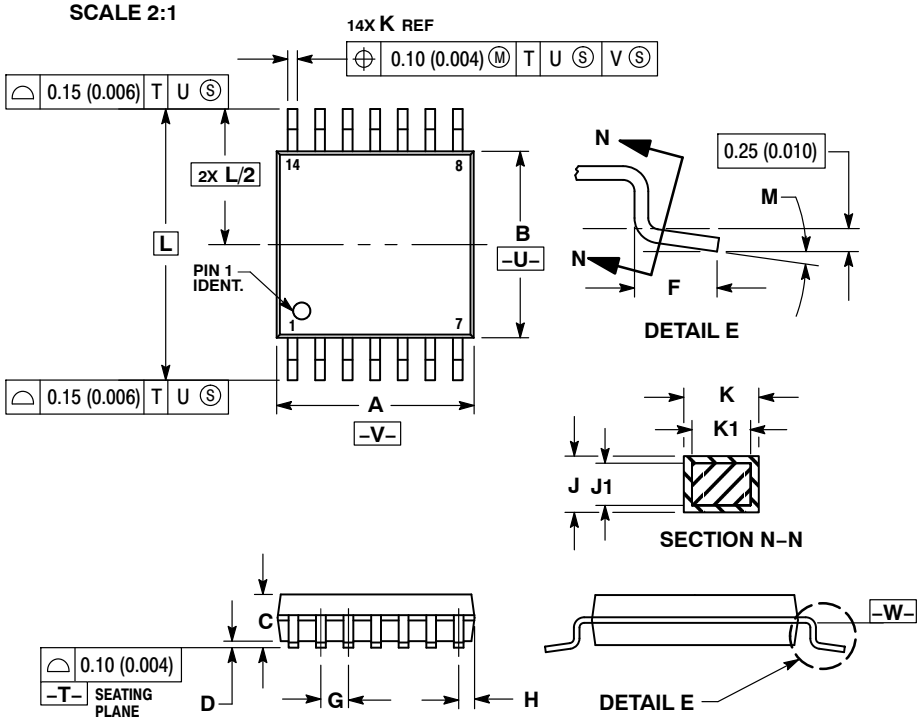
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SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

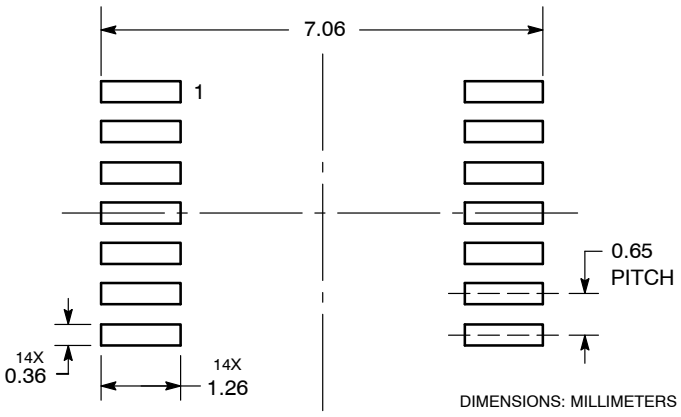
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

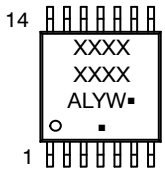
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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