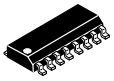
8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter

With LSTTL-Compatible Inputs

MC74LVX259



SOIC−16
D SUFFIX
CASE 751B



TSSOP−16
DT SUFFIX
CASE 948F

The MC74LVX259 is an 8−bit Addressable Latch fabricated with silicon gate CMOS technology.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

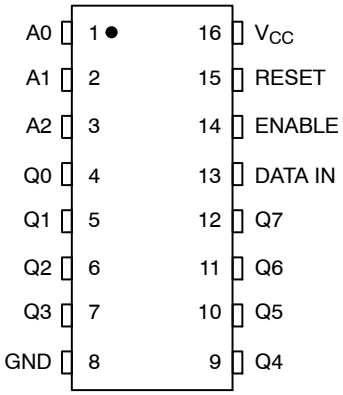
The LVX259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non−addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one−of−eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the LVX259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The MC74LVX259 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74LVX259 to be used to interface 5.0 V circuits to 3.0 V circuits.

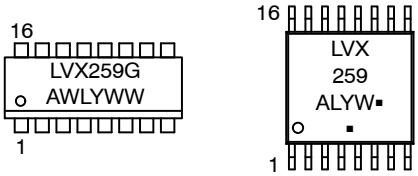
Features

- High Speed: t_{PD} = 7.0 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- CMOS−Compatible Outputs: V_{OH} > 0.8 V_{CC}; V_{OL} < 0.1 V_{CC} @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb−Free and are RoHS Compliant

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC−16 TSSOP−16

LVX259 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7.

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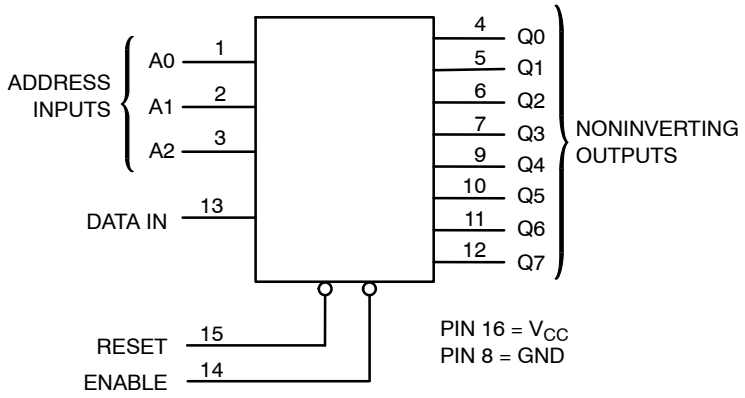


Figure 1. Logic Diagram

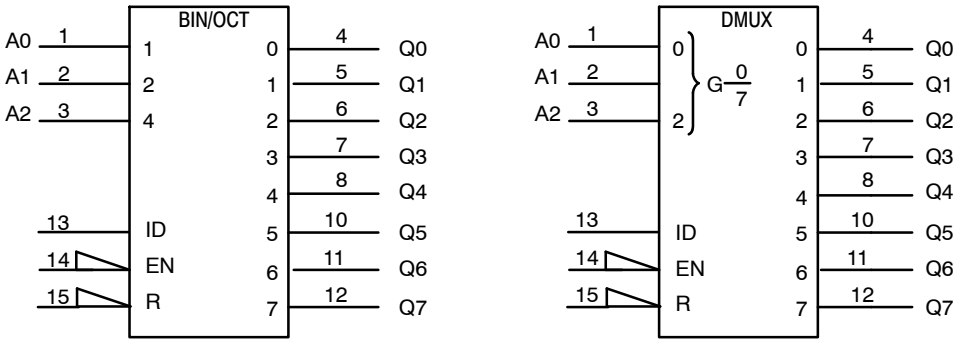


Figure 2. IEC Logic Symbol

MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8−Line Demultiplexer
H	L	Reset

LATCH SELECTION TABLE

Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

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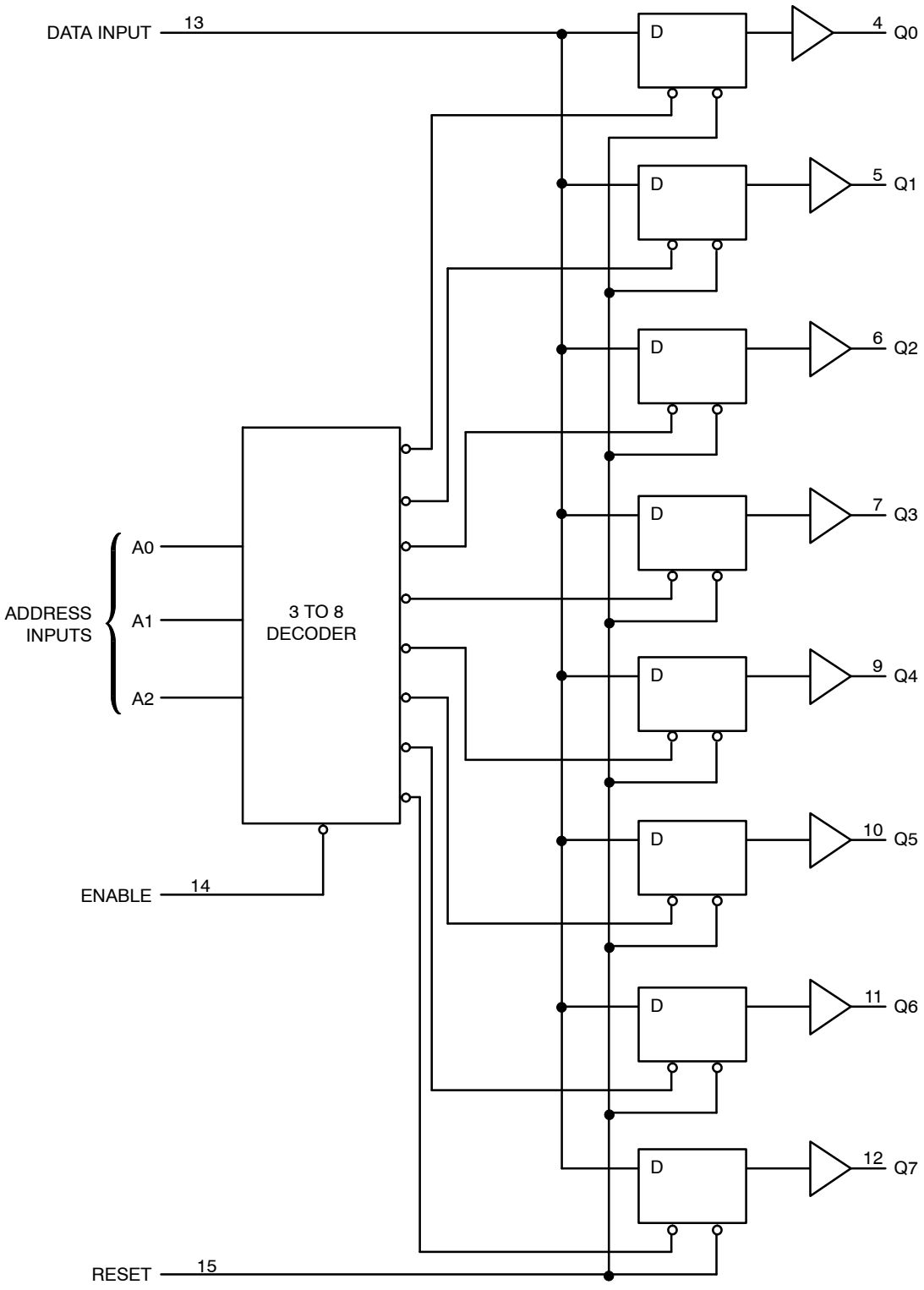


Figure 3. Expanded Logic Diagram

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 > 2000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4)	±300	mA
θ_{JA}	Thermal Resistance, Junction−to−Ambient	SOIC Package TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	3.6	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types		−40	85	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 3.3 V ± 0.3 V	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	−40°C ≤ T_A ≤ 85°C Min	−40°C ≤ T_A ≤ 85°C Max	Unit
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 3.6	0.75 V_{CC} 0.7 V_{CC} 0.7 V_{CC}	– – –	– – –	0.75 V_{CC} 0.7 V_{CC} 0.7 V_{CC}	– – –	V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 3.6	– – –	– – –	0.25 V_{CC} 0.3 V_{CC} 0.3 V_{CC}	– – –	0.25 V_{CC} 0.3 V_{CC} 0.3 V_{CC}	V
V_{OH}	High−Level Output Voltage	I_{OH} = −50 μA	2.0	1.9	2.0	–	1.9	–	V
		I_{OH} = −50 μA	3.0	2.9	3.0	–	2.9	–	
		I_{OH} = −4 mA	3.0	2.58	–	–	2.48	–	
V_{OL}	Low−Level Output Voltage	I_{OL} = 50 μA	2.0	–	0.0	0.1	–	0.1	V
		I_{OL} = 50 μA	3.0	–	0.0	0.1	–	0.1	
		I_{OL} = 4 mA	3.0	–	–	0.36	–	0.44	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 3.6	–	–	±0.1	–	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_{IN} = V_{CC} or GND	3.6	1.0	1.0	2.0	–	–	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	−40°C ≤ T_A ≤ 85°C Min	−40°C ≤ T_A ≤ 85°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Data to Output (Figures 4 and 8)	V_{CC} = 2.7 V	C_L = 15pF C_L = 50pF	– –	6.3 9.0	9.0 14.0	1.0 1.0	12.0 15.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15pF C_L = 50pF	– –	5.6 8.0	8.0 12.0	1.0 1.0	11.0 14.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Address Select to Output (Figures 5 and 8)	V_{CC} = 2.7 V	C_L = 15pF C_L = 50pF	– –	6.3 9.0	9.0 14.0	1.0 1.0	12.0 15.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15pF C_L = 50pF	– –	5.6 8.0	8.0 12.0	1.0 1.0	11.0 14.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to Output (Figures 6 and 8)	V_{CC} = 2.7 V	C_L = 15pF C_L = 50pF	– –	6.3 9.0	9.0 14.0	1.0 1.0	12.0 15.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15pF C_L = 50pF	– –	5.6 8.0	9.0 12.0	1.0 1.0	11.0 14.0	
t_{PHL}	Maximum Propogation Delay, Reset to Output (Figures 6 and 8)	V_{CC} = 2.7 V	C_L = 15pF C_L = 50pF	– –	6.3 9.0	9.0 14.0	1.0 1.0	12.0 15.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15pF C_L = 50pF	– –	5.6 8.0	9.0 12.0	1.0 1.0	11.0 14.0	
C_{IN}	Maximum Input Capacitance			–	6	10	–	10	pF
				Typical @ 25°C, V_{CC} = 3.3 V					
C_{PD}	Power Dissipation Capacitance (Note 5)			30					pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

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TIMING REQUIREMENTS Input $t_r = t_f = 3.0$ ns

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$T_A = \leq 85°C$		Unit
			Min	Typ	Max	Min	Max	
t_w	Minimum Pulse Width, Reset or Enable (Figure 7)	V_{CC} = 2.7 V	4.5	–	–	5.0	–	ns
		V_{CC} = 3.3 V ± 0.3 V	4.5	–	–	5.0	–	
t_{su}	Minimum Setup Time, Address or Data to Enable (Figure 7)	V_{CC} = 2.7 V	4.0	–	–	4.0	–	ns
		V_{CC} = 3.3 V ± 0.3 V	3.0	–	–	3.0	–	
t_h	Minimum Hold Time, Enable to Address or Data (Figure 6 or 7)	V_{CC} = 2.7 V	2.0	–	–	2.0	–	ns
		V_{CC} = 3.3 V ± 0.3 V	2.0	–	–	2.0	–	
t_r, t_f	Maximum Input, Rise and Fall Times (Figure 4)	V_{CC} = 2.7 V	–	–	400	–	300	ns
		V_{CC} = 3.3 V ± 0.3 V	–	–	300	–	300	

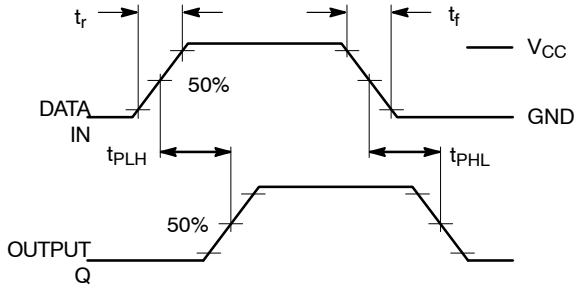


Figure 4. Switching Waveform

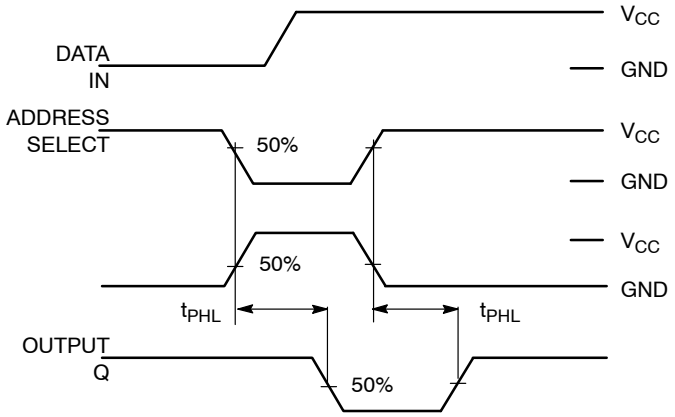


Figure 5. Switching Waveform

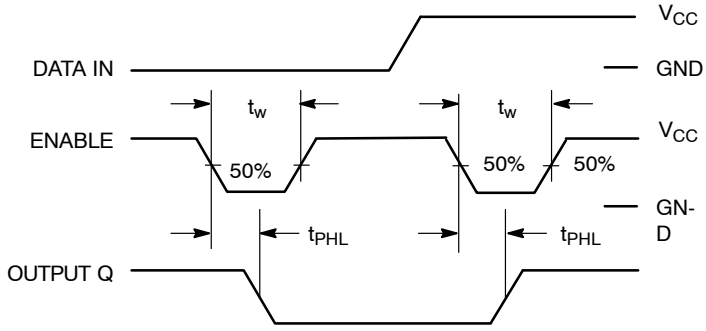


Figure 6. Switching Waveform

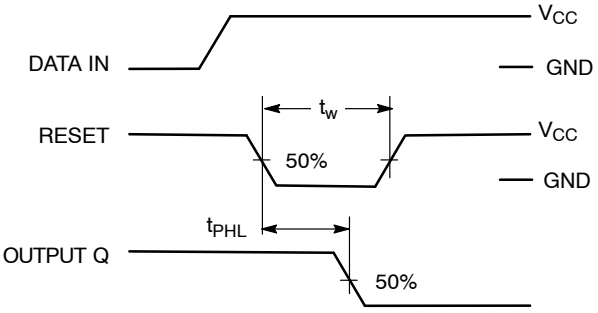


Figure 7. Switching Waveform

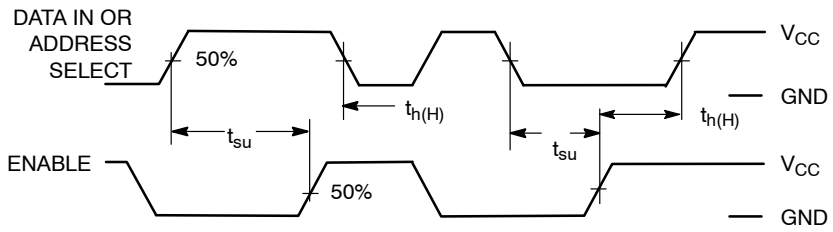
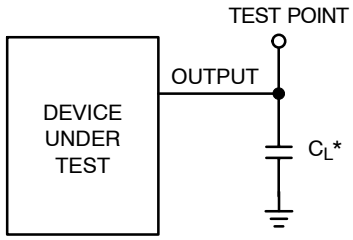


Figure 8. Switching Waveform



*Includes all probe and jig capacitance

Figure 9. Test Circuit

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EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 −0.0 (0.059" +0.004 −0.0)	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

6. Metric Dimensions Govern−English are in parentheses for reference only.
7. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX259DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74LVX259DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

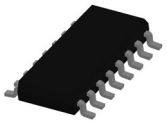
DISCONTINUED (Note 8)

MC74LVX259DG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74LVX259DTG	TSSOP−16 (Pb−Free)	96 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

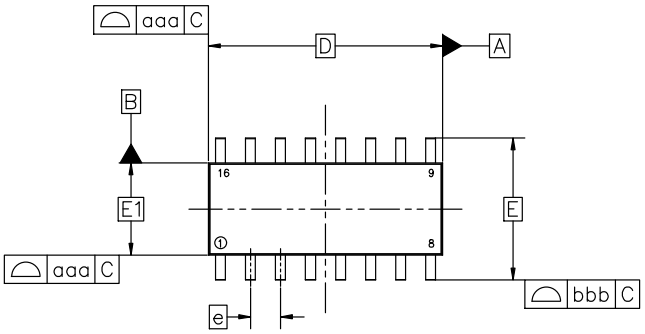
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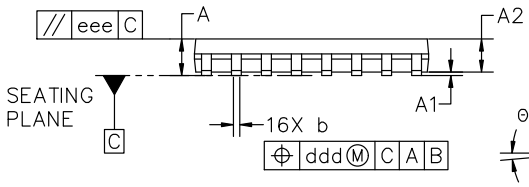
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

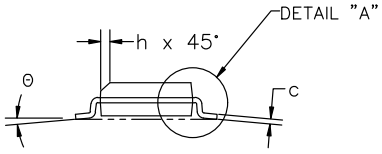
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



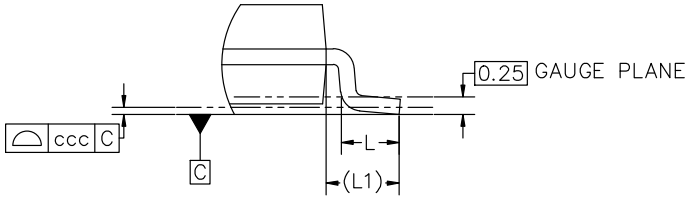
TOP VIEW



SIDE VIEW

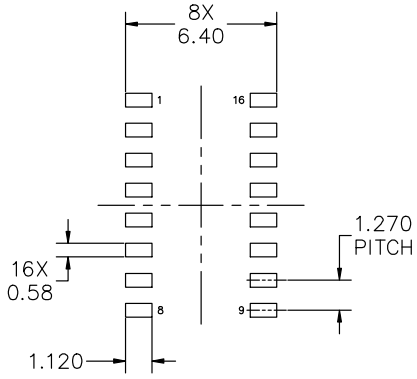


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

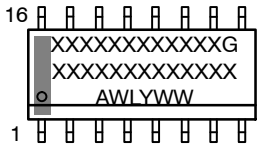
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SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

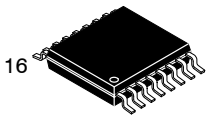
PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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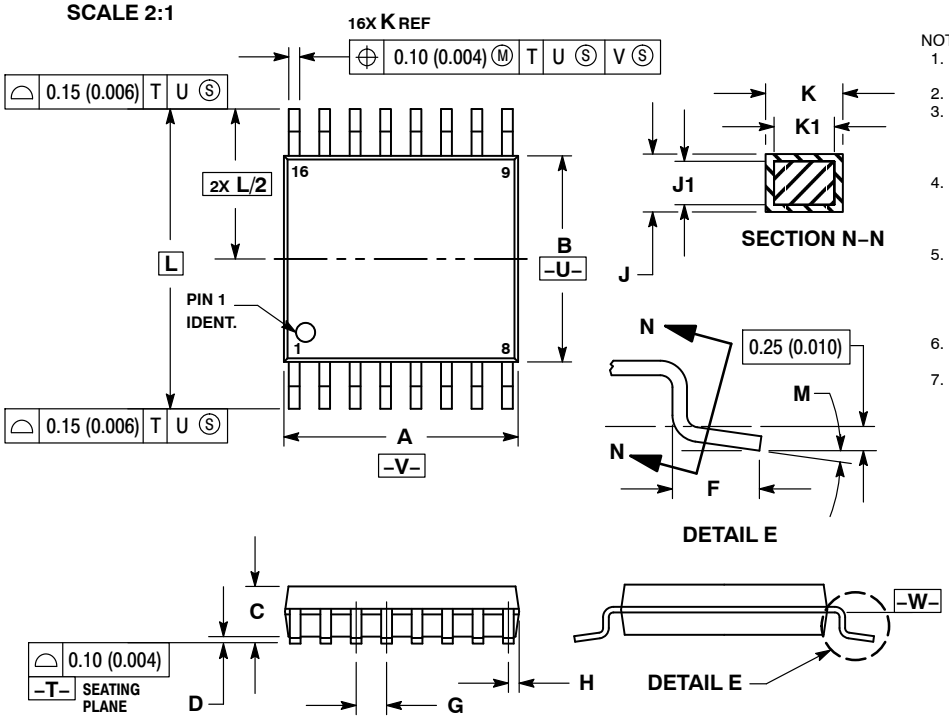
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SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

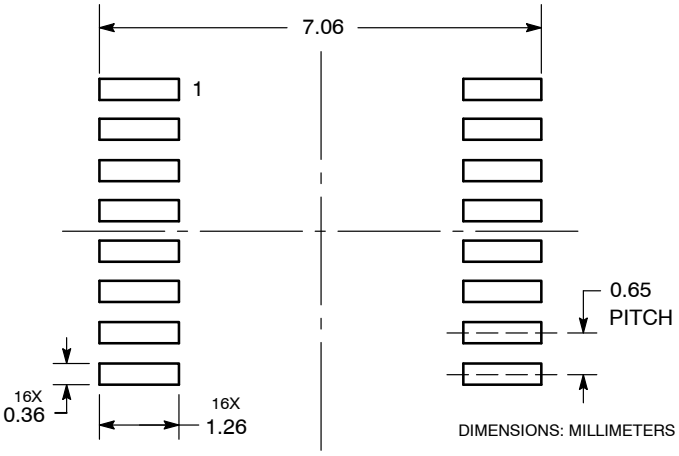
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

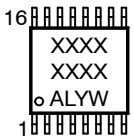
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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