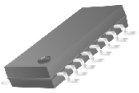
High-Current, High & Low-Side, Gate-Drive IC

FAN7391



SOIC14
14−SOP
CASE 751EF

Description

The FAN7391 is a monolithic high− and low−side gate−drive IC, which can drive high−speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross−conduction.

High−voltage process and common−mode noise−canceling techniques provide stable operation of the high−side driver under high−dv/dt noise circumstances. An advanced level−shift circuit offers high−side gate driver operation up to V_S = −9.8 V (typical) for V_{BS} = 15 V.

The advanced input filter of HIN provides protection against short−pulsed input signals caused by noise.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high−current and low−output voltage−drop feature makes this device suitable for the PDP sustain pulse driver, motor driver, switching mode power supply, and high−power DC−DC converter applications.

Features

- Floating Channels for Bootstrap Operation to +600 V
- Typically 4.5 A / 4.5 A Sourcing / Sinking Current Driving Capability
- Common−Mode dv/dt Noise−Canceling Circuit
- Built−in Under−Voltage Lockout for Both Channels
- Built−in Advanced Input Filter
- Matched Propagation Delay for Both Channels
- Logic (V_{SS}) and Power (COM) Ground ±5 V Offset
- 3.3 V and 5 V Input Logic Compatible
- Output In−Phase with Input
- This is a Pb−Free Device

Applications

- Plasma Display Panel (PDP) Sustain Driver
- High−Intensity Discharge (HID) Lamp Ballast
- Switching Mode Power Supply (SMPS)
- Motor Driver

Related Resources

- AN−6076 − Design and Application Guide of Bootstrap Circuit for High−Voltage Gate−Drive IC
- AN−9052 − Design Guide for Selection of Bootstrap Components
- AN−8102 − Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications

MARKING DIAGRAM



FAN7391 = Device Code
$Y = **onsemi** Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

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TYPICAL APPLICATION CIRCUIT

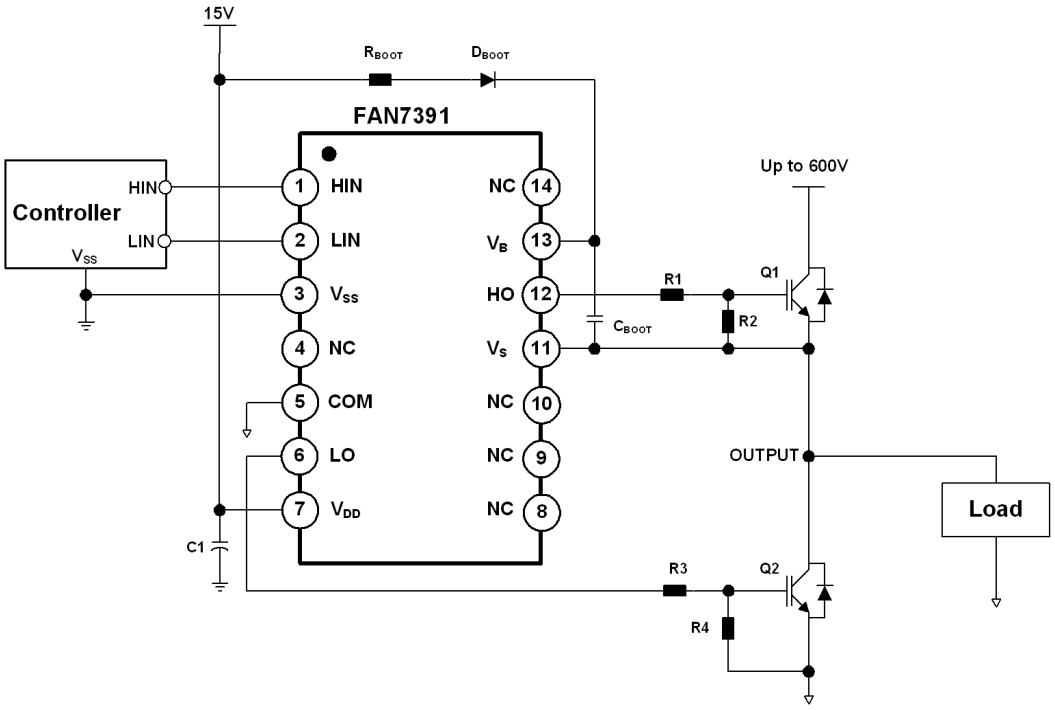


Figure 1. Application Circuit for Half−Bridge

INTERNAL BLOCK DIAGRAM

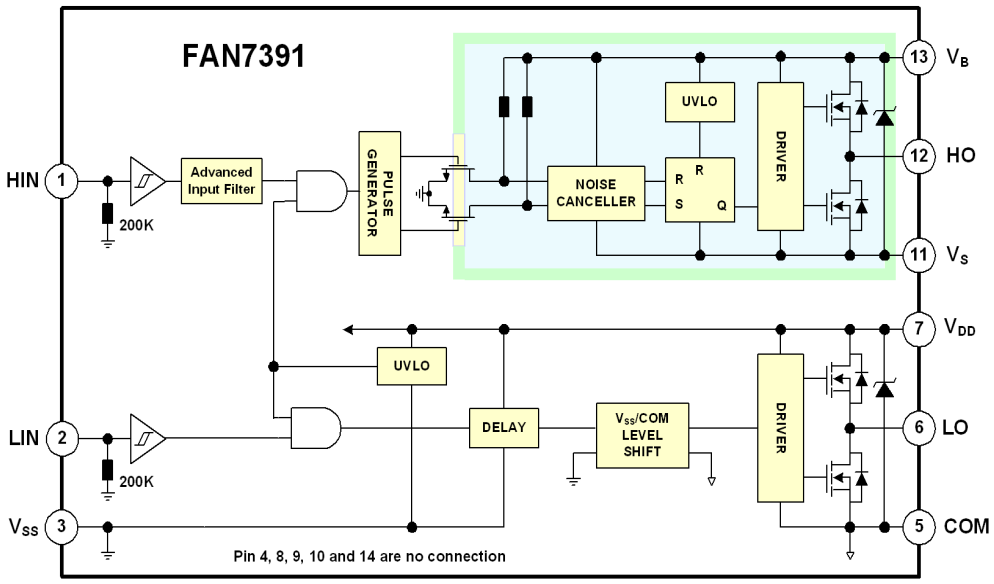


Figure 2. Functional Block Diagram

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PIN CONFIGURATION

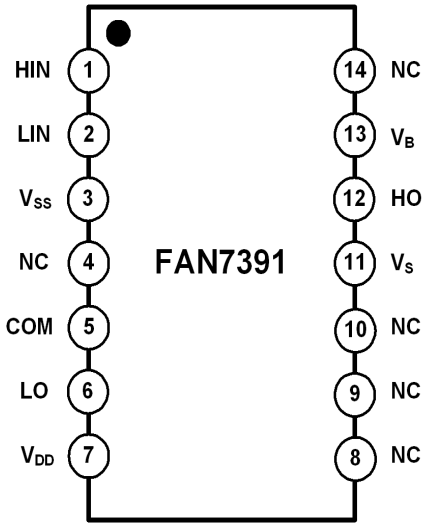


Figure 3. Pin Assignments (Top View)

PIN DEFINITIONS

14−Pin	Name	Description
1	HIN	Logic Input for High−Side Gate Driver Output
2	LIN	Logic Input for Low−Side Gate Driver Output
3	V_{SS}	Logic Ground
5	COM	Low−Side Driver Return
6	LO	Low−Side Driver Output
7	V_{DD}	Low−Side and Logic Part Supply Voltage
11	V_S	High−Voltage Floating Supply Return
12	HO	High−Side Driver Output
13	V_B	High−Side Floating Supply
4, 8, 9, 10, 14	NC	No Connect

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Characteristics	Min	Max	Unit
V_S	High−Side Floating Supply Offset Voltage	$V_B - V_{SHUNT}$	$V_B + 0.3$	V
V_B	High−Side Floating Supply Voltage	−0.3	625.0	V
V_{HO}	High−Side Floating Output Voltage, HO Pin	$V_S - 0.3$	$V_B + 0.3$	V
V_{DD}	Low−Side and Logic Fixed Supply Voltage	−0.3	V_{SHUNT}	V
V_{LO}	Low−Side Output Voltage, LO Pin	−0.3	$V_{DD} + 0.3$	V
V_{IN}	Logic Input Voltage (HIN and LIN)	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
V_{SS}	Logic Ground	$V_{DD} - 25$	$V_{DD} + 0.3$	V
dV_S/dt	Allowable Offset Voltage Slew Rate	−	50	V/ns
P_D (Note 1, 2, 3)	Power Dissipation	−	1.0	W
θ_{JA}	Thermal Resistance, Junction−to−Ambient	−	110	°C/W
T_J	Junction Temperature	−	+150	°C
T_{STG}	Storage Temperature	−	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR−4 glass epoxy material).
2. Refer to the following standards:
   JESD51−2: Integral circuits thermal test method environmental conditions − natural convection; and
   JESD51−3: Low effective thermal conductivity test board for leaded surface−mount packages.
3. Do not exceed P_D maximum under any circumstances.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_B	High−Side Floating Supply Voltage	$V_S + 10$	$V_S + 20$	V
V_S	High−Side Floating Supply Offset Voltage	$6 - V_{DD}$	600	V
V_{HO}	High−Side Output Voltage	V_S	V_B	V
V_{DD}	Low−Side and Logic Supply Voltage	10	20	V
V_{LO}	Low−Side Output Voltage	COM	V_{DD}	V
V_{IN}	Logic Input Voltage (HIN and LIN)	V_{SS}	V_{DD}	V
T_A	Operating Ambient Temperature	−40	+125	°C
PW_{HIN}	Pulse Width of Logic Input for High−Side Gate Driver	100	−	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD}, V_{BS}) = 15.0 V, V_S = V_{SS} = COM, T_A = 25°C, unless otherwise specified. The V_{IL}, V_{IH}, and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input signals HIN and LIN. The V_O and I_O parameters are referenced to COM and V_S is applicable to the respective output signals HO and LO.)

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
POWER SUPPLY SECTION (V_{DD} AND V_{BS})						
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} Supply Under−Voltage Positive−Going Threshold		8.0	8.8	9.8	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} Supply Under−Voltage Negative−Going Threshold		7.4	8.3	9.0	
V_{DDUVH} V_{BSUVH}	V_{DD} and V_{BS} Supply Under−Voltage Lockout Hysteresis Voltage		–	0.5	–	
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 600 V	–	–	50	μA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN} = 0 V or 5 V	–	45	80	
I_{QDD}	Quiescent V_{DD} Supply Current	V_{IN} = 0 V or 5 V	–	75	110	
I_{PBS}	Operating V_{BS} Supply Current	f_{IN} = 20 kHz, rms value	–	530	640	μA
I_{PDD}	Operating V_{DD} Supply Current	f_{IN} = 20 kHz, rms value	–	530	640	
SHUNT REGULATOR SECTION						
V_{SHUNT}	V_{DD} and V_{BS} Shunt Regulator Clamping Voltage	V_{DD} = Sweep or V_{BS} = Sweep, I_{SHUNT} = 5 mA	21	23	25	V
LOGIC INPUT SECTION (HIN, LIN)						
V_{IH}	Logic “1” Input Voltage		2.5	–	–	V
V_{IL}	Logic “0” Input Voltage		–	–	1.2	
I_{IN+}	Logic “1” Input Bias Current	V_{IN} = 5 V	–	25	50	μA
I_{IN-}	Logic “0” Input Bias Current	V_{IN} = 0 V	–	1.0	2.0	
R_{IN}	Input Pull−Down Resistance		100	200	–	kΩ
GATE DRIVER OUTPUT SECTION (HO, LO)						
V_{OH}	High−Level Output Voltage, V_{BIAS}−V_O	No Load	–	–	1.0	V
V_{OL}	Low−Level Output Voltage, V_O	No Load	–	–	35	mV
I_{O+}	Output High, Short−Circuit Pulsed Current (Note 4)	V_O = 0 V, V_{IN} = 5 V, PW < 1 0 μs	3.5	4.5		A
I_{O-}	Output Low, Short−Circuit Pulsed Current (Note 4)	V_O = 15 V, V_{IN} = 0 V, PW < 10 μs	3.5	4.5	–	
V_S	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO		–	−9.8	−7.0	V
V_{SS}−COM	V_{SS}−COM/COM−V_{SS} Voltage Endurability		−5	–	5	V

4. This parameter guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD}, V_{BS}) = 15.0 V, V_S = V_{SS} = COM = 0 V, C_L = 1000 pF, and T_A = 25°C unless otherwise specified.)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
ton	Turn−On Propagation Delay	V_S = 0 V	–	150	220	ns
toff	Turn−Off Propagation Delay	V_S = 0 V	–	150	220	
MT	Delay Matching, HS & LS Turn−On/Off		–	15	50	
t_r	Turn−On Rise Time		–	25	50	
t_f	Turn−Off Fall Time		–	20	45	

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TYPICAL CHARACTERISTICS

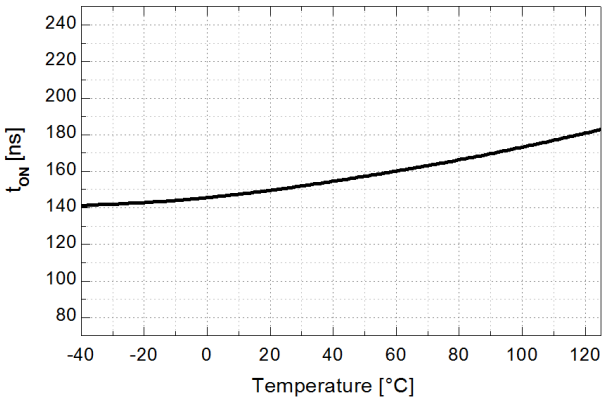


Figure 4. Turn−On Propagation Delay vs. Temperature

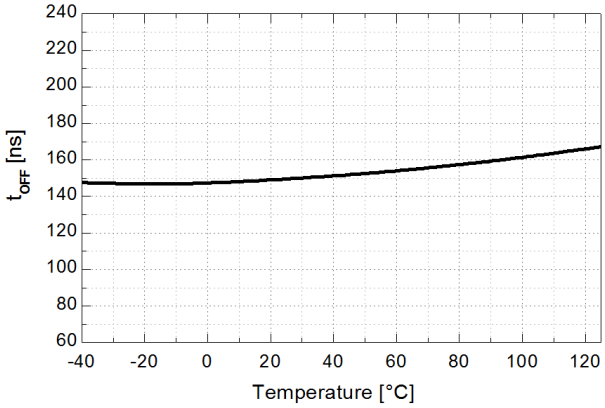


Figure 5. Turn−Off Propagation Delay vs. Temperature

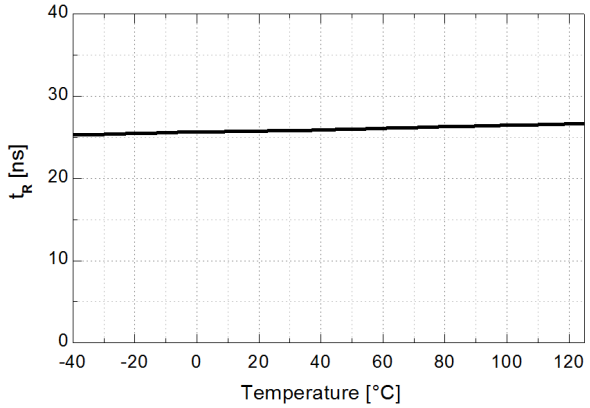


Figure 6. Turn−On Rise Time vs. Temperature

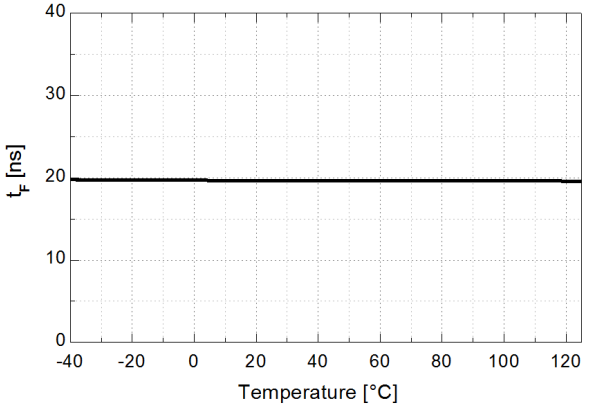


Figure 7. Turn−Off Fall Time vs. Temperature

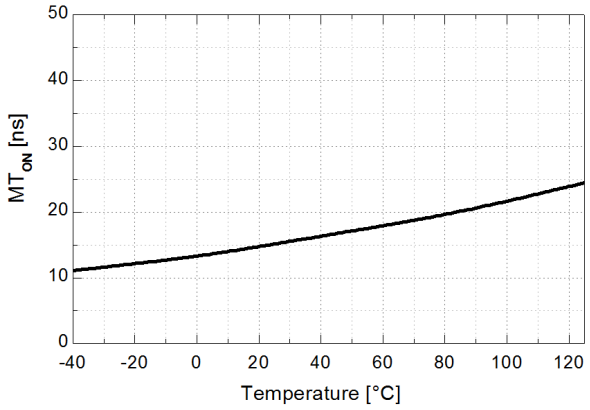


Figure 8. Turn−On Delay Matching vs. Temperature

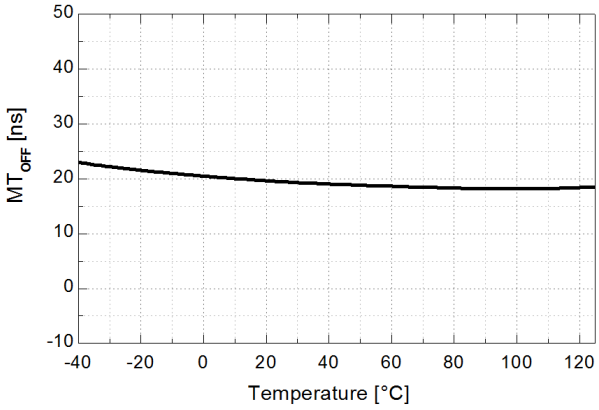


Figure 9. Turn−Off Delay Matching vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

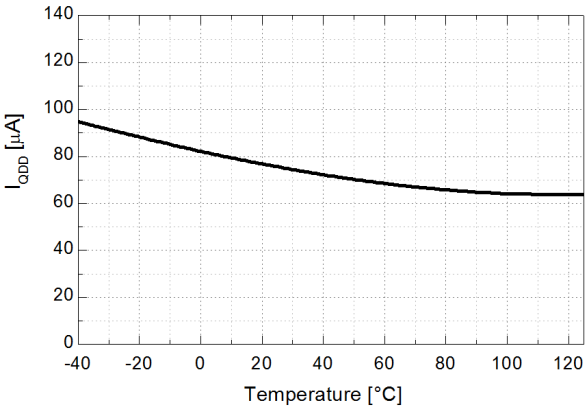


Figure 10. Quiescent V_{DD} Supply Current vs. Temperature

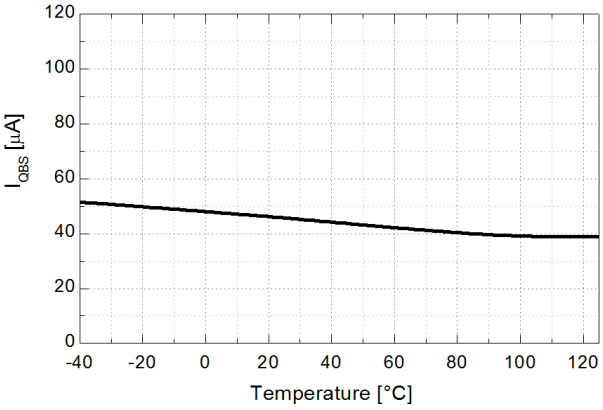


Figure 11. Quiescent V_{BS} Supply Current vs. Temperature

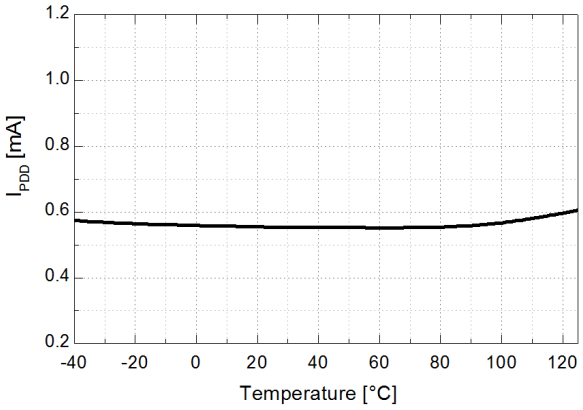


Figure 12. Operating V_{DD} Supply Current vs. Temperature

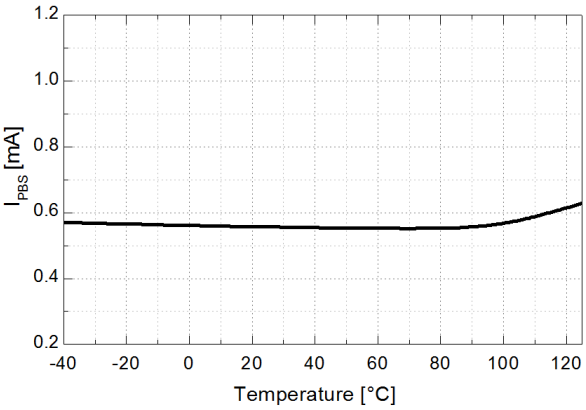


Figure 13. Operating V_{BS} Supply Current vs. Temperature

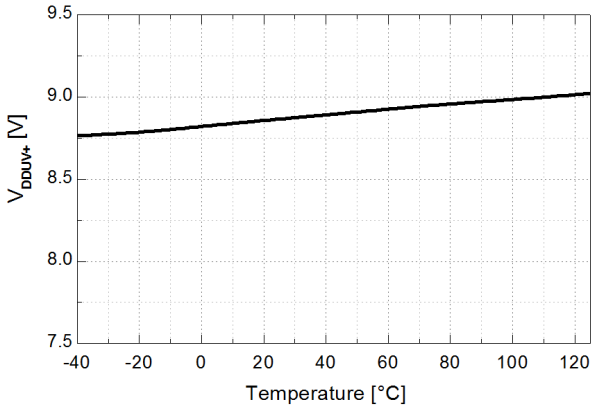


Figure 14. V_{DD} UVLO+ vs. Temperature

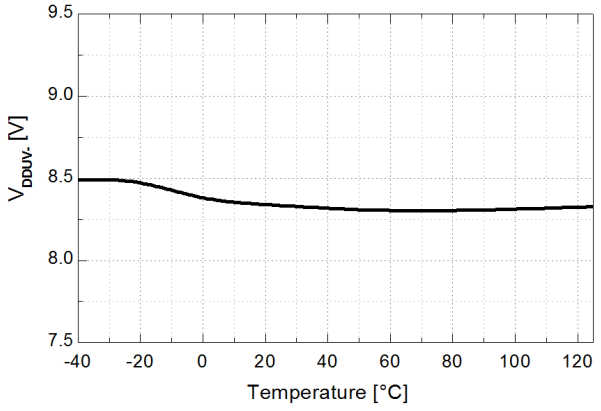


Figure 15. V_{DD} UVLO− vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

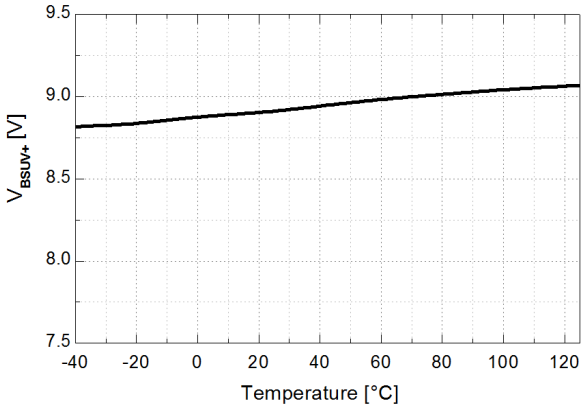


Figure 16. V_{BS} UVLO+ vs. Temperature

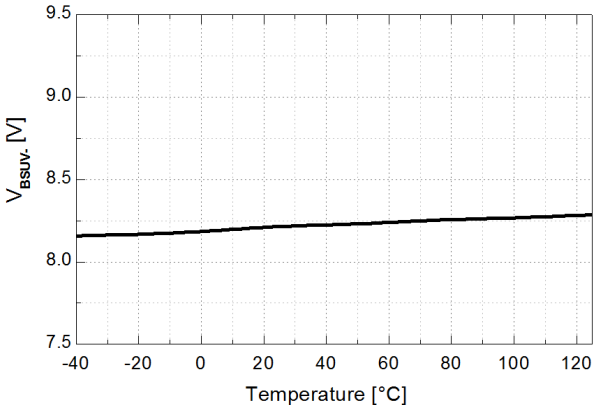


Figure 17. V_{BS} UVLO− vs. Temperature

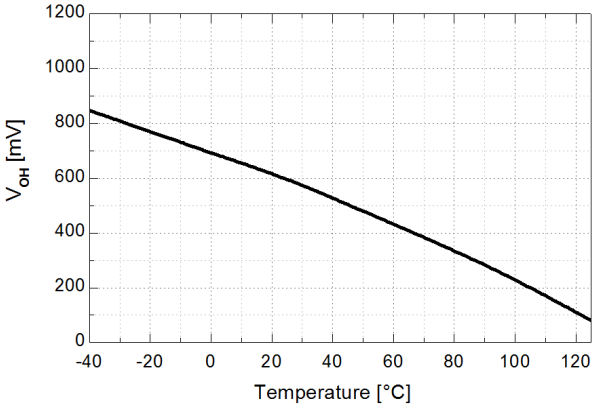


Figure 18. High−Level Output Voltage vs. Temperature

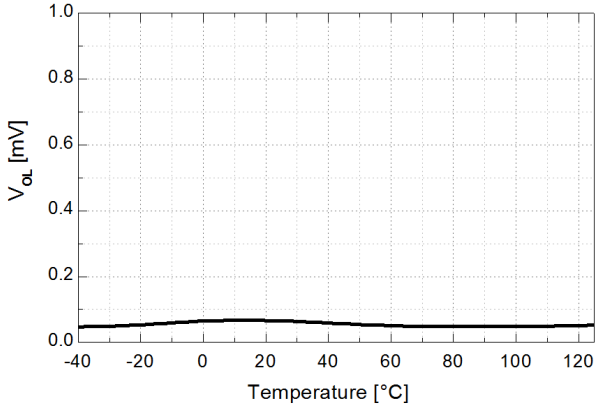


Figure 19. Low−Level Output Voltage vs. Temperature

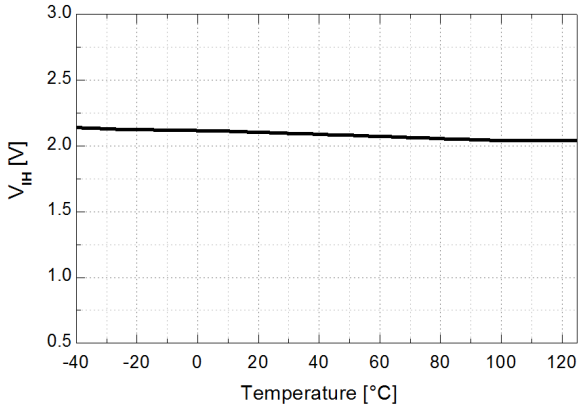


Figure 20. Logic HIGH Input Voltage vs. Temperature

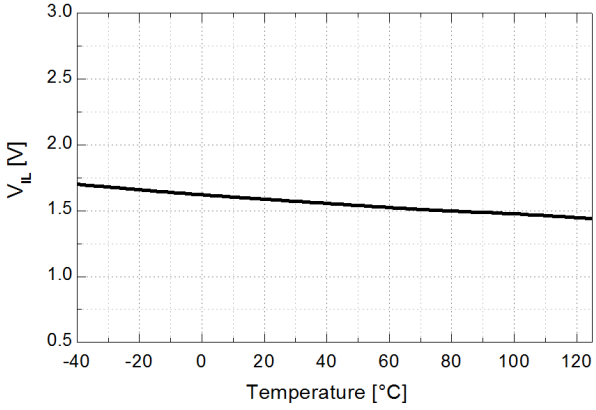


Figure 21. Logic LOW Input Voltage vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

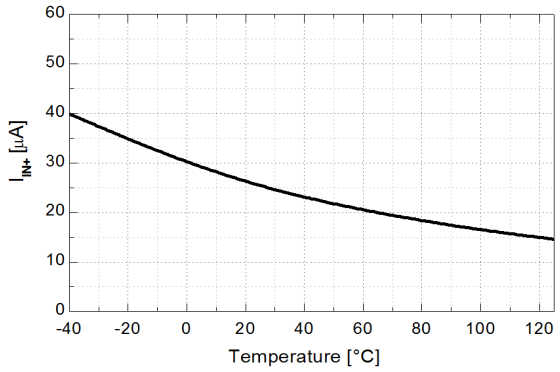


Figure 22. Logic Input High Bias Current vs. Temperature

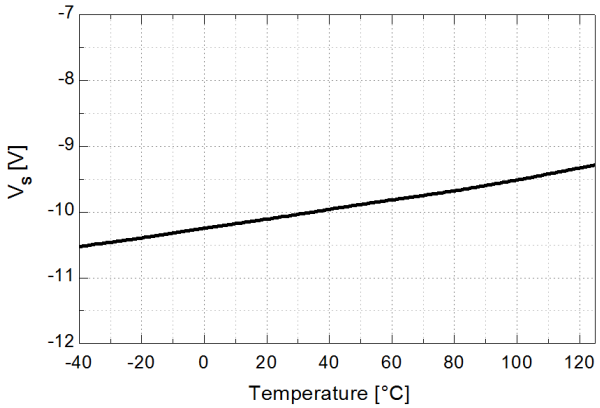


Figure 23. Allowable Negative V_S Voltage vs. Temperature

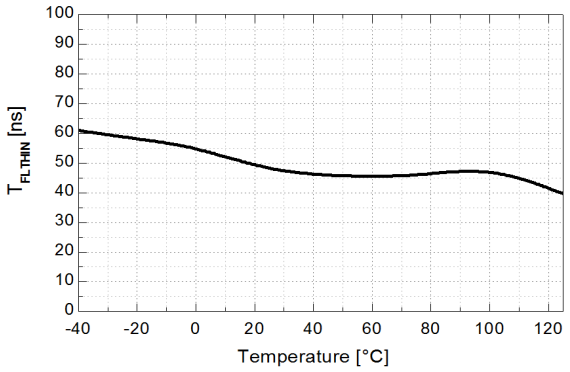


Figure 24. Input Filtering Time of HIN vs. Temperature

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SWITCHING TIME DEFINITIONS

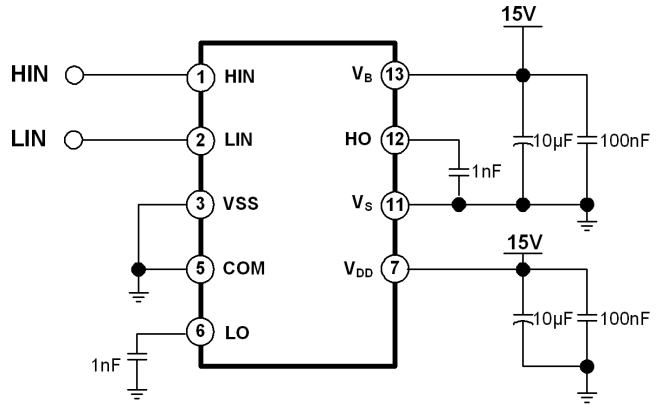


Figure 25. Switching Time Test Circuit (Referenced 14−SOP)

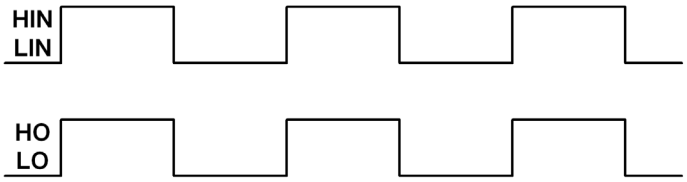


Figure 26. Input / Output Timing Diagram

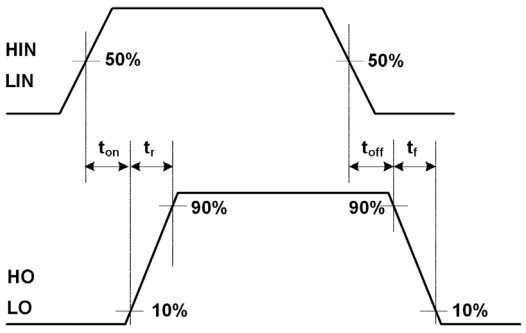


Figure 27. Switching Time Waveform Definitions

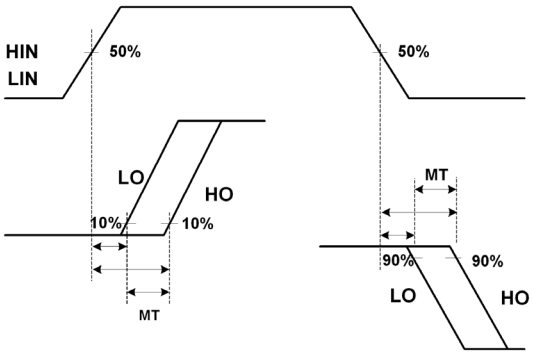


Figure 28. Delay Matching Waveform Definitions

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APPLICATIONS INFORMATION

Advanced Input Noise Filter

Figure 29 shows the input noise filter method, which has symmetry duration between the input signal (t_{INPUT}) and the output signal (t_{OUTPUT}) and helps to reject noise spikes and short pulses. This input filter is applied to the HIN. The upper pair of waveforms (Example A) shows an input signal duration (t_{INPUT}) much longer than input filter time (t_{FLTHIN}); it is approximately the same duration between the input signal time (t_{INPUT}) and the output signal time (t_{OUTPUT}). The lower pair of waveforms (Example B) shows an input signal time (t_{INPUT}) slightly longer than input filter time (t_{FLTHIN}); it is approximately the same duration between input signal time (t_{INPUT}) and the output signal time (t_{OUTPUT}).

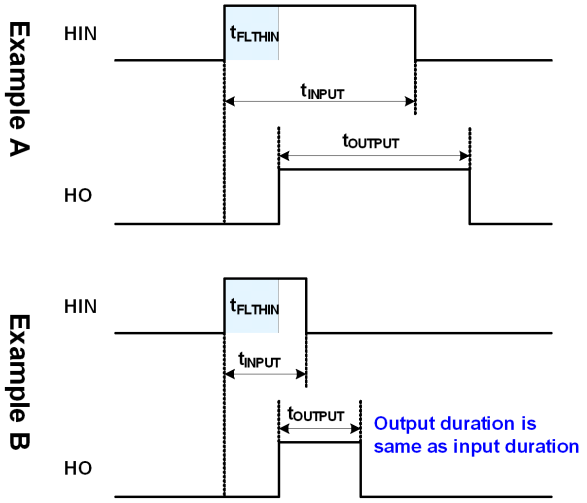


Figure 29. Input Noise Filter Definition

Short−Pulsed Input Noise Rejection Method

The Advanced input filter circuitry provides protection against short−pulsed input signals caused by noise.

If the input signal duration is less than input filter time (t_{FLTHIN}), the output does not change states.

Example A and B of the Figure 30 show the input and output waveforms with short−pulsed noise spikes with a duration less than input filter time; the output does not change states.

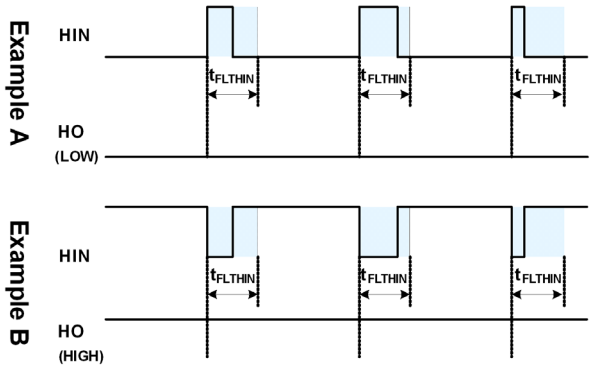


Figure 30. Noise Rejecting Input Filter Definition

Figure 31 shows the characteristics of the input filters while receiving narrow ON and OFF pulses. If input signal pulse duration, PW_{HIN}, is less than input filter time, t_{FLTHIN}; the output pulse, PW_{HO}, is zero. The input signal is rejected by input filter. Once the input signal pulse duration, PW_{HIN}, exceeds input filter time, t_{FLTHIN}, the output pulse durations, PW_{HO}, matches the input pulse durations, PW_{HIN}. FAN7391 input filter time, t_{FLTHIN}, is about 50 ns for the high−side outputs.

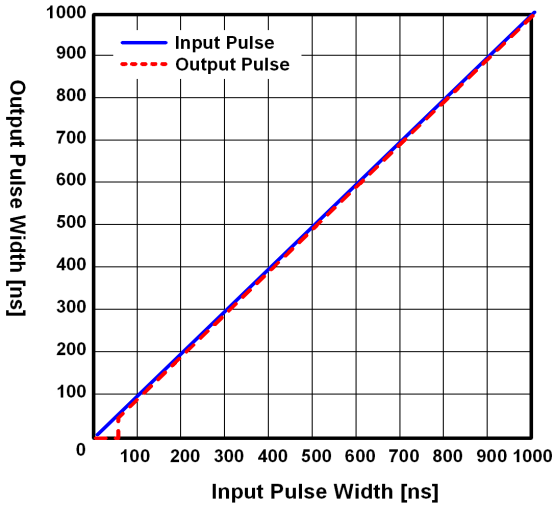


Figure 31. Input Filter Characteristic of Narrow ON

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Negative V_S Transient

The bootstrap circuit has the advantage of being simple and low cost, but has some limitations. The biggest difficulty with this circuit is the negative voltage present at the emitter of the high−side switching device when high− side switch is turned−off in half−bridge application.

If the high−side switch, Q1, turns−off while the load current is flowing to an inductive load, a current commutation occurs from high−side switch, Q1, to the diode, D2, in parallel with the low−side switch of the same inverter leg. Then the negative voltage present at the emitter of the high−side switching device, just before the freewheeling diode, D2, starts clamping, causes load current to suddenly flow to the low−side freewheeling diode, D2, as shown in Figure 32.

This negative voltage can be trouble for the gate driver's output stage, there is the possibility to develop an overvoltage condition of the bootstrap capacitor, input signal missing and latch−up problems because it directly affects the source V_S pin of the gate driver, as shown in Figure 33. This undershoot voltage is called "negative V_S transient".

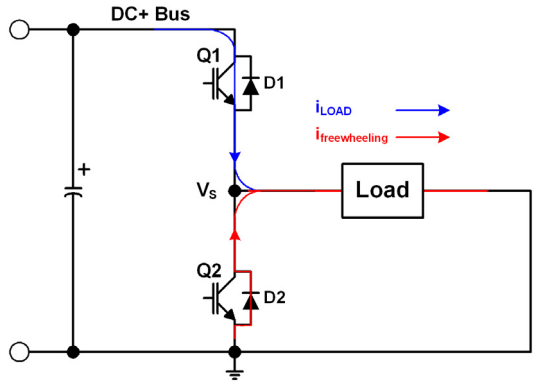


Figure 32. Half−Bridge Application Circuits

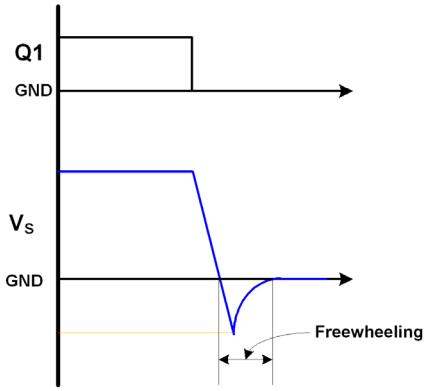


Figure 33. V_S Waveforms During Q1 Turn−Off

Figure 34 and Figure 35 show the commutation of the load current between high−side switch, Q1, and low−side freewheeling diode, D3, in same inverter leg. The parasitic inductances in the inverter circuit from the die wire bonding to the PCB tracks are jumped together in L_C and L_E for each IGBT. When the high−side switch, Q1, and low−side switch, Q4, are turned on, the V_{S1} node is below DC+ voltage by the voltage drops associated with the power switch and the parasitic inductances of the circuit due to load current is flows from Q1 and Q4, as shown in Figure 34. When the high−side switch, Q1, is turned off and Q4, remained turned on, the load current to flows the low−side freewheeling diode, D3, due to the inductive load connected to VS1 as shown in Figure 35. The current flows from ground (which is connected to the COM pin of the gate driver) to the load and the negative voltage present at the emitter of the high−side switching device.

In this case, the COM pin of the gate driver is at a higher potential than the V_S pin due to the voltage drops associated with freewheeling diode, D3, and parasitic elements, L_{C3} and L_{E3}.

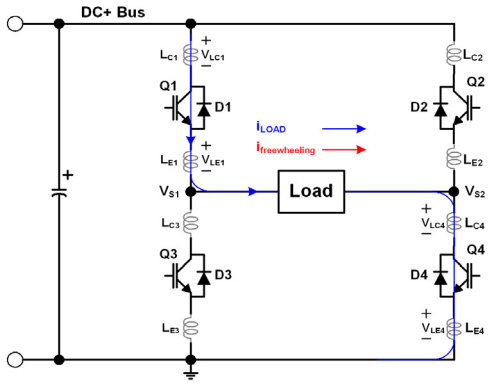


Figure 34. Q1 and Q4 Turn−On

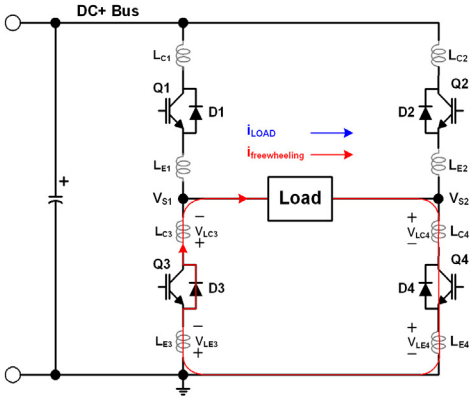


Figure 35. Q1 Turn−Off and D3 Conducting

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The FAN7391 has a negative V_S transient performance curve, as shown in Figure 36.

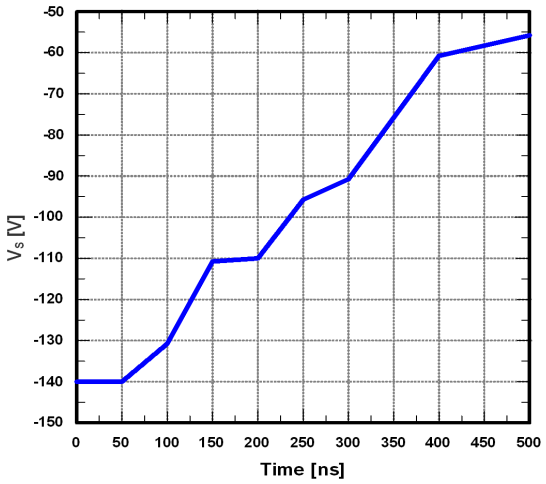


Figure 36. Negative V_S Transient Characteristic

Even though the FAN7391 has been shown able to handle these negative V_S transient conditions, it is strongly recommended that the circuit designer limit the negative V_S transient as much as possible by careful PCB layout to minimized the value of parasitic elements and component use. The amplitude of negative V_S voltage is proportional to the parasitic inductances and the turn−off speed, di/dt, of the switching device.

General Guidelines

Printed Circuit Board Layout

The layout recommended for minimized parasitic elements is as follows:

- Direct tracks between switches with no loops or deviation.
- Avoid interconnect links. These can add significant inductance.
- Reduce the effect of lead−inductance by lowering package height above the PCB.
- Consider co−locating both power switches to reduce track length.
- To minimize noise coupling, the ground plane should not be placed under or near the high−voltage floating side.
- To reduce the EM coupling and improve the power switch turn−on/off performance, the gate drive loops must be reduced as much as possible.

Placement of Components

The recommended placement and selection of component as follows:

- Place a bypass capacitor between the V_{DD} and V_{SS} pins. A ceramic 1 μF capacitor is suitable for most applications. This component should be placed as close as possible to the pins to reduce parasitic elements.
- The bypass capacitor from V_{CC} to COM supports both the low−side driver and bootstrap capacitor recharge. A value at least ten times higher than the bootstrap capacitor is recommended.
- The bootstrap resistor, R_{BOOT}, must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. If the resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM (ground). Recommended use is typically 5~10 Ω that increase the V_{BS} time constant. If the voltage drop of of bootstrap resistor and diode is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra−fast recovery diode can be used.
- The bootstrap capacitor, C_{BOOT}, uses a low−ESR capacitor, such as ceramic capacitor.

It is strongly recommended that the placement of components is as follows:

- Place components tied to the floating voltage pins (V_B and V_S) near the respective high−voltage portions of the device and the FAN7391. NC (not connected) pins in this package maximize the distance between the high−voltage and low−voltage pins (*see Figure 3*).
- Place and route for bypass capacitors and gate resistors as close as possible to gate drive IC.
- Locate the bootstrap diode, D_{BOOT}, as close as possible to bootstrap capacitor, C_{BOOT}.

The bootstrap diode must use a lower forward voltage drop and minimal switching time as soon as possible for fast recovery or ultra−fast diode.

ORDERING INFORMATION

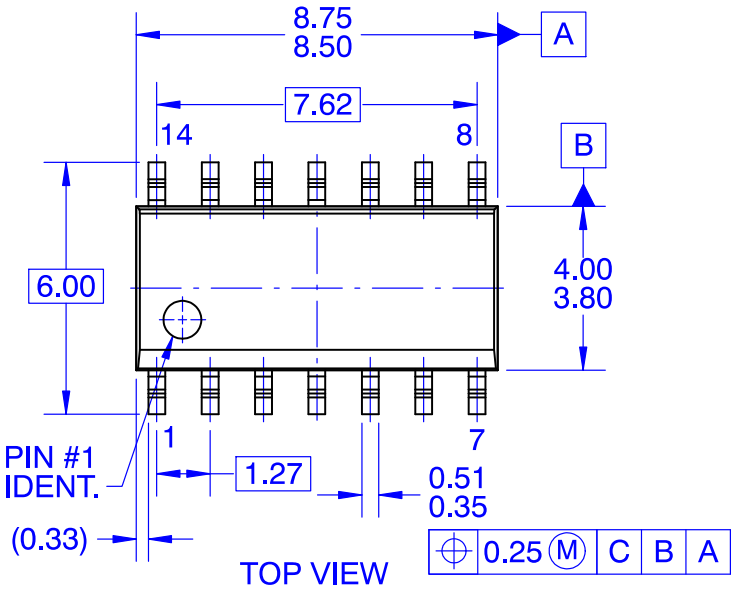
Device	Package	Operating Temperature Range	Shipping†
FAN7391MX	SOIC14 14−SOP (Pb−Free)	−40°C~125°C	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

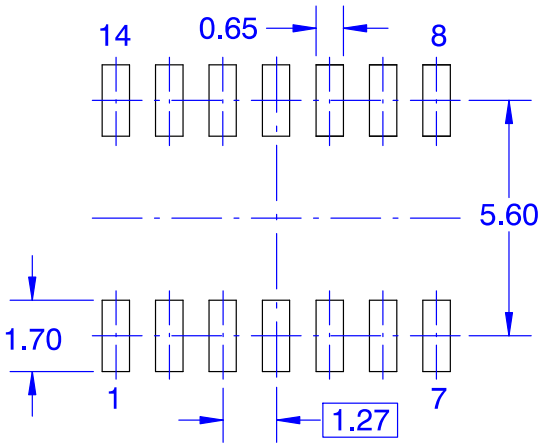
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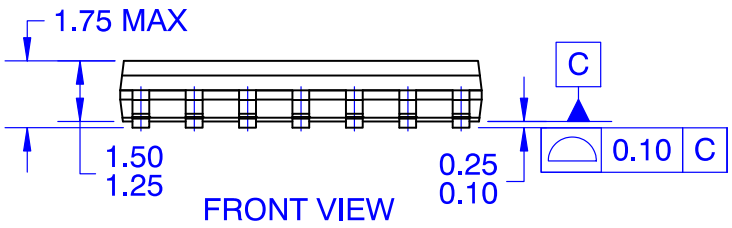
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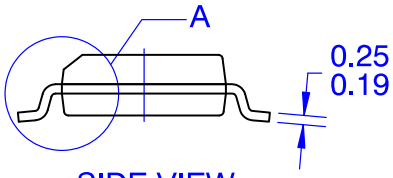
TOP VIEW



LAND PATTERN RECOMMENDATION

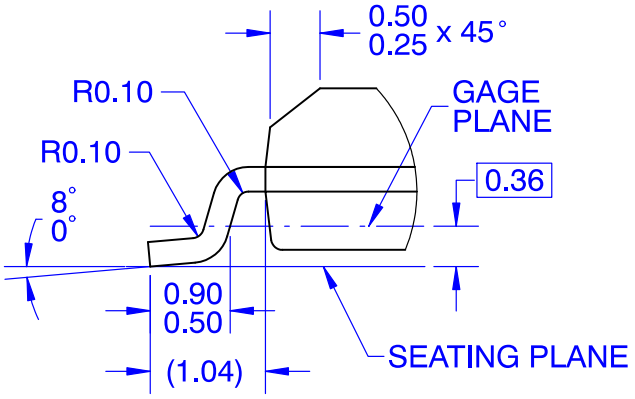


FRONT VIEW



SIDE VIEW

NOTES:
A. CONFORMS TO JEDEC MS−012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145−14M
E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

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