Octal D-Type Flip-Flop with 3-State Outputs

With 5V−Tolerant Inputs

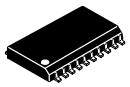
MC74LVX374

The MC74LVX374 is an advanced high speed CMOS octal D−type flip−flop with 3−state outputs. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8−bit D−type flip−flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

Features

- High Speed: f_{max} = 160 MHz (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb−Free and are RoHS Compliant

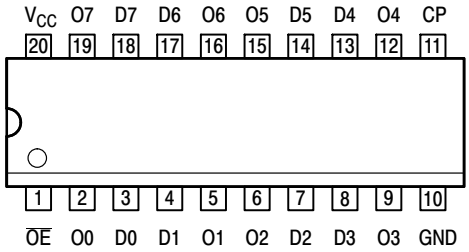


SOIC−20
DW SUFFIX
CASE 751D



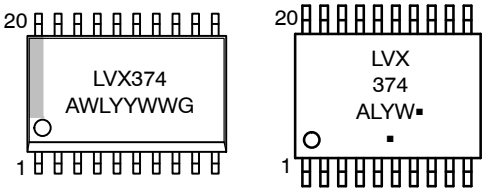
TSSOP−20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT



20−Lead (Top View)

MARKING DIAGRAMS



SOIC−20 **TSSOP−20**

LVX374	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
CP	Clock Pulse Input
D0−D7	Data Inputs
O0−O7	3−State Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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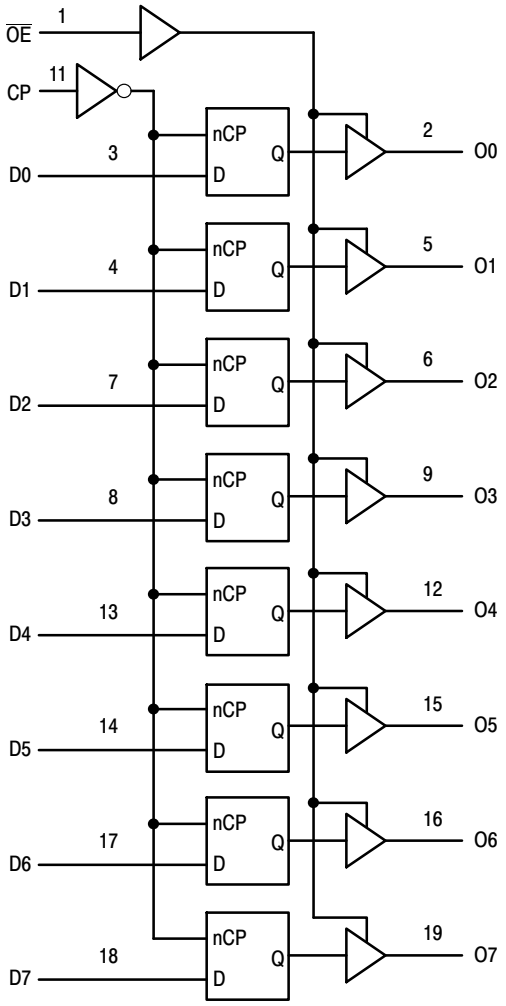


Figure 1. Logic Diagram

INPUTS			OUTPUTS	
$\overline{OE}$	CP	Dn	On	OPERATING MODE
L L	↑ ↑	l h	L H	Load and Read Register
L	↑	X	NC	Hold and Read Register
H	↑	X	Z	Hold and Disable Outputs
H H	↑ ↑	l h	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low−to−High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low−to−High Clock Transition; NC = No Change, State Prior to Low−to−High Clock Transition; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↑ Low−to−High Transition; ↑ Not a Low−to−High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_{in}	DC Input Voltage	−0.5 to +7.0	V
V_{out}	DC Output Voltage	−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	−20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low−Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High−Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low−Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5 V or GND	3.6			±0.1		±1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 2.7 V	C_L = 15 pF	60	115		50		MHz
			C_L = 50 pF	45	60		40		
		V_{CC} = 3.3 ± 0.3 V	C_L = 15 pF	100	160		85		
			C_L = 50 pF	60	95		55		
t_{PLH}, t_{PHL}	Propagation Delay CP to O	V_{CC} = 2.7 V	C_L = 15 pF		8.5	16.3	1.0	19.5	ns
			C_L = 50 pF		11.0	19.8	1.0	23.0	
		V_{CC} = 3.3 ± 0.3 V	C_L = 15 pF		6.7	10.6	1.0	12.5	
			C_L = 50 pF		9.2	14.1	1.0	16.0	
t_{PZL}, t_{PZH}	Output Enable Time $\overline{OE}$ to O	V_{CC} = 2.7 V, R_L = 1 kΩ	C_L = 15 pF		7.6	14.5	1.0	17.5	ns
			C_L = 50 pF		10.1	18.0	1.0	21.0	
		V_{CC} = 3.3 ± 0.3 V, R_L = 1 kΩ	C_L = 15 pF		5.9	9.3	1.0	11.0	
			C_L = 50 pF		8.4	12.8	1.0	14.5	
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OE}$ to O	V_{CC} = 2.7 V, R_L = 1 kΩ	C_L = 50 pF		11.5	18.5	1.0	22.0	ns
		V_{CC} = 3.3 ± 0.3 V, R_L = 1 kΩ	C_L = 50 pF		9.6	13.2	1.0	15.0	
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 1)	V_{CC} = 2.7 V	C_L = 50 pF			1.5		1.5	ns
		V_{CC} = 3.3 ± 0.3 V	C_L = 50 pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
Cin	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three−State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2)		32				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.5	−0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Typ	$T_A = 25°C$ Limit	$T_A = -40$ to $85°C$ Limit	Unit
t_w	Minimum Pulse Width, CP	V_{CC} = 2.7 V		7.5	8.0	ns
		V_{CC} = 3.3 ± 0.3 V		5.0	5.5	
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 2.7 V		6.5	6.5	ns
		V_{CC} = 3.3 ± 0.3 V		4.5	4.5	
t_h	Minimum Hold Time, D to CP	V_{CC} = 2.7 V		2.0	2.0	ns
		V_{CC} = 3.3 ± 0.3 V		2.0	2.0	

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SWITCHING WAVEFORMS

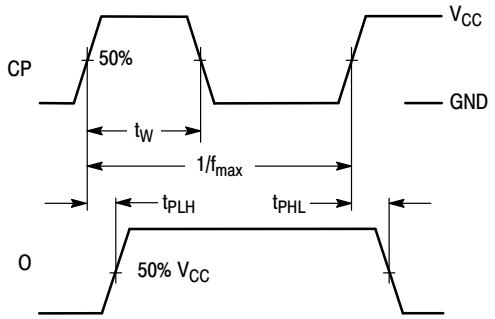


Figure 2.

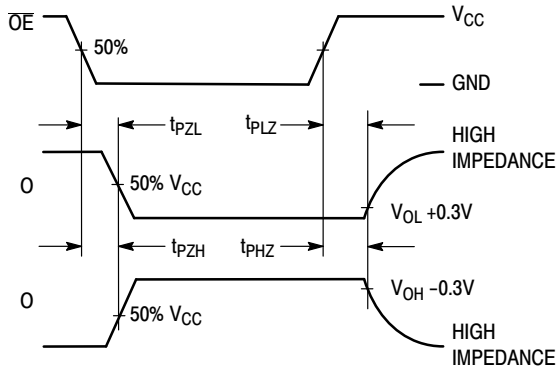


Figure 3.

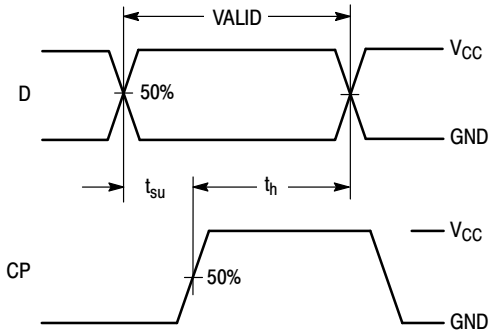
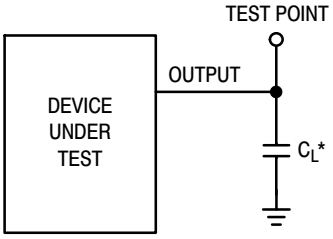


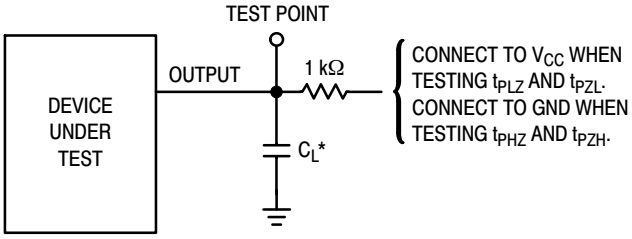
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



*Includes all probe and jig capacitance

Figure 6. Three−State Test Circuit

ORDERING INFORMATION

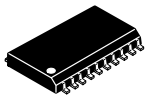
Device	Package	Shipping†
MC74LVX374DWR2G	SOIC−20 (Pb−Free)	1000 Tape & Reel
MC74LVX374DTR2G	TSSOP−20 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

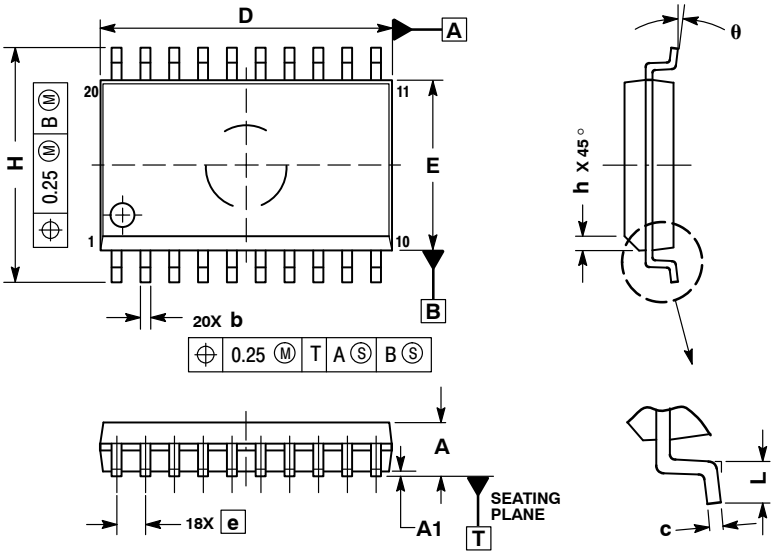
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SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



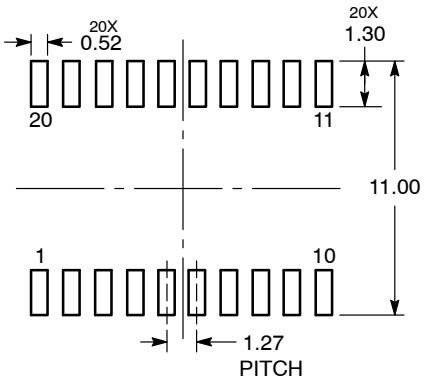
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

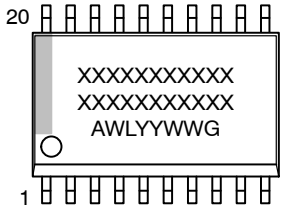
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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