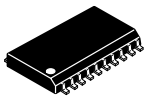
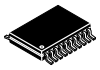
# Octal 3-STATE Buffer

# MM74HC244



SOIC−20
CASE 751BJ



TSSOP−20
CASE 948AQ



TSSOP−20 WB
CASE 948E

## General Description

The MM74HC244 is a non−inverting buffer and has two active low enables ($1\overline{G}$ and $2\overline{G}$); each enable independently controls 4 buffers. This device does not have Schmitt trigger inputs.

These 3−STATE buffers utilize advanced silicon−gate CMOS technology and are general purpose high speed non−inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. All three devices have a fanout of 15 LS−TTL equivalent inputs.

All inputs are protected from damage due to static discharge by diodes to $V_{CC}$ and ground.

## Features

- Typical Propagation Delay: 14 ns
- 3−STATE Outputs for Connection to System Buses
- Wide Power Supply Range: 2–6 V
- Low Quiescent Supply Current: 160 μA
- Output Current: 6 mA
- These are Pb−Free Devices

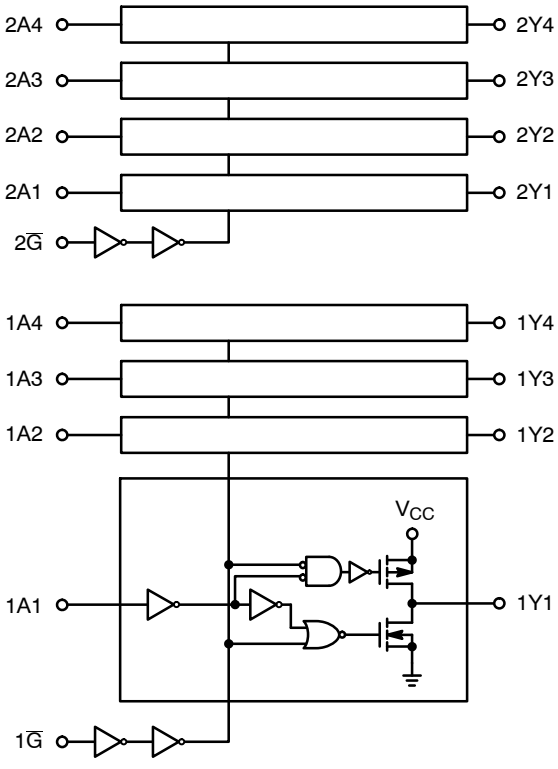
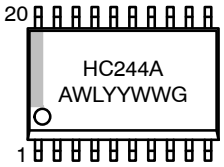
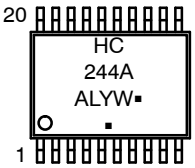



**Figure 1. Logic Diagram**

## MARKING DIAGRAMS




(SOIC−20)

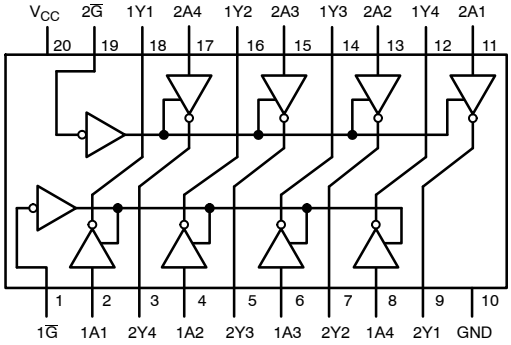



(TSSOP−20,
TSSOP−20WB)

| | |
|---|---|
| HC240A | = Specific Device Code |
| A | = Assembly Location |
| L/WL | = Wafer Lot |
| Y/YY | = Year |
| W/WW | = Work Week |
| ▪ or G | = Pb−Free Package |

(Note: Microdot may be in either location)

## CONNECTION DIAGRAM




(Top View)

## TRUTH TABLE

| $1\overline{G}$ | 1A | 1Y | $2\overline{G}$ | 2A | 2Y |
|---|---|---|---|---|---|
| L | L | L | L | L | L |
| L | H | H | L | H | H |
| H | L | Z | H | L | Z |
| H | H | Z | H | H | Z |

H = HIGH Level
L = LOW Level
Z = HIGH Impedance

## ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 4 of this data sheet.

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## MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage | −0.5 to $V_{CC}$ + 0.5 | V |
| $V_{OUT}$ | DC Output Voltage | −0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$, $I_{OK}$ | Clamp Diode Current | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | ±35 | mA |
| $I_{CC}$ | DC VCC or GND Current, per Pin | ±70 | mA |
| $T_{STG}$ | Storage Temperature Range | −65 to +150 | °C |
| $P_D$ | Power Dissipation<br>SOIC−20W<br>TSSOP−20 | <br>1302<br>833 | mW |
| $T_L$ | Lead Temperature (Soldering 10 seconds) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

## RECOMMENDED OPERATIONG CONDITIONS (Note 1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 | 6 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input or Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Times<br>$V_{CC}$ = 2.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | <br>−<br>−<br>− | <br>1000<br>500<br>400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Note 2)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | −40°C ≤ $T_A$ ≤ 85°C | −55°C ≤ $T_A$ ≤ 125°C | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | 2.0<br>4.5<br>6.0 | −<br>−<br>− | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | 2.0<br>4.5<br>6.0 | −<br>−<br>− | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 20 μA | 2.0<br>4.5<br>6.0 | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 6.0 mA<br>$\|I_{OUT}\|$ ≤ 7.8 mA | <br>4.5<br>6.0 | <br>4.2<br>5.7 | <br>3.98<br>5.4 | <br>3.84<br>5.34 | <br>3.7<br>5.2 | V |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 20 μA | 2.0<br>4.5<br>6.0 | 0<br>0<br>0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 6.0 mA<br>$\|I_{OUT}\|$ ≤ 7.8 mA | <br>4.5<br>6.0 | <br>0.2<br>0.2 | <br>0.26<br>0.26 | <br>0.33<br>0.33 | <br>0.4<br>0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0 | − | ±0.1 | ±1.0 | ±1.0 | μA |



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**DC ELECTRICAL CHARACTERISTICS** (Note 2) (continued)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | −40°C ≤ $T_A$ ≤ 85°C | −55°C ≤ $T_A$ ≤ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | | |
| $I_{OZ}$ | Maximum 3−STATE Output Leakage Current | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND<br>$\overline{G}$ = $V_{IH}$ | 6.0 | − | ±0.5 | ±5 | ±10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND<br>$I_{OUT}$ = 0 μA | 6.0 | − | 8.0 | 80 | 160 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For a power supply of 5 V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5 V and 4.5 V respectively. (The $V_{IH}$ value at 5.5 V is 3.85 V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

**AC ELECTRICAL CHARACTERISTICS**

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Unit |
|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | $C_L$ = 45 pF | 14 | 20 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum Enable Delay to Active Output | $R_L$ = 1 kΩ, $C_L$ = 45 pF | 17 | 28 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Maximum Disable Delay from Active Output | $R_L$ = 1 kΩ, $C_L$ = 5 pF | 15 | 25 | ns |

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 2.0 V to 6.0 V, $C_L$ = 50 pF, $t_r$ = $t_f$ = 6 ns (unless otherwise specified))

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | −40°C ≤ $T_A$ ≤ 85°C | −55°C ≤ $T_A$ ≤ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | $C_L$ = 50 pF<br>$C_L$ = 150 pF | 2.0<br>2.0 | 58<br>83 | 115<br>165 | 145<br>208 | 171<br>246 | ns |
| | | $C_L$ = 50 pF<br>$C_L$ = 150 pF | 4.5<br>4.5 | 14<br>17 | 23<br>33 | 29<br>42 | 34<br>49 | ns |
| | | $C_L$ = 50 pF<br>$C_L$ = 150 pF | 6.0<br>6.0 | 10<br>14 | 20<br>28 | 25<br>35 | 29<br>42 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum Output Enable Time | $R_L$ = 1 kΩ<br>$C_L$ = 50 pF<br>$C_L$ = 150 pF | 2.0<br>2.0 | 75<br>100 | 150<br>200 | 189<br>252 | 224<br>298 | ns |
| | | $C_L$ = 50 pF<br>$C_L$ = 150 pF | 4.5<br>4.5 | 15<br>30 | 30<br>40 | 38<br>50 | 45<br>60 | ns |
| | | $C_L$ = 50 pF<br>$C_L$ = 150 pF | 6.0<br>6.0 | 13<br>17 | 26<br>34 | 32<br>43 | 38<br>51 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Maximum Output Disable Time | $R_L$ = 1 kΩ<br>$C_L$ = 50 pF | 2.0<br>4.5<br>6.0 | 75<br>15<br>13 | 150<br>30<br>26 | 189<br>38<br>32 | 224<br>45<br>38 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Rise and Fall Time | | 2.0<br>4.5<br>6.0 | −<br>−<br>− | 60<br>12<br>10 | 75<br>15<br>13 | 90<br>18<br>15 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 3) | (per buffer)<br>$\overline{G}$ = $V_{IH}$<br>$\overline{G}$ = $V_{IL}$ | <br>−<br>− | <br>12<br>50 | <br>−<br>− | <br>−<br>− | <br>−<br>− | pF |
| $C_{IN}$ | Maximum Input Capacitance | | − | 5 | 10 | 10 | 10 | pF |
| $C_{OUT}$ | Maximum Output Capacitance | | − | 10 | 20 | 20 | 20 | pF |

3. $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} \cdot V_{CC}^2 \cdot f + I_{CC} \cdot V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \cdot V_{CC} \cdot f + I_{CC}$.



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## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MM74HC244WM | SOIC−20<br>(Pb−Free) | 38 Units / Tube |
| MM74HC244WMX | SOIC−20<br>(Pb−Free) | 1000 / Tape & Reel |
| MM74HC244MTC | TSSOP−20 WB<br>(Pb−Free) | 75 Units / Tube |
| MM74HC244MTCX | TSSOP−20<br>(Pb−Free) | 2500 / Tape & Reel |

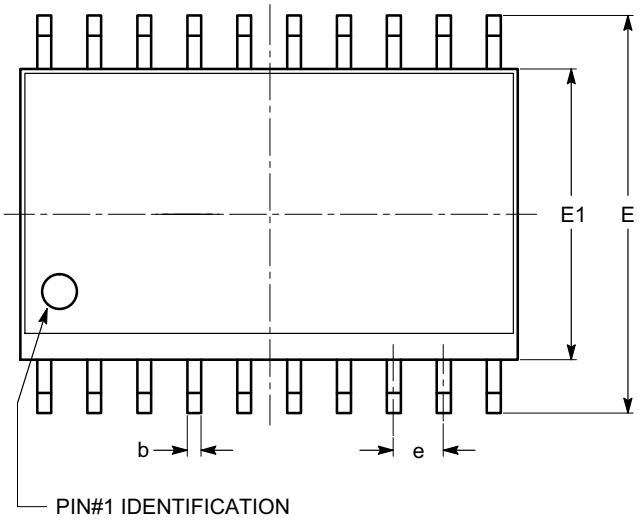
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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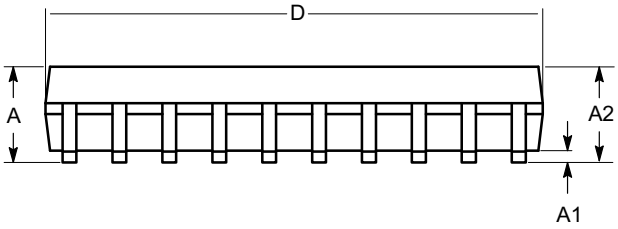
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CASE 751BJ
ISSUE O

DATE 19 DEC 2008

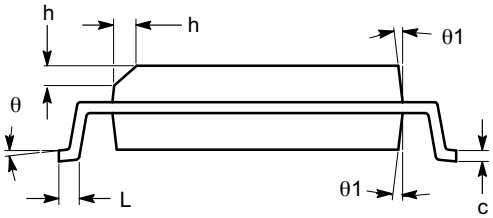



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 2.36 | 2.49 | 2.64 |
| A1 | 0.10 | | 0.30 |
| A2 | 2.05 | | 2.55 |
| b | 0.31 | 0.41 | 0.51 |
| c | 0.20 | 0.27 | 0.33 |
| D | 12.60 | 12.80 | 13.00 |
| E | 10.01 | 10.30 | 10.64 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.75 |
| L | 0.40 | 0.81 | 1.27 |
| θ | 0° | | 8° |
| θ1 | 5° | | 15° |




**SIDE VIEW**




**END VIEW**

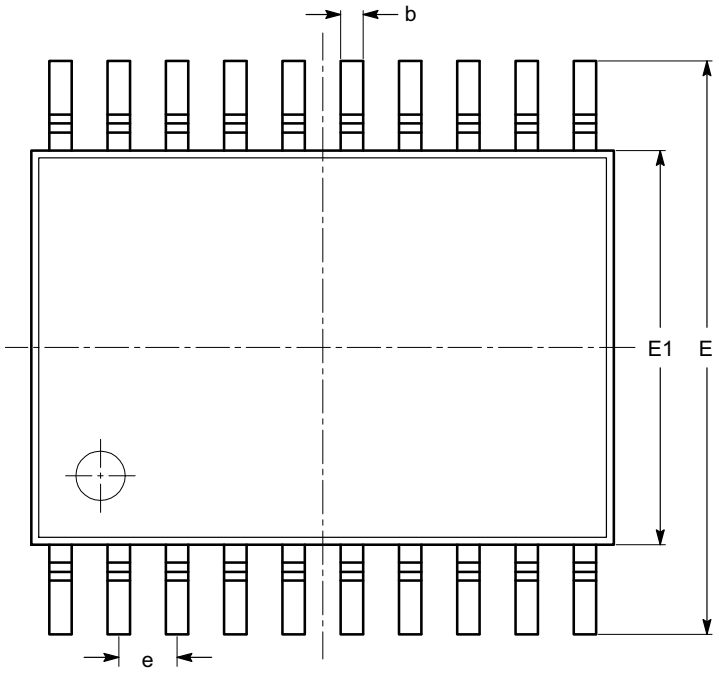
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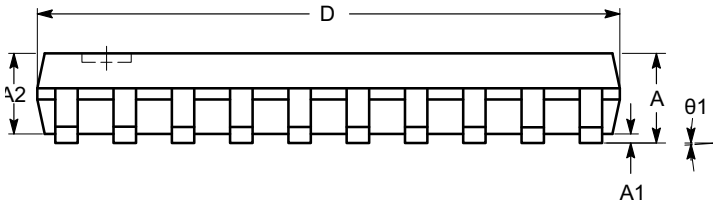
**TSSOP20, 4.4x6.5**
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

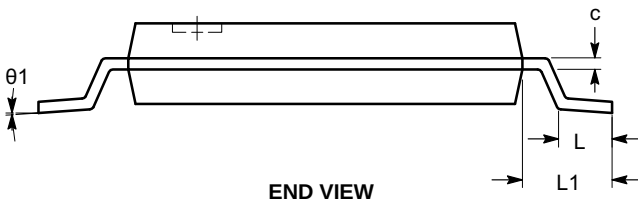



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 6.40 | 6.50 | 6.60 |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | | 0.65 BSC | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 REF | |
| θ | 0° | | 8° |




SIDE VIEW




END VIEW

**Notes:**
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(2) Complies with JEDEC MO-153.

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