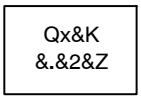
IntelliMAX™ Dual-Input Single-Output Advanced Power Switch with True Reverse-Current Blocking

FPF1320, FPF1321



WLCSP−6
CASE 567RM

MARKING DIAGRAM



Qx	= Specific Device Code x = S or T
&K	= Traceability Code
&.	= Pin one dot
&2	= Date Code
&Z	= Assembly plant code

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page See detailed ordering and shipping information on page 12 of this data sheet.

Description

The FPF1320/21 is a Dual−Input Single−Output (DISO) load switch consisting of two sets of slew−rate controlled, low on−resistance, P−channel MOSFET switches and integrated analog features. The slew−rate−controlled turn−on characteristic prevents inrush current and the resulting excessive voltage droop on the power rails. The input voltage range operates from 1.5 V to 5.5 V to align with the requirements of low−voltage portable device power rails. FPF1320/21 performs seamless power−source transitions between two input power rails using the SEL pin with advanced break−before−make operation.

FPF1320/21 has a TRCB function to block unwanted reverse current from output to input during ON/OFF states. The switch is controlled by logic inputs of the SEL and EN pins, which are capable of interfacing directly with low−voltage control signals (GPIO).

FPF1321 has 65 Ω on−chip load resistor for output quick discharge when EN is LOW.

FPF1320/21 is available in 1.0 mm x 1.5 mm WLCSP, 6−bump, with 0.5 mm pitch. FPF1321B is available in 1.0 mm x 1.5 mm WLCSP, 6−bump, 0.5 mm pitch with backside laminate.

Features

- DISO Load Switches
- Input Supply Operating Range: 1.5 V ~ 5.5 V
- R_{ON} 50 mΩ at V_{IN} = 3.3 V Per Channel (Typical)
- True Reverse − Current Blocking (TRCB)
- Fixed Slew Rate Controlled 130 μs for < 1 μF C_{OUT}
- I_{SW}: 1.5 A Per Channel (Maximum)
- Quick Discharge Feature on FPF1321
- Logic CMOS IO Meets JESD76 Standard for GPIO Interface and Related Power Supply Requirements
- ESD Protected:
  - Human Body Model: > 6 kV
  - Charged Device Model: > 1.5 kV
  - IEC 61000−4−2 Air Discharge: > 15 kV
  - IEC 61000−4−2 Contact Discharge: > 8 kV
- These are Pb−Free and Halide Free Devices

Applications

- Smart Phones / Tablet PCs
- Portable Devices
- Near Field Communication (NFC) Capable SIM Card Power Supply

© Semiconductor Components Industries, LLC, 2011

APPLICATION DIAGRAM

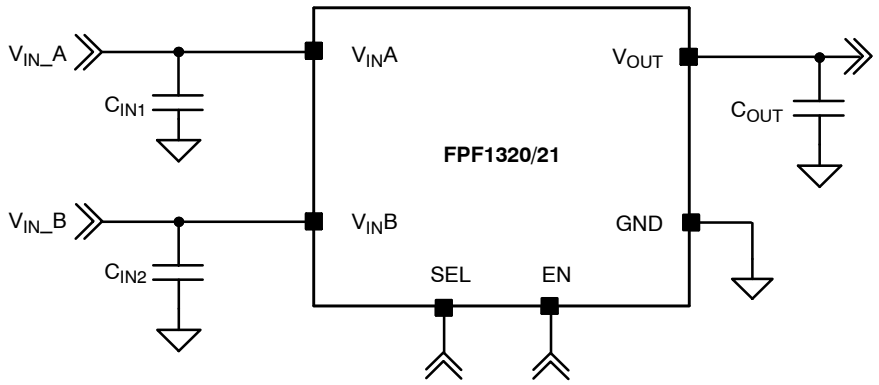


Figure 1. Typical Application

BLOCK DIAGRAM

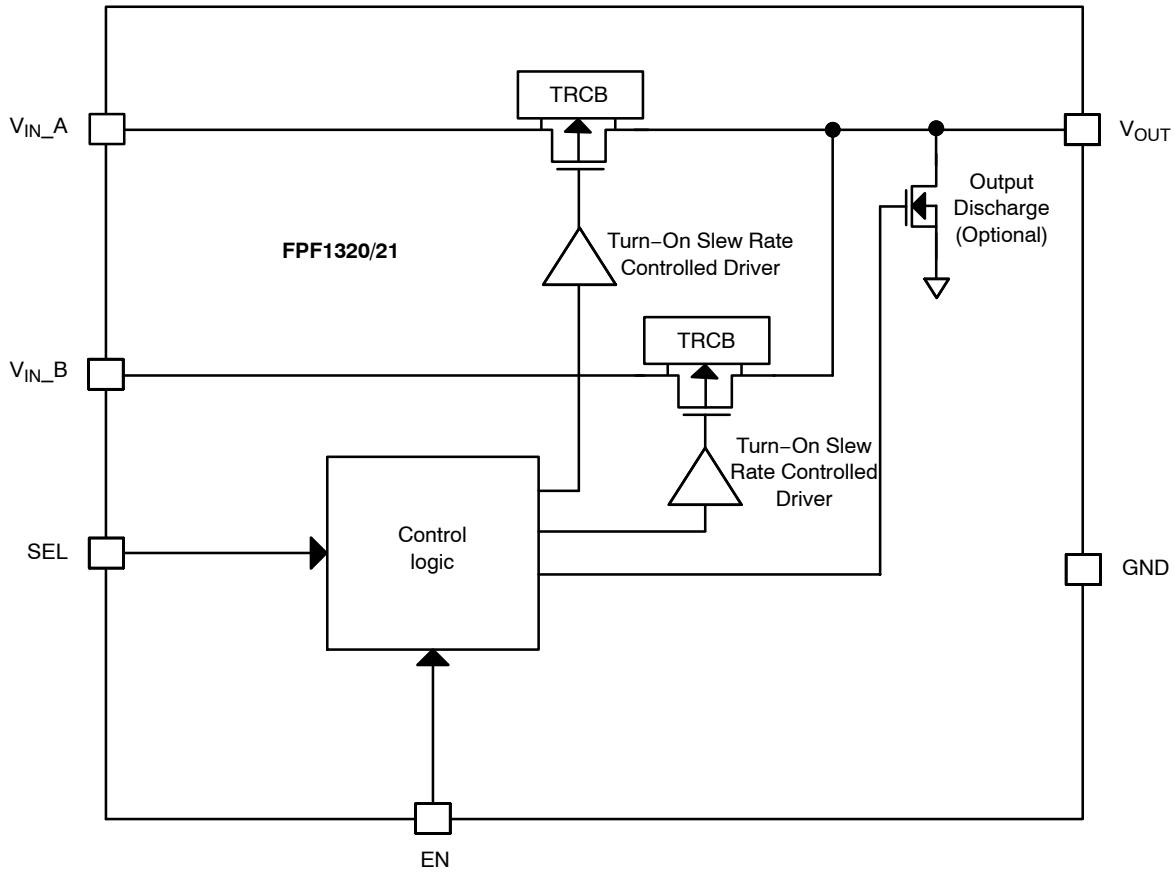


Figure 2. Functional Block Diagram (Output Discharge Path for FPF1321 Only)

Share Feedback
Your Opinion Matters

PIN CONFIGURATION

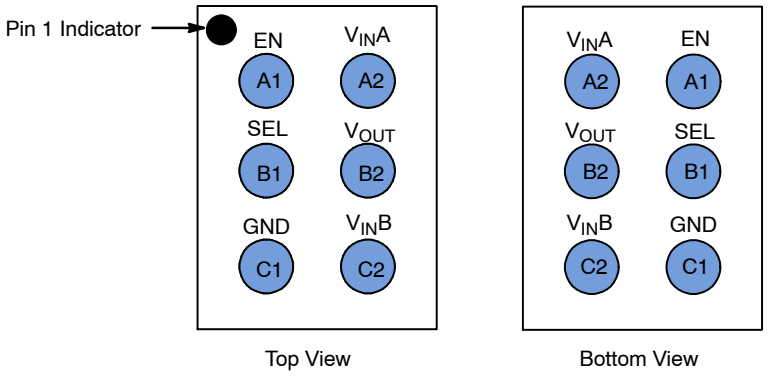


Figure 3. Pin Assignments

PIN DESCRIPTION

Pin #	Name	Description
A1	EN	Enable input. Active HIGH. There is an internal pull−down resistor at the EN pin.
B1	SEL	Input power selection inputs. See Truth Table. There are internal pull−down resistors at the SEL pins.
A2	$V_{IN}A$	Supply Input. Input to the power switch A.
B2	V_{OUT}	Switch output
C1	GND	Ground
C2	$V_{IN}B$	Supply Input. Input to power switch B.

TRUTH TABLE

SEL	EN	Switch A	Switch B	V_{OUT}	Status
Low	High	ON	OFF	$V_{IN}A$	$V_{IN}A$ Selected
High	High	OFF	ON	$V_{IN}B$	$V_{IN}B$ Selected
X	Low	OFF	OFF	Floating for FPF1320 GND for FPF1321	Both Switches are OFF

Share Feedback
Your Opinion Matters

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters		Min	Max	Unit
V_{IN}	$V_{IN}A$, $V_{IN}B$, V_{SEL}, V_{EN}, V_{OUT} to GND		−0.3	6	V
I_{SW}	Maximum Continuous Switch Current per Channel		–	1.5	A
P_D	Total Power Dissipation at T_A = 25°C		–	1.2	W
T_{STG}	Operating and Storage Junction Temperature		−65	150	°C
Θ_{JA}	Thermal Resistance, Junction−to−Ambient (1 in.^{2} Pad of 2−oz. Copper)		–	85 (Note 1)	°C/W
			–	110 (Note 2)	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114	6.0	–	kV
		Charged Device Model, JESD22−C101	1.5	–	
		Air Discharge ($V_{IN}A$, $V_{IN}B$ to GND), IEC61000−4−2 System Level	15.0	–	
		Contact Discharge ($V_{IN}A$, $V_{IN}B$ to GND), IEC61000−4−2 System Level	8.0	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Measured using 2S2P JEDEC std. PCB.
2. Measured using 2S2P JEDEC PCB cold−plate method.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameters	Min	Max	Unit
V_{IN}	Input Voltage on $V_{IN}A$, $V_{IN}B$	1.5	5.5	V
T_A	Ambient Operating Temperature	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V_{IN}A$ = $V_{IN}B$ = 1.5 to 5.5 V, T_A = −40 to 85°C unless otherwise noted. Typical values are at $V_{IN}A$ = $V_{IN}B$ = 3.3 V, T_A = 25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BASIC OPERATION						
$V_{IN}A$, $V_{IN}B$	Input Voltage	–	1.5	–	5.5	V
I_{SD}	Shutdown Current	SEL = HIGH or LOW, EN = GND, V_{OUT} = GND, $V_{IN}A$ = $V_{IN}B$ = 5.5 V	–	–	5	μA
I_Q	Quiescent Current	I_{OUT} = 0 mA, SEL = HIGH or LOW, EN = HIGH, $V_{IN}A$ = $V_{IN}B$ = 5.5 V	–	12	22	μA
R_{ON}	On−Resistance	$V_{IN}A$ = $V_{IN}B$ = 5.5 V, I_{OUT} = 200 mA, T_A = 25°C	–	42	60	mΩ
		$V_{IN}A$ = $V_{IN}B$ = 3.3 V, I_{OUT} = 200 mA, T_A = 25°C	–	50	–	
		$V_{IN}A$ = $V_{IN}B$ = 1.8 V, I_{OUT} = 200 mA, T_A = 25°C to 85°C	–	80	–	
		$V_{IN}A$ = $V_{IN}B$ = 1.5 V, I_{OUT} = 200 mA, T_A = 25°C	–	–	170	
V_{IH}	SEL, EN Input Logic High Voltage	$V_{IN}A$, $V_{IN}B$ = 1.5 V – 5.5 V	1.15	–	–	V
V_{IL}	SEL, EN Input Logic Low Voltage	$V_{IN}A$, $V_{IN}B$ = 1.8 V – 5.5 V	–	–	0.65	V
	SEL, EN Input Logic Low Voltage	$V_{IN}A$, $V_{IN}B$ = 1.5 V – 1.8 V	–	–	0.60	
V_{DROOP_OUT}	Output Voltage Droop while Channel Switching from Higher Input Voltage Lower Input Voltage (Note 3)	$V_{IN}A$ = 3.3 V, $V_{IN}B$ = 5 V, Switching from $V_{IN}A$ → $V_{IN}B$, R_L = 150 Ω, C_{OUT} = 1 μF	–	–	100	mV
I_{SEL}/I_{EN}	Input Leakage at SEL and EN Pin	–	–	–	1.2	μA

Share Feedback
Your Opinion Matters

ELECTRICAL CHARACTERISTICS $V_{IN}A$ = $V_{IN}B$ = 1.5 to 5.5 V, T_A = −40 to 85°C unless otherwise noted. Typical values are at $V_{IN}A$ = $V_{IN}B$ = 3.3 V, T_A = 25°C (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BASIC OPERATION (continued)						
R_{SEL_PD}/ R_{EN_PD}	Pull−Down Resistance at SEL or EN Pin	–	–	7	–	MΩ
R_{PD}	Output Pull−Down Resistance	SEL = HIGH or LOW, EN = GND, I_{FORCE} = 20 mA, T_A = 25°C, FPF1321	–	65	–	Ω
TRUE REVERSE CURRENT BLOCKING						
V_{T_RCB}	RCB Protection Trip Point	V_{OUT} − $V_{IN}A$ or $V_{IN}B$	–	45	–	mV
V_{R_RCB}	RCB Protection Release Trip Point	$V_{IN}A$ or $V_{IN}B$ −V_{OUT}	–	25	–	mV
I_{RCB}	$V_{IN}A$ or $V_{IN}B$ Current During RCB	V_{OUT} = 5.5 V, $V_{IN}A$ or $V_{IN}B$ = Short to GND	–	9	15	μA
t_{RCB_ON}	RCB Response Time w hen Device is ON (Note 3)	$V_{IN}A$ or $V_{IN}B$ = 5 V, $V_{OUT}V_{IN}A$,B = 100 mV	–	5	–	μs
DYNAMIC CHARACTERISTICS						
t_{DON}	Turn−On Delay (Note 4)	$V_{IN}A$ or $V_{IN}B$ = 3.3 V, R_L = 150 Ω, C_L = 1 μF, T_A = 25°C, SEL: HIGH, EN: LOW → HIGH	–	120	–	μs
t_R	V_{OUT} Rise Time (Note 4)		–	130	–	
t_{ON}	Turn−On Time (Note 6)		–	250	–	
t_{DOFF}	Turn−Off Delay (Note 4)	$V_{IN}A$ or $V_{IN}B$ = 3.3 V, R_L = 150 Ω, C_L = 1 μF, T_A = 25°C, SEL: HIGH, EN: HIGH→ LOW	–	15	–	μs
t_F	V_{OUT} Fall Time (Note 4)		–	320	–	
t_{OFF}	Turn−Off Time (Note 7)		–	335	–	
t_{DOFF}	Turn−Off Delay (Note 4, Note 5)	$V_{IN}A$ or $V_{IN}B$ = 3.3 V, R_L = 150 Ω, C_L = 1 μF, T_A = 25°C, SEL: HIGH, EN: HIGH→ LOW, Output Discharge Mode, FPF1321	–	6	–	μs
t_F	V_{OUT} Fall Time (Note 4, Note 5)		–	110	–	
t_{OFF}	Turn−Off Time (Note 5, Note 7)		–	116	–	
t_{TRANR}	Transition Time LOW → HIGH (Note 4)	$V_{IN}A$ = 3.3 V, $V_{IN}B$ = 5 V, Switching from $V_{IN}A$ → $V_{IN}B$, SEL: LOW → HIGH, EN: HIGH, R_L = 150 Ω, C_L = 1 μF, T_A = 25°C	–	3	–	μs
t_{SLH}	Switch−Over Rising Delay (Note 4)		–	1	–	
t_{TRANF}	Transition Time HIGH → LOW (Note 4)	$V_{IN}A$ = 3.3 V, $V_{IN}B$ = 5 V, Switching from $V_{IN}B$ → $V_{IN}A$, SEL: HIGH → LOW, EN: HIGH, R_L = 150 Ω, C = 1 μF, T_A = 25°C	–	45	–	μs
t_{SHL}	Switch−Over Falling Delay (Note 4)		–	5	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. This parameter is guaranteed by design and characterization; not production tested.
4. t_{DON}/t_{DOFF}/t_R/t_F/t_{TRANR}/t_{TRANF}/t_{SLH}/t_{SHL} are defined in Figure 4.
5. FPF1321 output discharge is enabled during off.
6. t_{ON} = t_R + t_{DON}
7. t_{OFF} = t_F + t_{DOFF}

Share Feedback
Your Opinion Matters

TIMING DIAGRAM

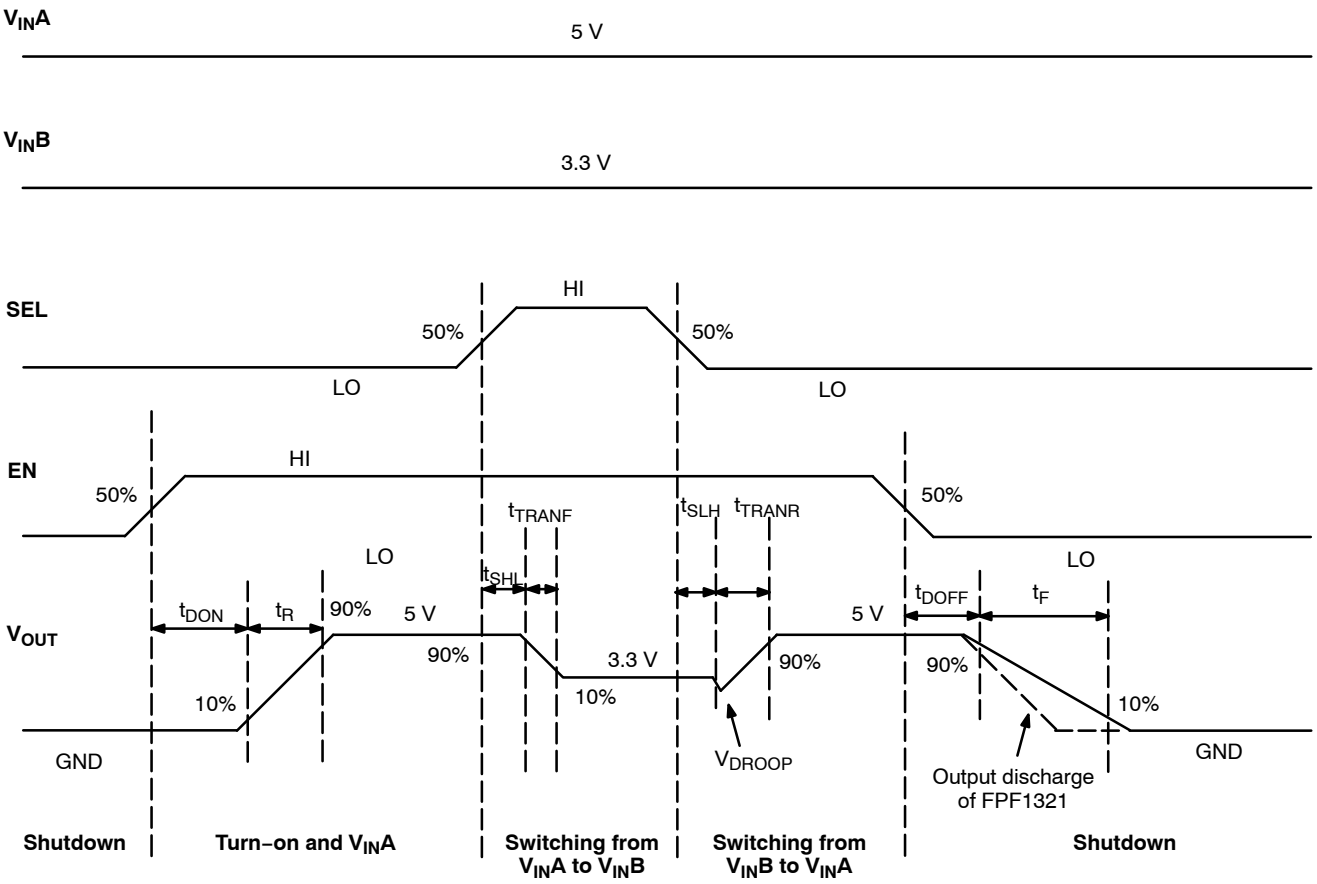


Figure 4. Dynamic Behavior Timing Diagram

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS

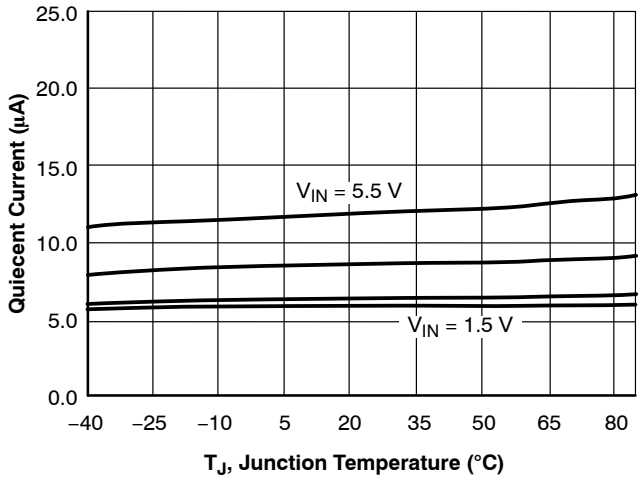


Figure 5. Supply Current vs. Temperature

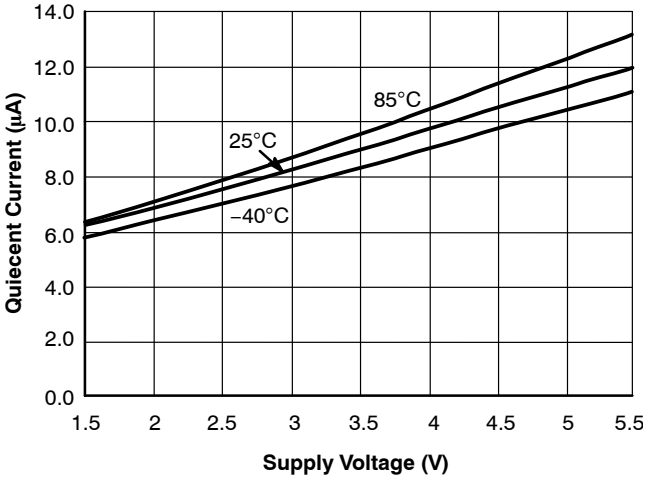


Figure 6. Supply Current vs. Supply Voltage

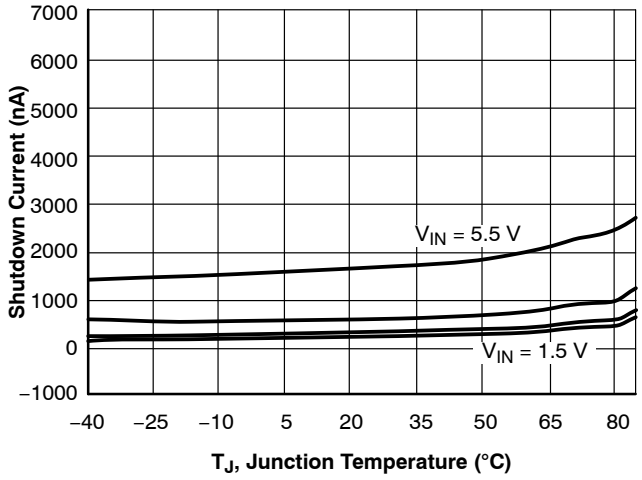


Figure 7. Shutdown Current vs. Temperature

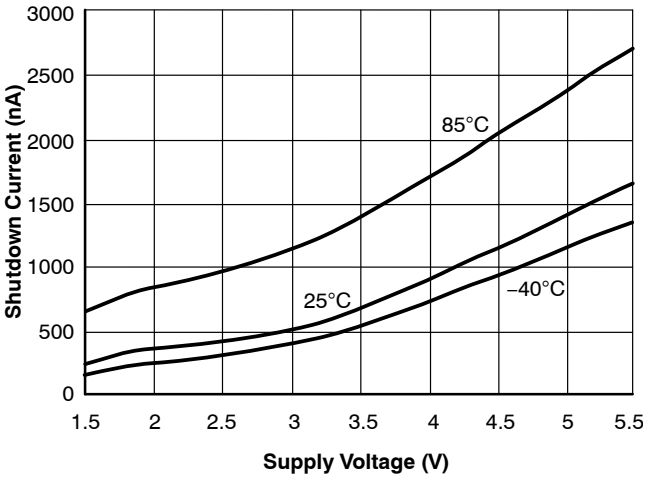


Figure 8. Shutdown Current vs. Supply Voltage

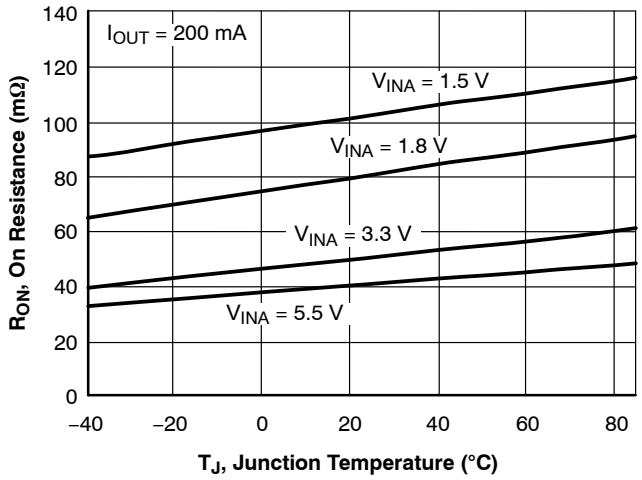


Figure 9. R_{ON} vs. Temperature

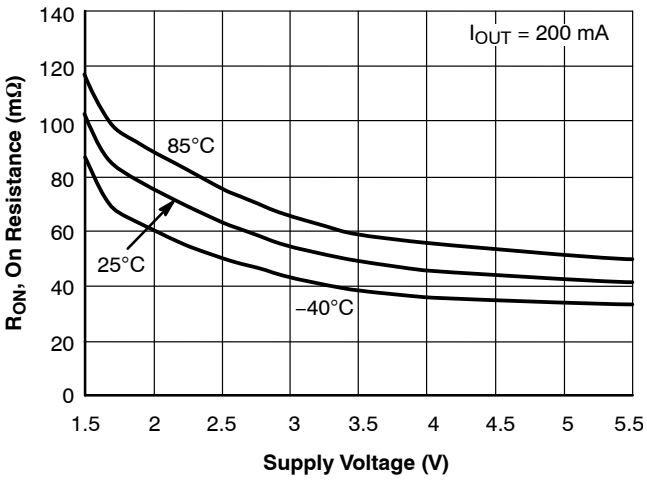


Figure 10. R_{ON} vs. Supply Voltage

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS (CONTINUED)

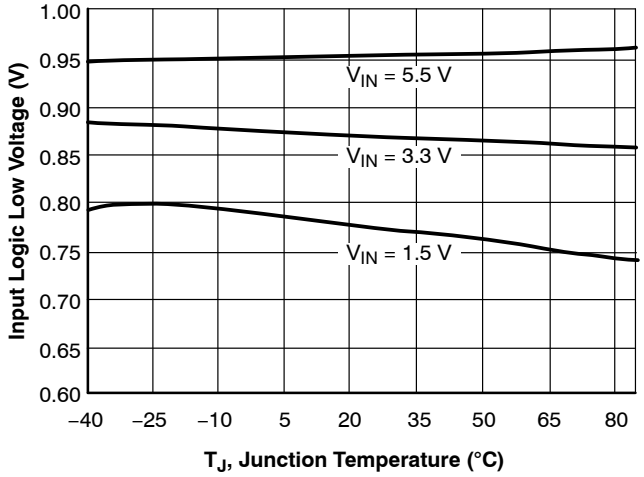


Figure 11. V_{IL} vs. Temperature

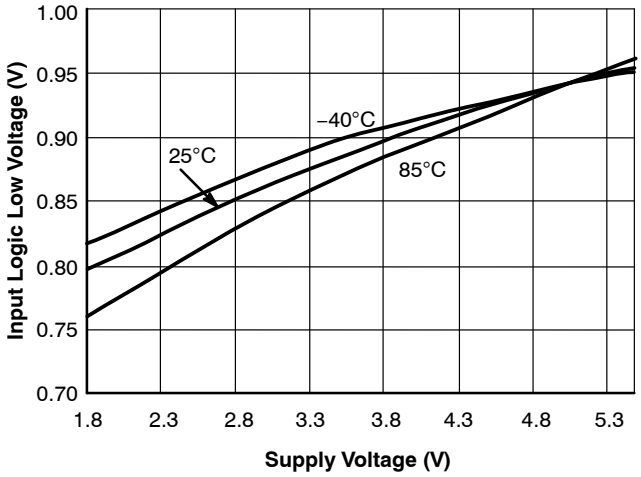


Figure 12. V_{IL} vs. Supply Voltage

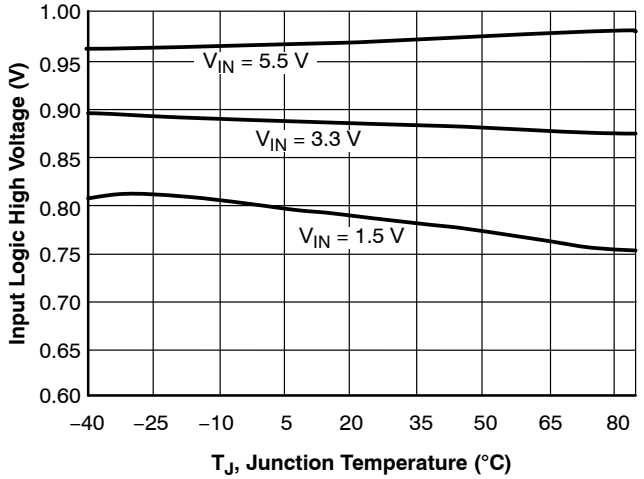


Figure 13. V_{IH} vs. Temperature

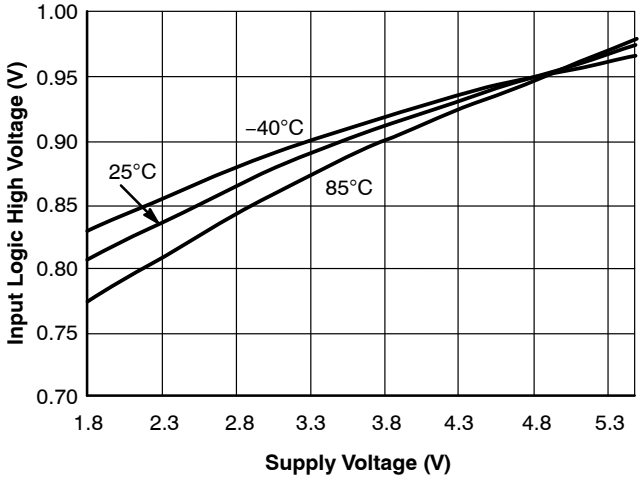


Figure 14. V_{IH} vs. Supply Voltage

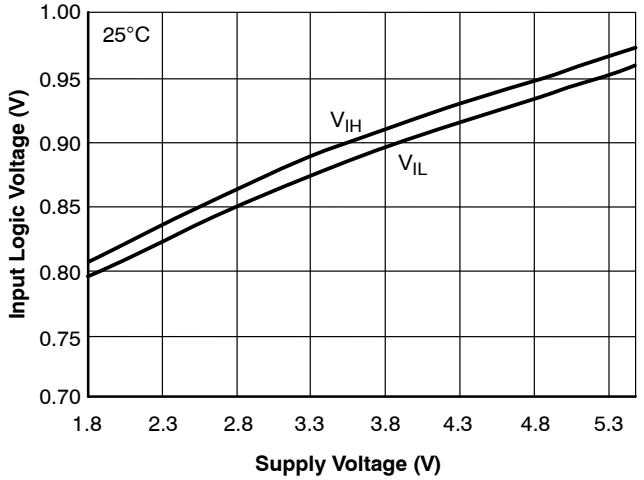


Figure 15. V_{IH}/V_{IL} vs. Supply Voltage

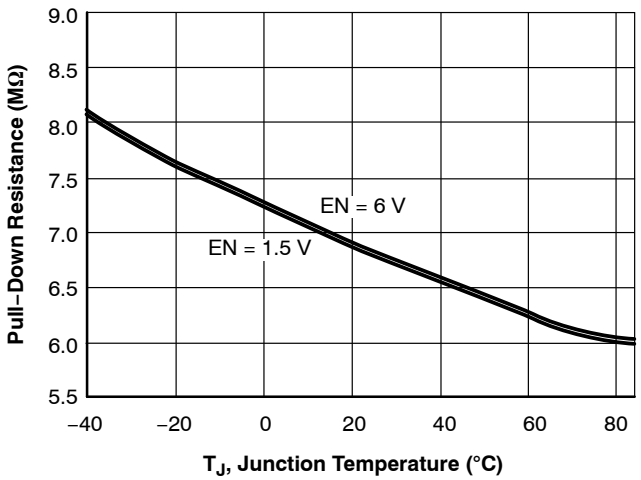


Figure 16. R_{SEL_PD} and R_{EN_PD} vs. Temperature

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS (CONTINUED)

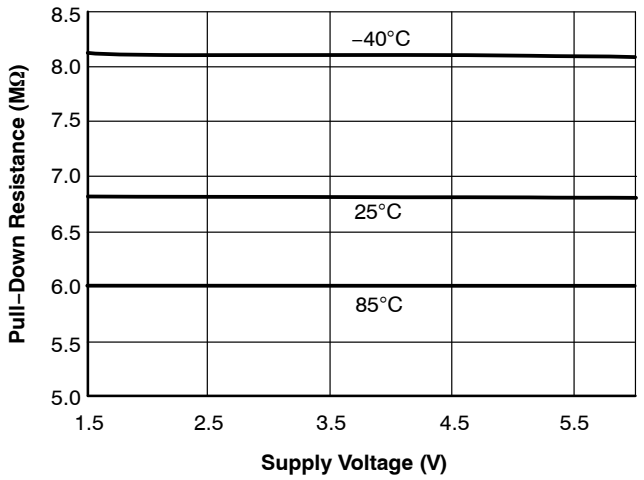


Figure 17. R_{SEL_PD} and R_{EN_PD} vs. Supply Voltage

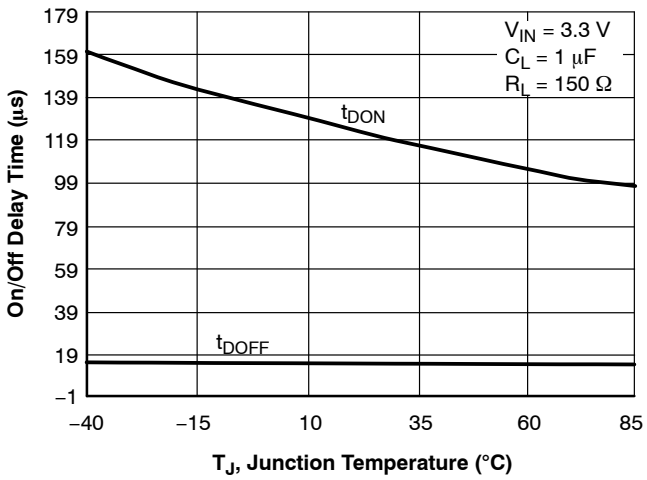


Figure 18. t_{DON} and t_{DOFF} vs. Temperature

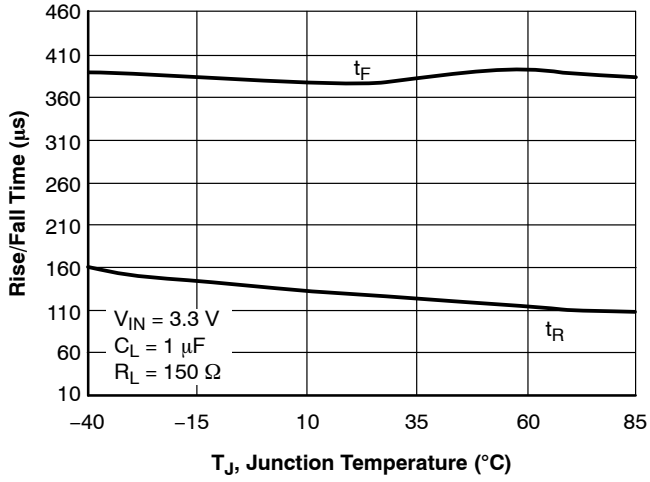


Figure 19. t_R and t_F with FPF1320 vs. Temperature

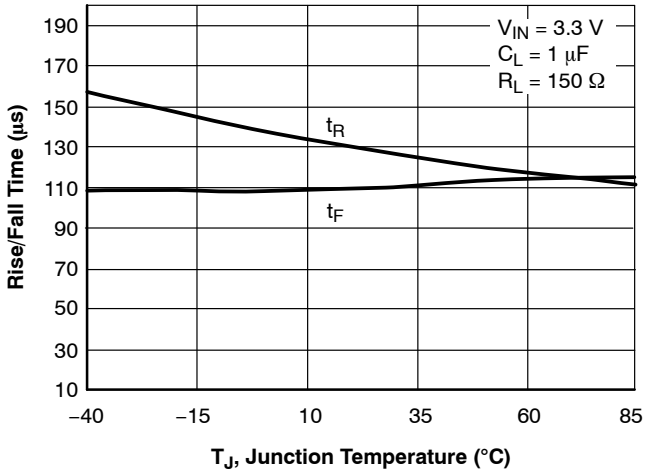


Figure 20. t_R and t_F with FPF1321 vs. Temperature

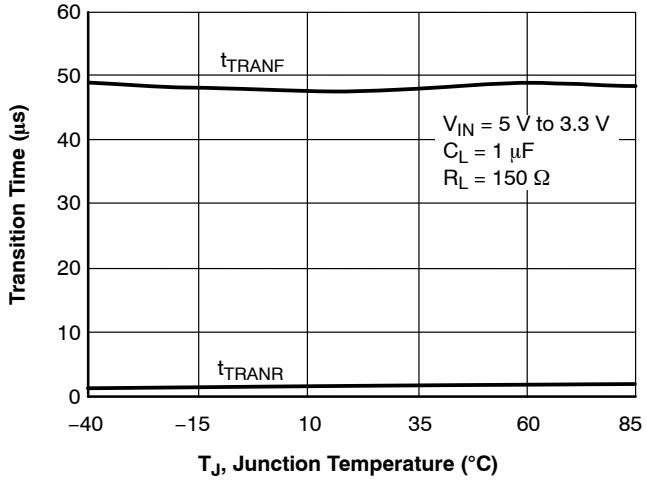


Figure 21. Transition Time vs. Temperature

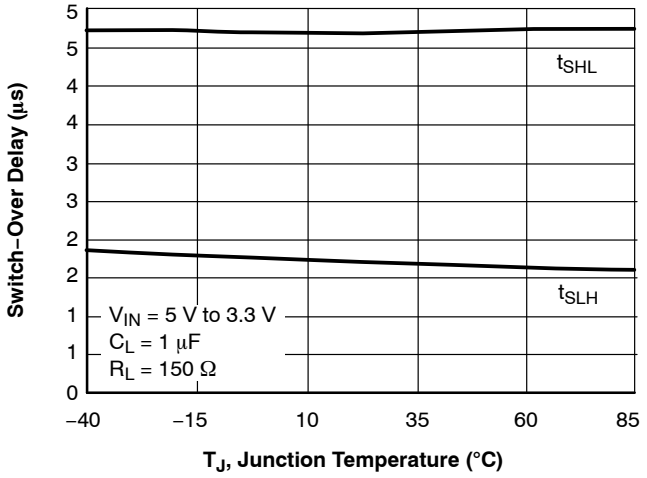


Figure 22. Switch Over Time vs. Temperature

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS (CONTINUED)

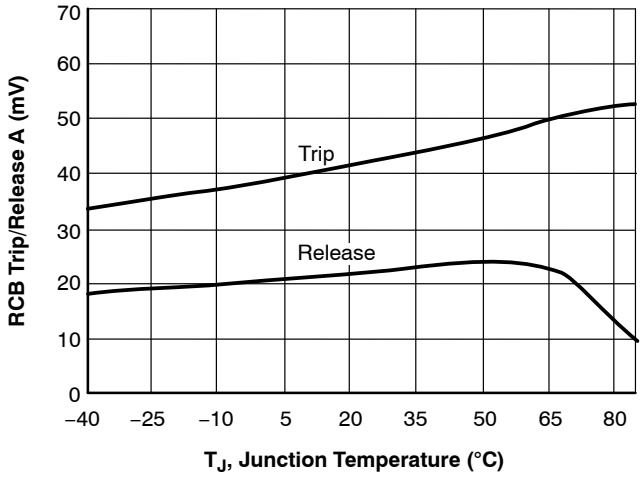


Figure 23. TRCB Trip and Release vs. Temperature

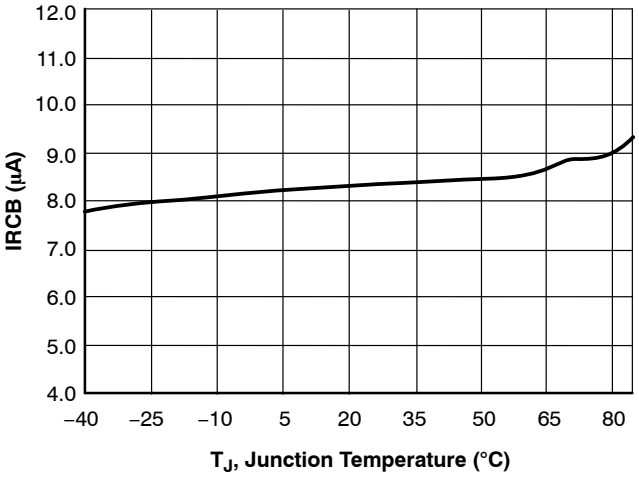


Figure 24. I_{RCB} vs. Temperature

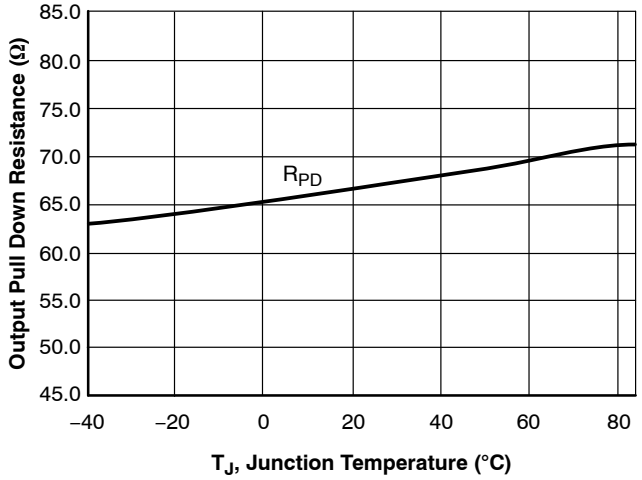


Figure 25. R_{PD} with FPF1321 vs. Temperature

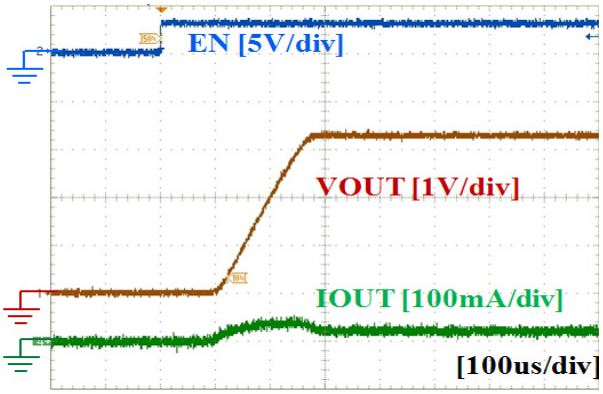


Figure 26. Turn−On Response
(V_{IN}A = 3.3 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, R_L = 150 Ω, SEL = LOW)

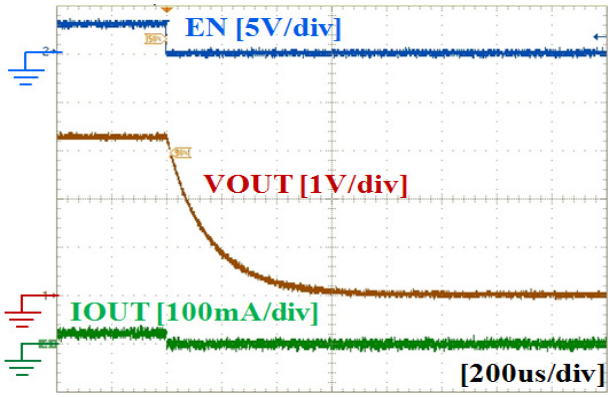


Figure 27. Turn−Off Response with FPF1320
(V_{IN}A = 3.3 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, R_L = 150 Ω, SEL = LOW)

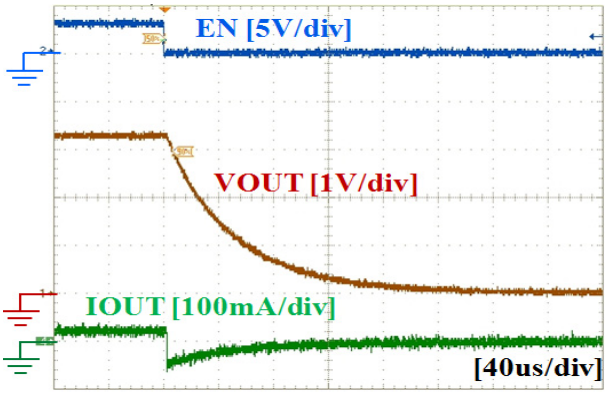


Figure 28. Turn−Off Response with FPF1321
(V_{IN}A = 3.3 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, R_L = 150 Ω, SEL = LOW)

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS (CONTINUED)

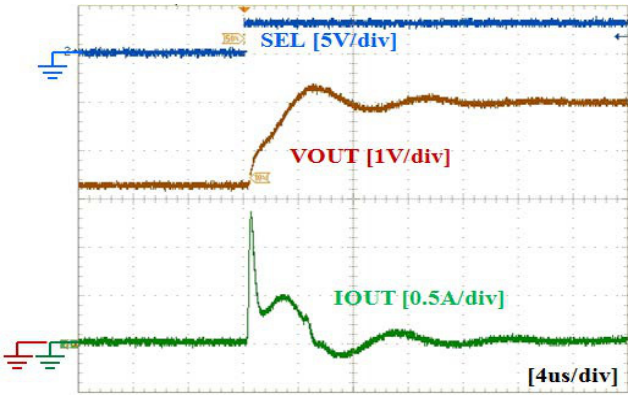


Figure 29. Power Source Transition from 3.3 V to 5 V (V_{IN}A = 3.3 V, V_{IN}B = 5 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, R_L = 150 Ω)

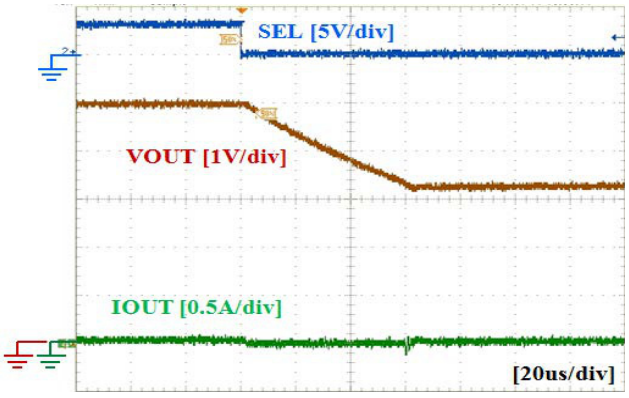


Figure 30. Power Source Transition from 5 V to 3.3 V (V_{IN}A = 3.3 V, V_{IN}B = 5 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, R_L = 150 Ω)

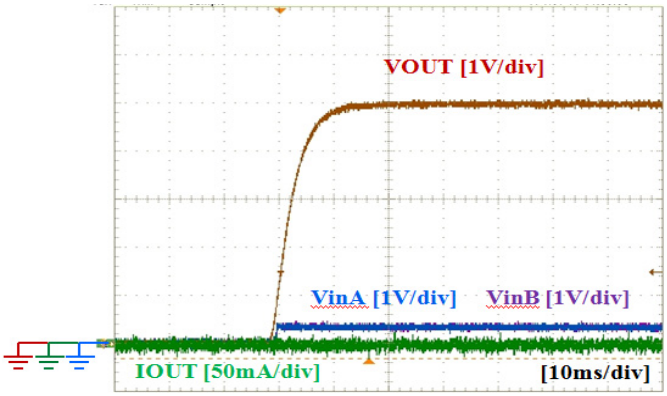


Figure 31. TRCB During Off (V_{IN}A = V_{IN}B = Floating, V_{OUT} = 5 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, EN = LOW, No R_L)

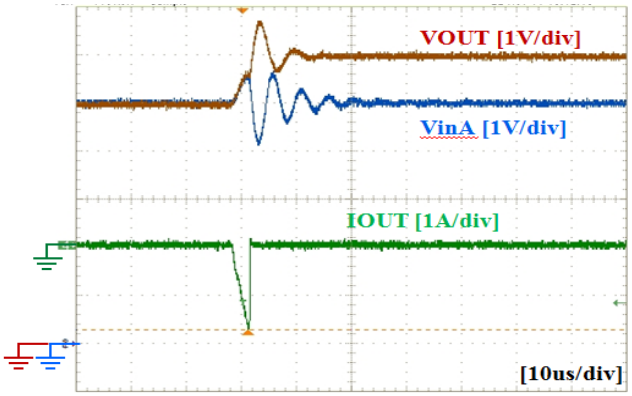


Figure 32. TRCB During On (V_{IN}A = 5 V, V_{OUT} = 6 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, EN = HIGH, No R_L)

OPERATION AND APPLICATION DESCRIPTION

The FPF1320 and FPF1321 are dual−input single−output power multiplexer switches with controlled turn−on and seamless power source transition. The core is a 50 mΩ P−channel MOSFET and controller capable of functioning over a wide input operating range of 1.5 V to 5.5 V per channel. The EN and SEL pins are active−HIGH, GPIO/CMOS−compatible input. They control the state of the switch and input power source selection, respectively. TRCB functionality blocks unwanted reverse current during both ON and OFF states when higher V_{OUT} than V_{IN}A or V_{IN}B is applied. FPF1321 has a 65 Ω output discharge path during off.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor; a capacitor must be placed between the V_{IN}A or V_{IN}B pins to the GND pin. At least 1 μF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher−value C_{IN} can be used to reduce more the voltage drop.

Inrush Current

Inrush current occurs when the device is turned on. Inrush current is dependent on output capacitance and slew rate control capability, as expressed by:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN} - V_{INITIAL}}{t_R} + I_{LOAD} \qquad \text{(eq. 1)}$$

Share Feedback
Your Opinion Matters

where:

C_{OUT}: Output capacitance;
t_R: Slew rate or rise time at V_{OUT};
V_{IN}: Input voltage, $V_{IN}A$ or $V_{IN}B$;
$V_{INITIAL}$: Initial voltage at C_{OUT}, usually GND; and
I_{LOAD}: Load current.

Higher inrush current causes higher input voltage drop, depending on the distributed input resistance and input capacitance. High inrush current can cause problems.

FPF1320/1 has a 130 μs of slew rate capability under 3.3 V_{IN} at 1 μF of C_{OUT} and 150 Ω of R_L so inrush current and input voltage drop can be minimized.

Power Source Selection

Input power source selection can be controlled by the SEL pin. When SEL is LOW, output is powered from $V_{IN}A$ while SEL is HIGH, $V_{IN}B$ is powering output. The SEL signal is ignored during device OFF.

Output Voltage Drop During Transition

Output voltage drop usually occurs during input power source transition period from low voltage to high voltage. The drop is highly dependent on output capacitance and load current.

FPF1320/1 adopts an advanced break−before−make control, which can result in minimized output voltage drop during the transition time.

Output Capacitor

Capacitor C_{OUT} of at least 1 μF is highly recommended between the V_{OUT} and GND pins to achieve minimized output voltage drop during input power source transition. This capacitor also prevents parasitic board inductance.

True Reverse−Current Blocking

The true reverse−current blocking feature protects the input source against current flow from output to input regardless of whether the load switch is on or off.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance on normal and short−circuit operation. Wide traces or large copper planes for power pins ($V_{IN}A$, $V_{IN}B$, V_{OUT} and GND) minimize the parasitic electrical effects and the thermal impedance.

ORDERING INFORMATION

Part Number	Top Mark	Channel	Switch Per Channel (Typ.) at 3.3 V_{IN}	Reverse Current Blocking	Output Discharge	Rise Time (t_R)	Package
FPF1320UCX	QS	DISO	50 mΩ	Yes	NA	130 μs	1.0 mm × 1.5 mm Wafer−Level Chip−Scale Package (WLCSP) 6−Bumps, 0.5 mm Pitch
FPF1321UCX	QT	DISO	50 mΩ	Yes	65 Ω	130 μs	

DISCONTINUED (Note 8)

FPF1321BUCX	QT	DISO	50 mΩ	Yes	65 Ω	130 μs	1.0 mm × 1.5 mm Wafer−Level Chip−Scale Package (WLCSP) 6−Bumps, 0.5 mm Pitch with Backside Laminate

8. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

PRODUCT−SPECIFIC DIMENSIONS

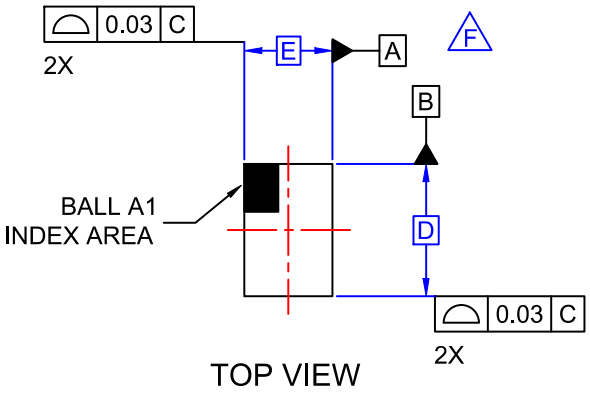
Product	D	E	X	Y
FPF1320UCX	1460 μm ± 30 μm	960 μm ± 30 μm	230 μm	230 μm
FPF1321UCX	1460 μm ± 30 μm	960 μm ± 30 μm	230 μm	230 μm
FPF1321BUCX	1460 μm ± 30 μm	960 μm ± 30 μm	230 μm	230 μm

IntelliMAX is a trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

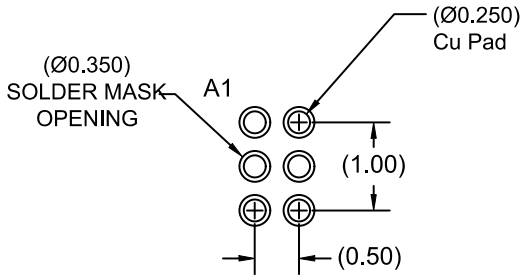
Share Feedback
Your Opinion Matters

WLCSP6 1.46x0.96x0.582
CASE 567RM
ISSUE O

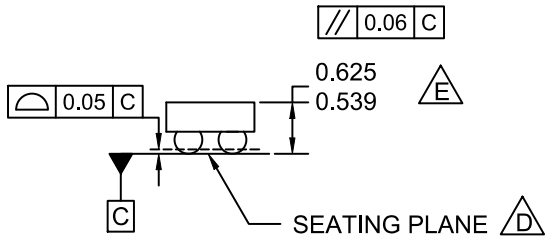
DATE 30 NOV 2016

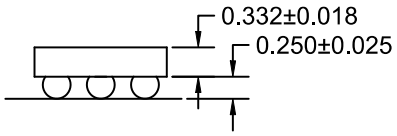


TOP VIEW

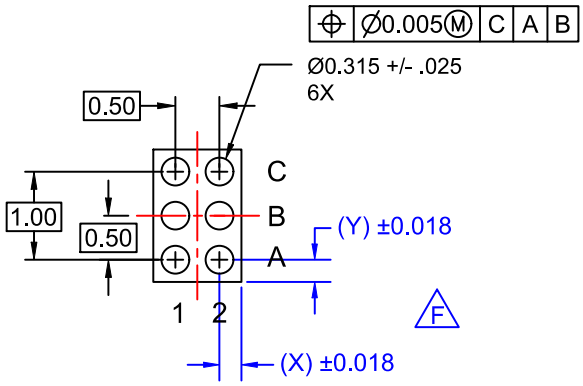


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

DOCUMENT NUMBER:	**98AON16579G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**WLCSP6 1.46x0.96x0.582**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales