High Performance Resonant Mode Controller featuring High-Voltage Drivers

NCP1396A, NCP1396B

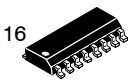
The NCP1396 A/B offers everything needed to build a reliable and rugged resonant mode power supply. Its unique architecture includes a 500 kHz Voltage Controlled Oscillator whose control mode brings flexibility when an ORing function is a necessity, e.g. in multiple feedback paths implementations. Thanks to its proprietary high−voltage technology, the controller welcomes a bootstrapped MOSFET driver for half−bridge applications accepting bulk voltages up to 600 V. Protections featuring various reaction times, e.g. immediate shutdown or timer−based event, brown−out, broken opto−coupler detection etc., contribute to a safer converter design, without engendering additional circuitry complexity. An adjustable deadtime also helps lowering the shoot−through current contribution as the switching frequency increases.

Features

- High−frequency Operation from 50 kHz up to 500 kHz
- 600 V High−Voltage Floating Driver
- Selectable Minimum Switching Frequency with ±3% Accuracy
- Adjustable Deadtime from 100 ns to 2 μs.
- Startup Sequence via an Adjustable Soft−start
- Brown−out Protection for a Simpler PFC Association
- Latched Input for Severe Fault Conditions, e.g. Over Temperature or OVP
- Timer−based Input with Auto−recovery Operation for Delayed Event Reaction
- Enable Input for Immediate Event Reaction or Simple ON/OFF Control
- V_{CC} Operation up to 20 V
- Low Startup Current of 300 μA
- 1 A / 0.5 A Peak Current Sink / Source Drive Capability
- Common Collector Optocoupler Connection for Easier ORing
- Internal Temperature Shutdown
- B Version features 10 V V_{CC} Startup Threshold
- These are Pb−Free Devices

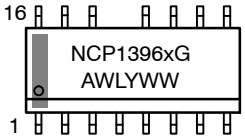
Typical Applications

- Flat Panel Display Power Converters
- High Power AC/DC Adapters for Notebooks
- Industrial and Medical Power Sources
- Offline Battery Chargers



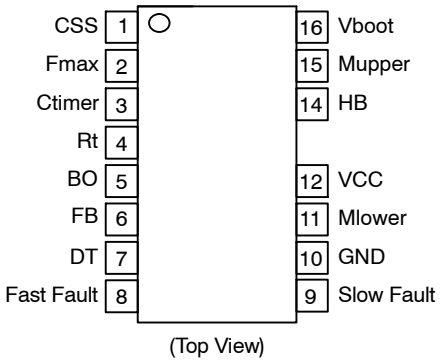
SO−16, LESS PIN 13
D SUFFIX
CASE 751AM

MARKING DIAGRAMS



x	= A or B
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

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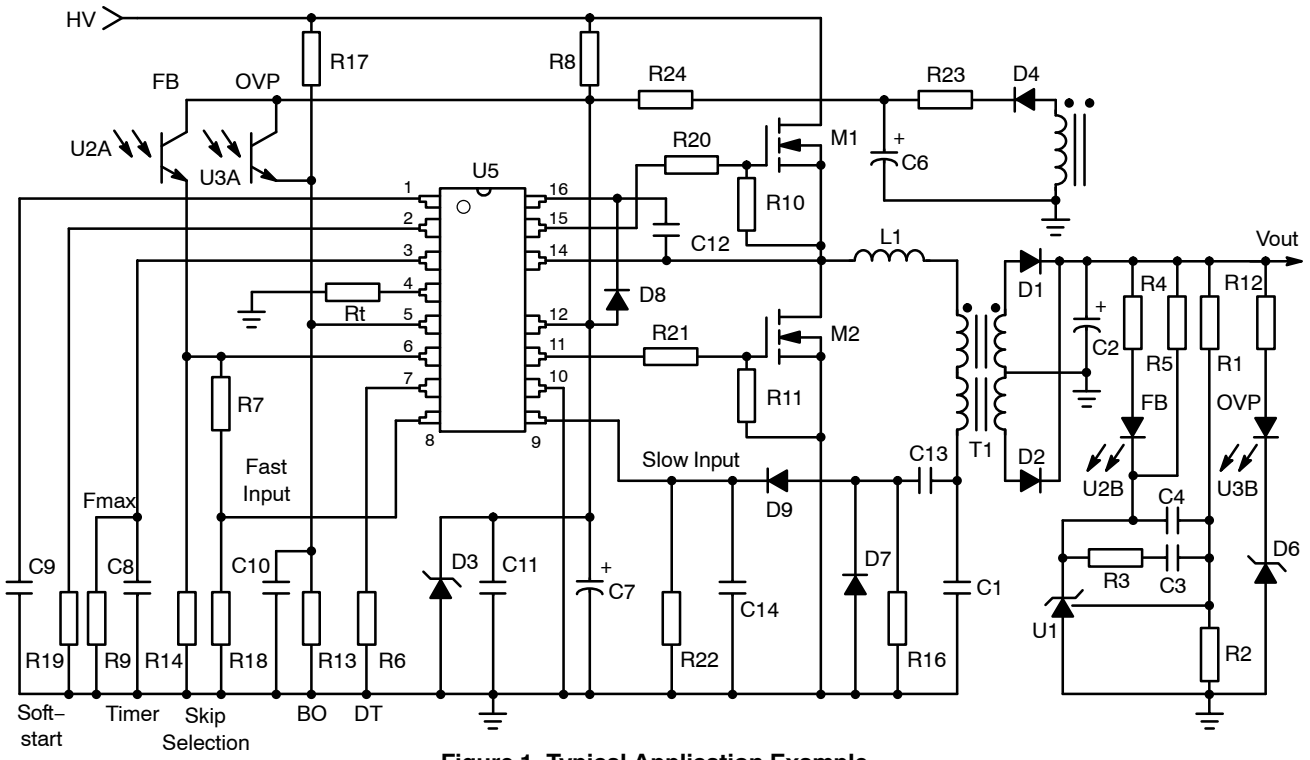


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	CSS	Soft−start	Select the soft−start duration
2	Fmax	Frequency clamp	A resistor sets the maximum frequency excursion
3	Ctimer	Timer duration	Sets the timer duration in presence of a fault
4	Rt	Timing resistor	Connecting a resistor to this pin, sets the minimum oscillator frequency reached for VFB = 1 V
5	BO	Brown−Out	Detects low input voltage conditions. When brought above Vlatch, it fully latches off the controller.
6	FB	Feedback	Injecting current in this pin increases the oscillation frequency up to Fmax.
7	DT	Dead−time	A simple resistor adjusts the dead−time width
8	Fast Fault	Quick fault detection	Fast shut−down pin. Upon release, a clean startup sequence occurs. Can be used for skip cycle purposes.
9	Slow Fault	Slow fault detection	When asserted, the timer starts to countdown and shuts down the controller at the end of its time duration.
10	GND	Analog ground	−
11	Mlower	Low side output	Drives the lower side MOSFET
12	V_{CC}	Supplies the controller	The controller accepts up to 20 V
13	−	−	−
14	HB	Half−bridge connection	Connects to the half−bridge output
15	Mupper	High side output	Drives the higher side MOSFET
16	Vboot	Bootstrap pin	The floating V_{CC} supply for the upper stage

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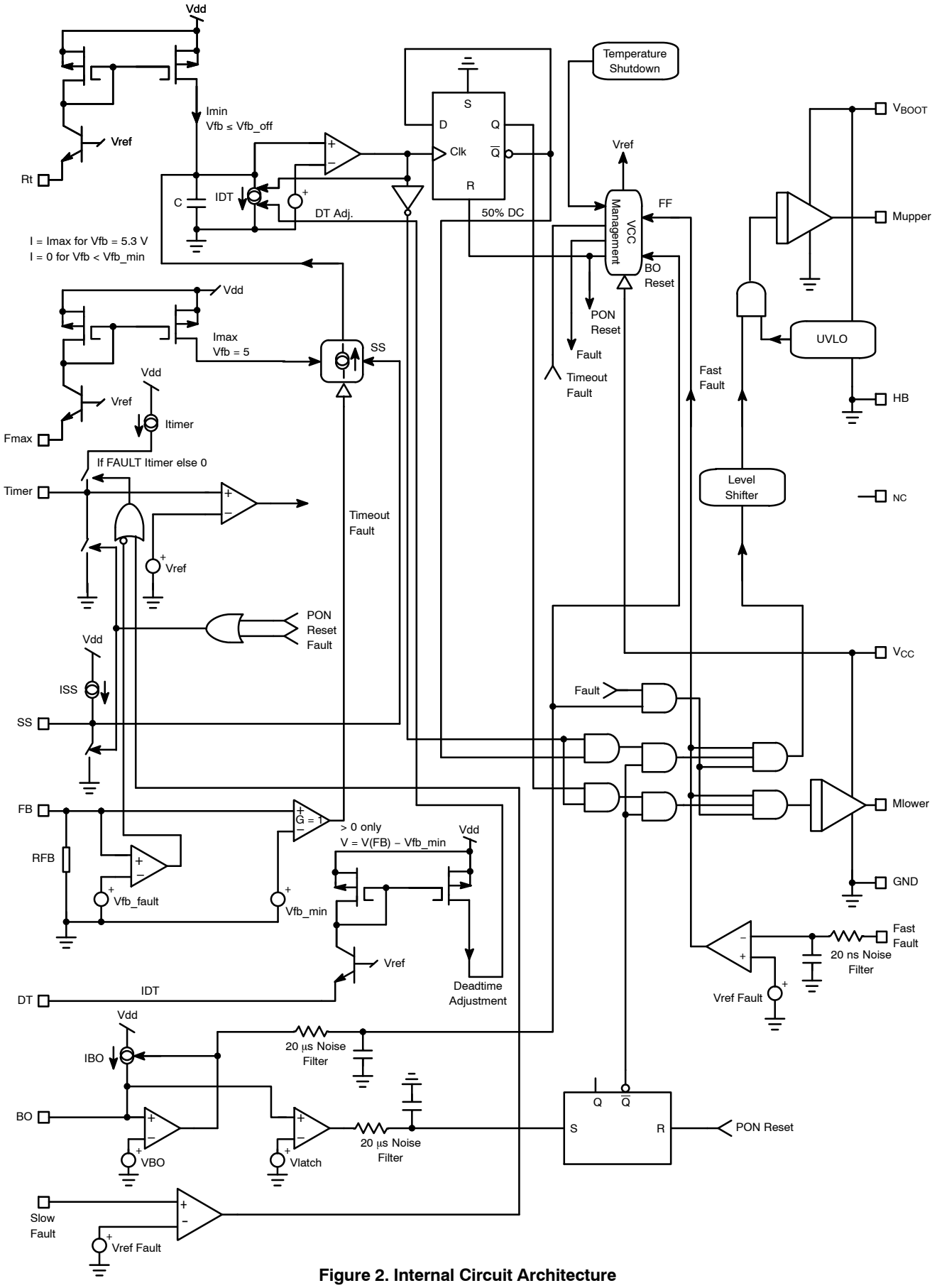


Figure 2. Internal Circuit Architecture

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage bridge pin, pin 14	VBRIDGE	−1 to 600	V
Floating supply voltage	VBOOT− VBRIDGE	0 to 20	V
High side output voltage	VDRV_HI	VBRIDGE−0.3 to VBOOT+0.3	V
Low side output voltage	VDRV_LO	−0.3 to V_{CC} + 0.3	V
Allowable output slew rate	dVBRIDGE/dt	50	V/ns
Power Supply voltage, pin 12	V_{CC}	20	V
Maximum voltage, all pins (except pin 11 and 10)	−	−0.3 to 10	V
Thermal Resistance − Junction−to−Air, SOIC version	$R_{\theta JA}$	130	°C/W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{JMAX}	+150	°C
Storage Temperature Range	T_{STG}	−60 to +150	°C
ESD Capability, Human Body Model (All pins except HV Pins)	−	2	kV
ESD Capability, Machine Model	−	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000V per JESD22−A114−B
   Machine Model Method 200V per JESD22−A115−A.
2. This device meets latch−up tests defined by JEDEC Standard JESD78.

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ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION						
Turn−on threshold level, V_{CC} going up − A version	12	VCC_{ON}	12.3	13.4	14.3	V
Turn−on threshold level, V_{CC} going up − B version	12	VCC_{ON}	9.5	10.5	11.5	V
Minimum operating voltage after turn−on	12	$VCC_{(min)}$	8.5	9.5	10.5	V
Startup voltage on the floating section	16−14	$Vboot_{ON}$	8	9	10	V
Cutoff voltage on the floating section	16−14	$Vboot_{(min)}$	7.4	8.4	9.4	V
Startup current, V_{CC} < VCC_{ON} 0°C < T_J < +125°C −40°C < T_J < +125°C	12	Istartup	− −	− −	300 350	μA
V_{CC} level at which the internal logic gets reset	12	VCC_{reset}	−	6.5	−	V
Internal IC consumption, no output load on pin 15/14 − 11/10, Fsw = 300 kHz	12	ICC1	−	4	−	mA
Internal IC consumption, 1 nF output load on pin 15/14 − 11/10, Fsw = 300 kHz	12	ICC2	−	11	−	mA
Consumption in fault mode (All drivers disabled, V_{CC} > $V_{CC(min)}$)	12	ICC3	−	1.2	−	mA
VOLTAGE CONTROL OSCILLATOR (VCO)						
Characteristic	**Pin**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Minimum switching frequency, Rt = 18 kΩ on pin 4, Vpin 6 = 0.8 V, DT = 300 ns	4	Fsw min	58.2	60	61.8	kHz
Maximum switching frequency, Rfmax = 1.3 kΩ on pin 2, Vpin 6 > 5.3 V, Rt = 18 kΩ, DT = 300 ns	2	Fsw max	425	500	575	kHz
Feedback pin swing above which Δf = 0	6	FBSW	−	5.3	−	V
Operating duty−cycle symmetry	11−15	DC	48	50	52	%
Delay before any driver re−start in fault mode	−	Tdel	−	20	−	μs
FEEDBACK SECTION						
Characteristic	**Pin**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Internal pull−down resistor	6	Rfb	−	20	−	kΩ
Voltage on pin 6 below which the FB level has no VCO action	6	Vfb_min	−	1.2	−	V
Voltage on pin 6 below which the controller considers a fault	6	Vfb_off	−	0.6	−	V
DRIVE OUTPUT						
Characteristic	**Pin**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output voltage rise−time @ CL = 1 nF, 10−90% of output signal	15−14/ 11−10	T_r	−	40	−	ns
Output voltage fall−time @ CL = 1 nF, 10−90% of output signal	15−14/ 11−10	T_f	−	20	−	ns
Source resistance	15−14/ 11−10	R_{OH}	−	13	−	Ω
Sink resistance	15−14/ 11−10	R_{OL}	−	5.5	−	Ω
Dead time with R_{DT} = 10 kΩ from pin 7 to GND	7	T_dead	250	300	340	ns
Maximum dead−time with R_{DT} = 82 kΩ from pin 7 to GND	7	T_dead−max	−	2	−	μs
Minimum dead−time, R_{DT} = 3 kΩ from pin 7 to GND	7	T_dead−min	−	100	−	ns
Leakage current on high voltage pins to GND	14, 15,16	IHV_LEAK	−	−	5	μA

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ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, unless otherwise noted.)

TIMERS

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Timer charge current	3	Itimer	–	160	–	μA
Timer duration with a 1 μF capacitor and a 1 MΩ resistor	3	T−timer	–	25	–	ms
Timer recurrence in permanent fault, same values as above	3	T−timerR	–	1.4	–	s
Voltage at which pin 3 stops output pulses	3	VtimerON	3.5	4	4.4	V
Voltage at which pin 3 re−starts output pulses	3	VtimerOFF	0.9	1	1.1	V
Soft−start ending voltage	1	VSS	–	2	–	V
Soft−start charge current 0°C < T_J < +125°C −40°C < T_J < +125°C	1	ISS	80 75	110 110	125 130	μA
Soft−start duration with a 100 nF capacitor (Note 3)	1	T−SS	–	1.8	–	ms

PROTECTION

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Reference voltage for fast input (Note 4)	8−9	VrefFaultF	1.00	1.05	1.10	V
Hysteresis for fast input (Note 4)	8−9	HysteFaultF	–	80	–	mV
Reference voltage for slow input 0°C < T_J < +125°C −40°C < T_J < +125°C	8−9	VrefFaultS	0.95 0.92	1.00 1.00	1.05 1.05	V
Hysteresis for slow input	8−9	HysteFaultS	–	60	–	mV
Propagation delay for fast fault input drive shutdown	8	TpFault	–	55	90	ns
Brown−Out input bias current	5	IBObias	–	0.02	–	μA
Brown−Out level (Note 4)	5	VBO	0.99	1.04	1.09	V
Hysteresis current, Vpin5 > VBO − A version 0°C < T_J < +125°C −40°C < T_J < +125°C	5	IBO_A	21.5 19	26.5 26.5	31.5 33	μA
Hysteresis current, Vpin5 > VBO − B version 0°C < T_J < +125°C −40°C < T_J < +125°C	5	IBO_B	86 80	106 106	126 132	μA
Latching voltage	5	Vlatch	3.6	4	4.4	V
Temperature shutdown	–	TSD	140	–	–	°C
Hysteresis	–	TSDhyste	–	30	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. The A version does not activate soft−start (unless the feedback pin voltage is below 0.6 V) when the fast−fault is released, this is for skip cycle implementation. The B version does activate the soft−start upon release of the fast−fault input for any feedback conditions.
4. Guaranteed by design

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TYPICAL CHARACTERISTICS – A VERSION

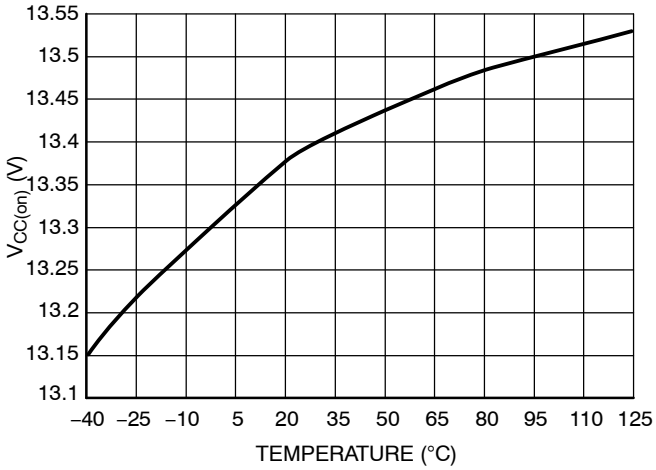


Figure 3. $V_{CC(on)}$

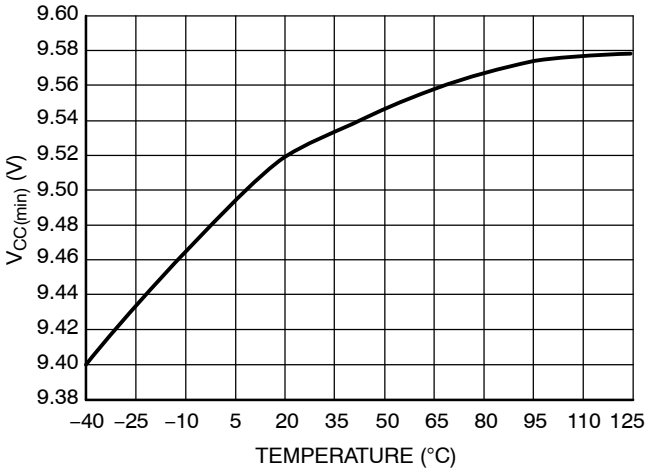


Figure 4. $V_{CC(min)}$

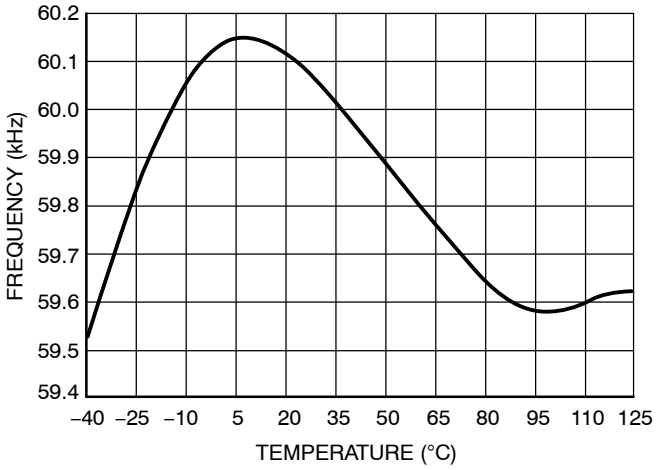


Figure 5. Fsw min

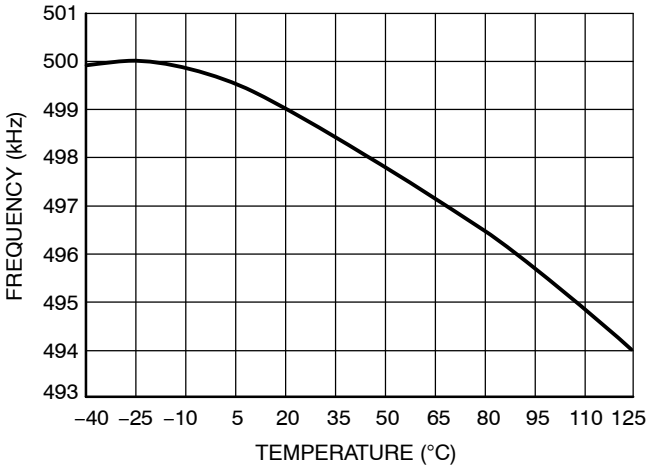


Figure 6. Fsw max

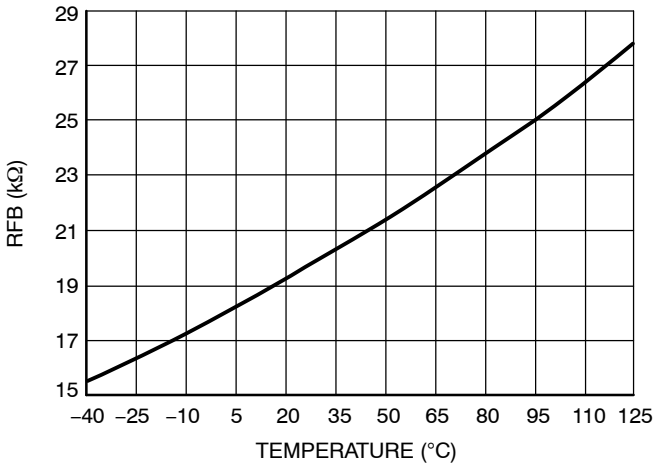


Figure 7. Pulldown Resistor (RFB)

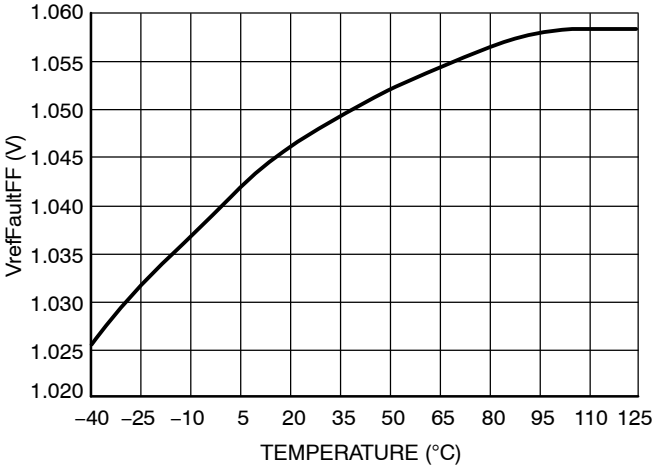


Figure 8. Fast Fault (VrefFaultF)

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TYPICAL CHARACTERISTICS – A VERSION

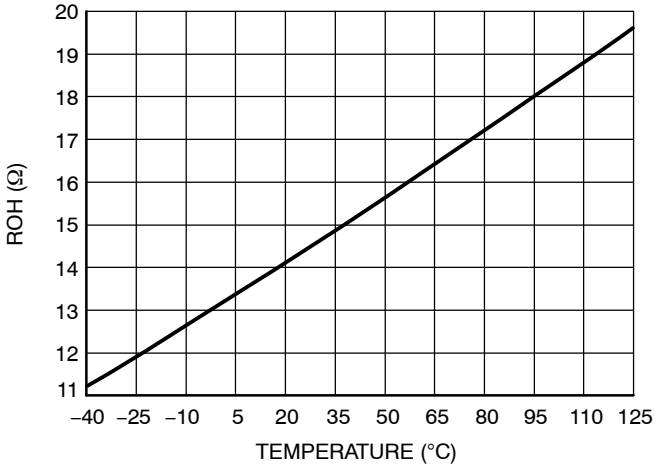


Figure 9. Source Resistance (ROH)

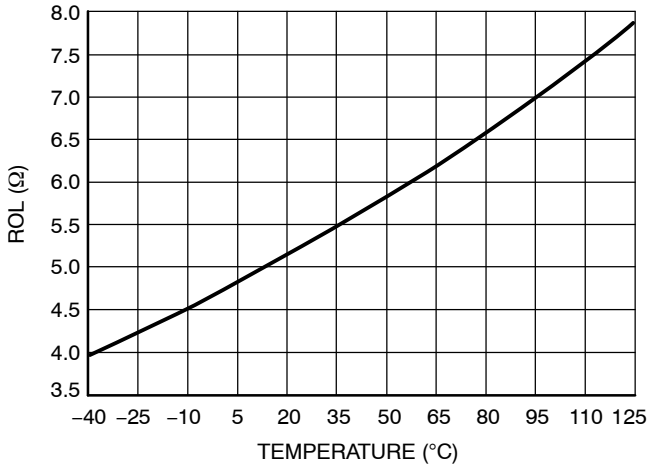


Figure 10. Sink Resistance (ROL)

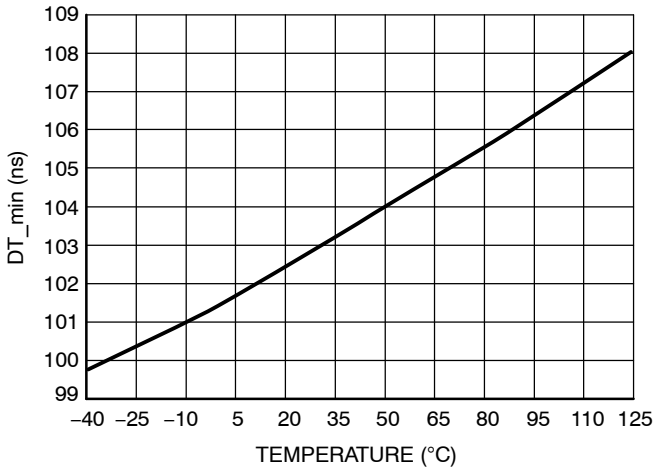


Figure 11. T_dead_min

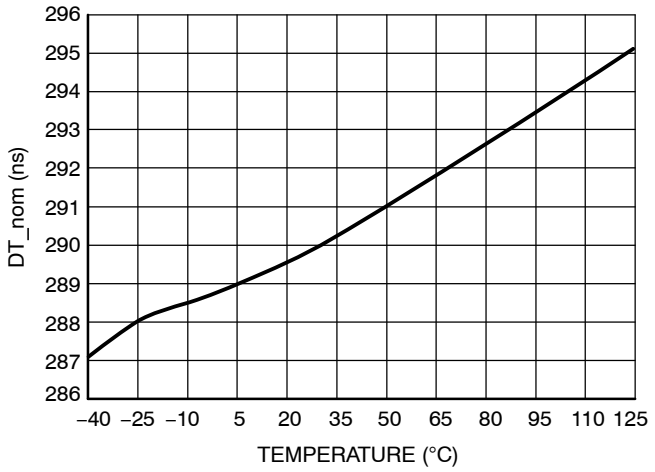


Figure 12. T_dead_nom

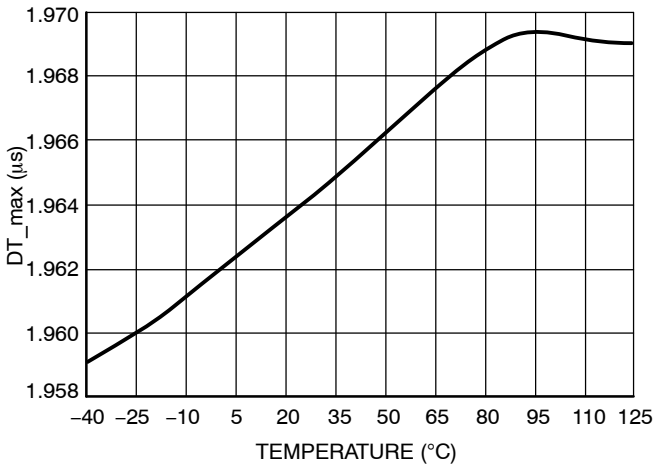


Figure 13. T_dead_max

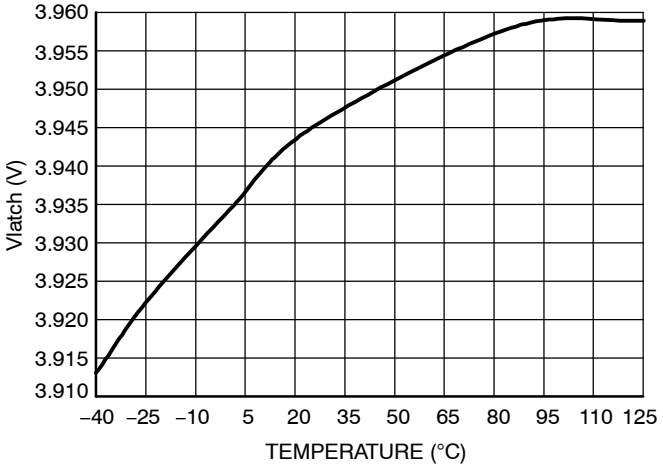


Figure 14. Latch Level (Vlatch)

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TYPICAL CHARACTERISTICS – A VERSION

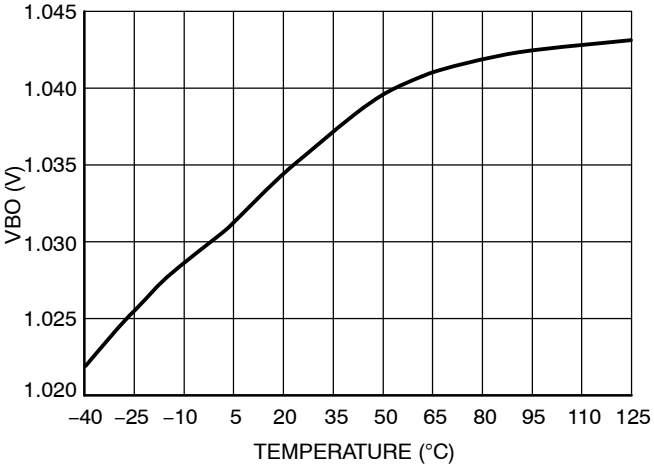


Figure 15. Brown−Out Reference (VBO)

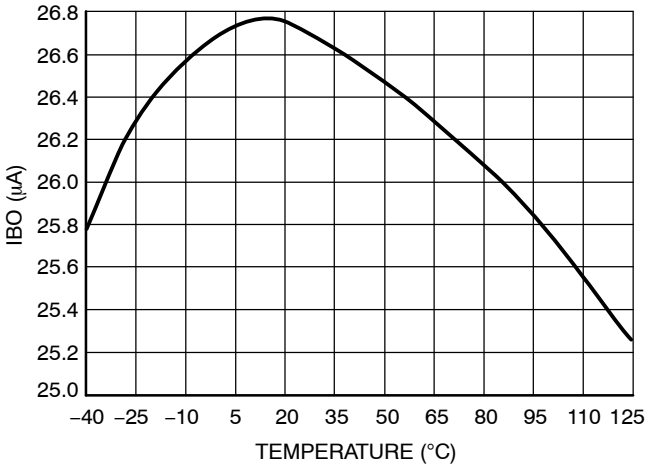


Figure 16. Brown−Out Hysteresis Current (IBO)

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TYPICAL CHARACTERISTICS – B VERSION

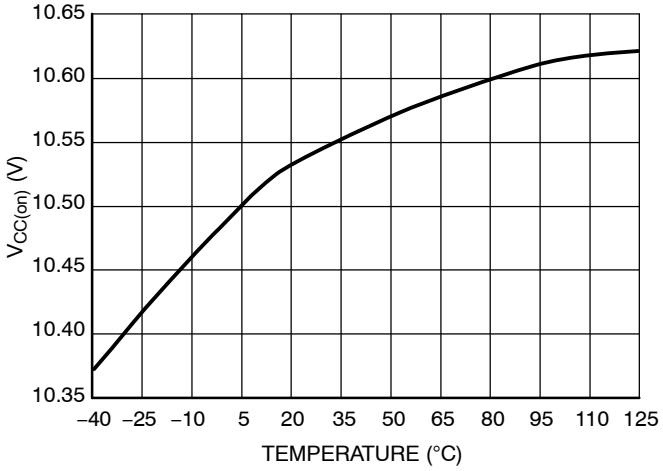


Figure 17. $V_{CC(on)}$

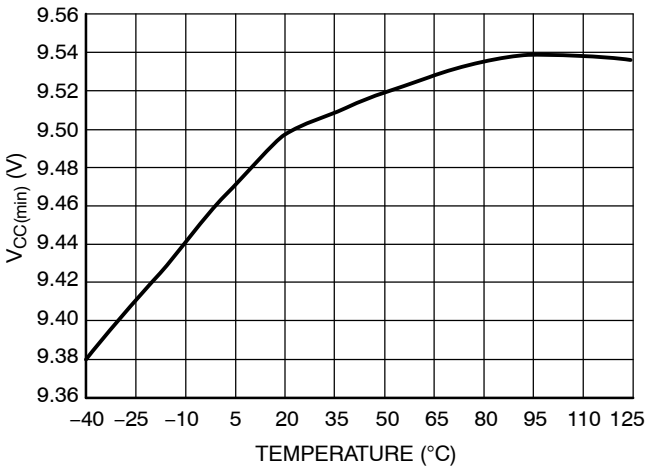


Figure 18. $V_{CC(min)}$

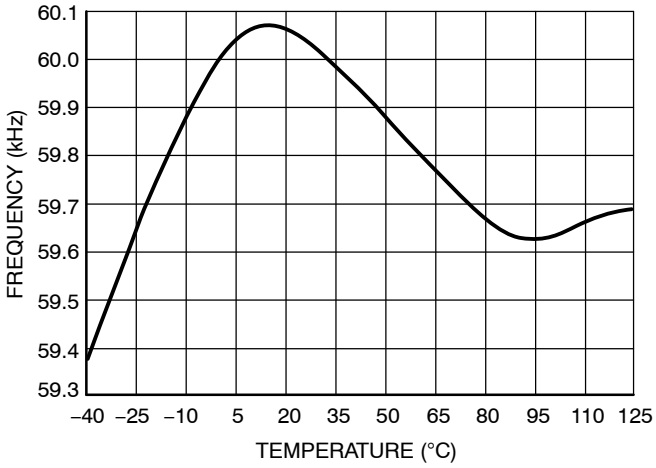


Figure 19. Fsw min

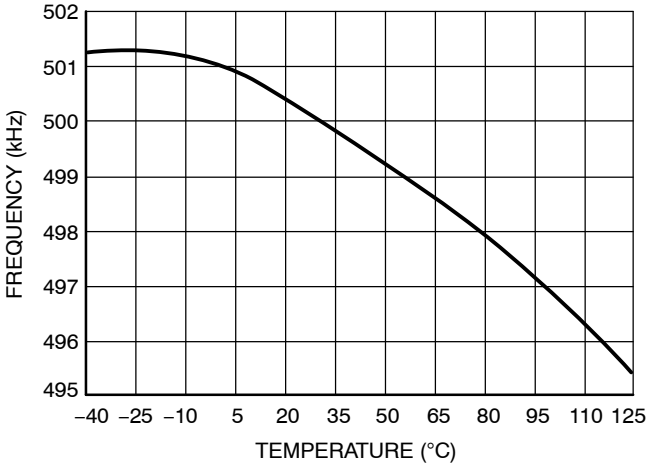


Figure 20. Fsw max

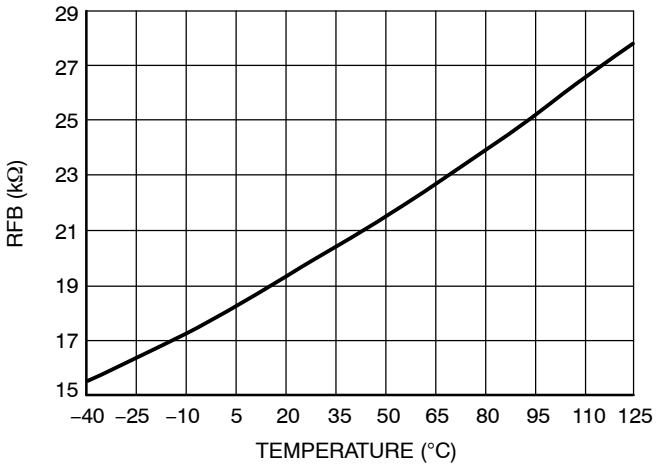


Figure 21. Pulldown Resistor (RFB)

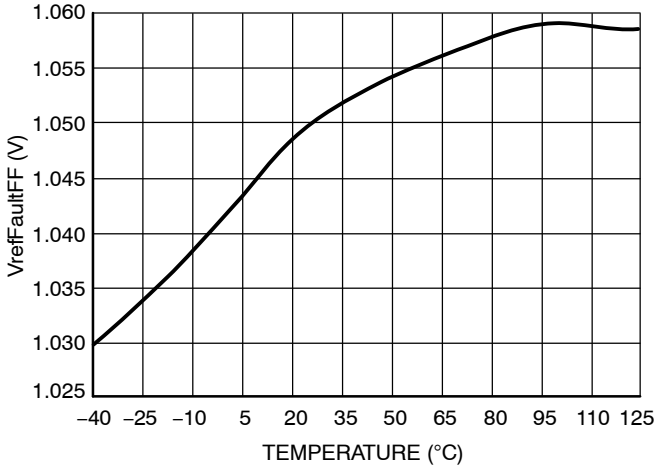


Figure 22. Fast Fault (VrefFaultF)

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TYPICAL CHARACTERISTICS – B VERSION

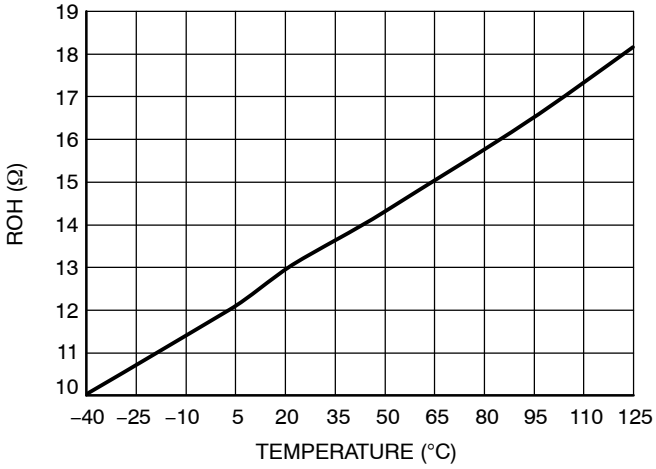


Figure 23. Source Resistance (ROH)

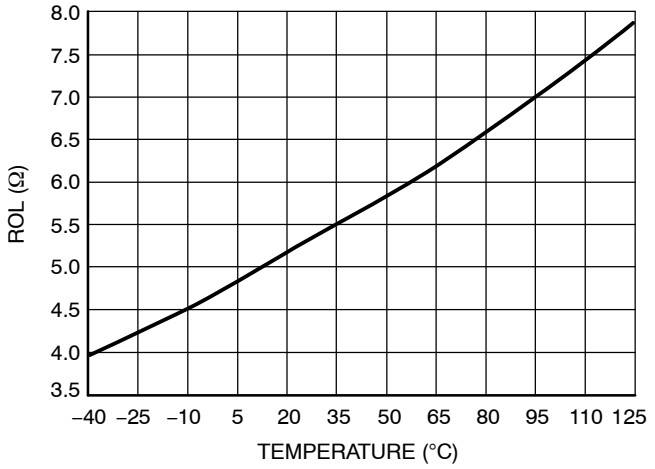


Figure 24. Sink Resistance (ROL)

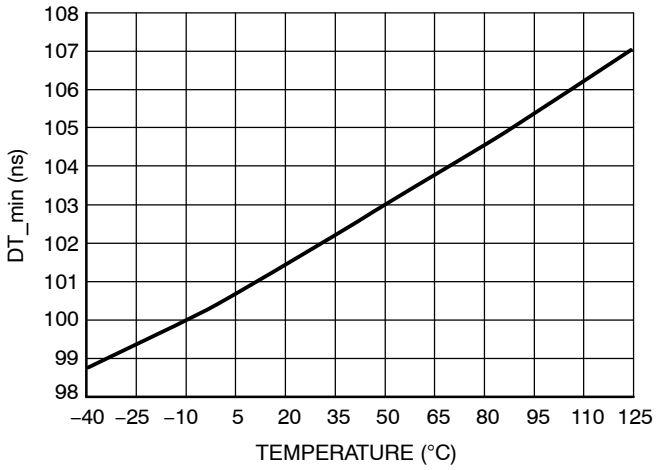


Figure 25. T_dead_min

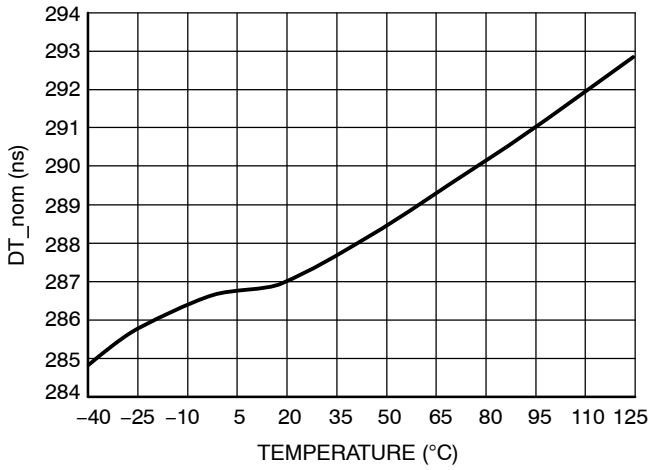


Figure 26. T_dead_nom

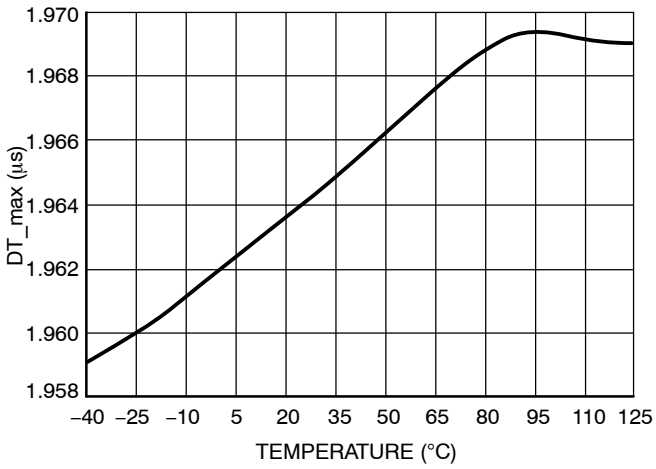


Figure 27. T_dead_max

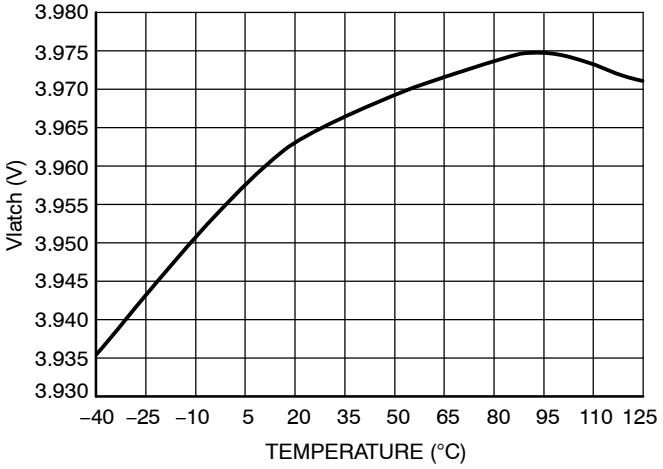


Figure 28. Latch Level (Vlatch)

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TYPICAL CHARACTERISTICS – B VERSION

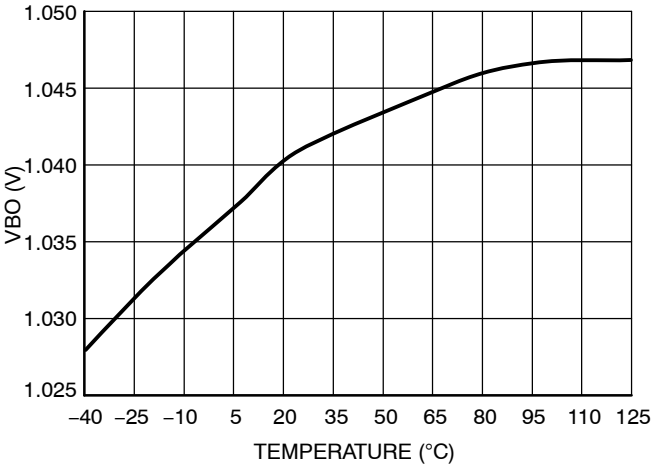


Figure 29. Brown−Out Reference (VBO)

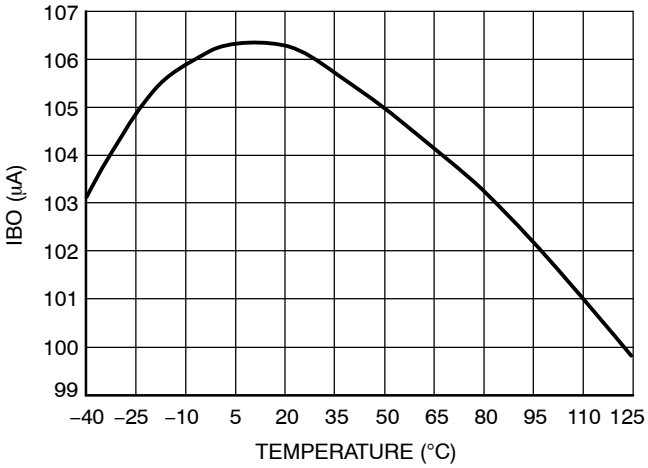


Figure 30. Brown−Out Hysteresis Current (IBO)

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APPLICATION INFORMATION

The NCP1396 A/B includes all necessary features to help building a rugged and safe switch−mode power supply featuring an extremely low standby power. The below bullets detail the benefits brought by implementing the NCP1396 controller:

- **Wide frequency range:** A high−speed Voltage Control Oscillator allows an output frequency excursion from 50 kHz up to 500 kHz on Mlower and Mupper outputs.
- **Adjustable dead−time:** Thanks to a single resistor wired to ground, the user has the ability to include some dead−time, helping to fight cross−conduction between the upper and the lower transistor.
- **Adjustable soft−start:** Every time the controller starts to operate (power on), the switching frequency is pushed to the programmed maximum value and slowly moves down toward the minimum frequency, until the feedback loop closes. The soft−start sequence is activated in the following cases: a) normal startup b) back to operation from an off state: during hiccup faulty mode, brown−out or temperature shutdown (TSD). In the NCP1396A, the soft−start is not activated back to operation from the fast fault input, unless the feedback pin voltage is below 0.6 V. To the opposite, in the B version, the soft−start is always activated back from the fast fault input whatever the feedback level is.
- **Adjustable minimum and maximum frequency excursion:** In resonant applications, it is important to stay away from the resonating peak to keep operating the converter in the right region. Thanks to a single external resistor, the designer can program its lowest frequency point, obtained in lack of feedback voltage (during the startup sequence or in short−circuit conditions). Internally trimmed capacitors offer a ±3% precision on the selection of the minimum switching frequency. The adjustable upper stop being less precise to ±15%.
- **Low startup current:** When directly powered from the high−voltage DC rail, the device only requires 300 μA to start−up. In case of an auxiliary supply, the B version offers a lower start−up threshold to cope with a 12 V dc rail.
- **Brown−Out detection:** To avoid operation from a low input voltage, it is interesting to prevent the controller from switching if the high−voltage rail is not within the right boundaries. Also, when teamed with a PFC front−end circuitry, the brown−out detection can ensure a clean start−up sequence with soft−start, ensuring that the PFC is stabilized before energizing the resonant tank. The A version features a 26.5 μA hysteresis current for the lowest consumption and the B version slightly increases this current to 100 μA in order to improve the noise immunity.
- **Adjustable fault timer duration:** When a fault is detected on the slow fault input or when the FB path is broken, a timer starts to charge an external capacitor. If the fault is removed, the timer opens the charging path and nothing happens. When the timer reaches its selected duration (via a capacitor on pin 3), all pulses are stopped. The controller now waits for the discharge via an external resistor of pin 3 capacitor to issue a new clean startup sequence with soft−start.
- **Cumulative fault events:** In the NCP1396A/B, the timer capacitor is not reset when the fault disappears. It actually integrates the information and cumulates the occurrences. A resistor placed in parallel with the capacitor will offer a simple way to adjust the discharge rate and thus the auto−recovery retry rate.
- **Fast and slow fault detection:** In some application, subject to heavy load transients, it is interesting to give a certain time to the fault circuit, before activating the protection. On the other hands, some critical faults cannot accept any delay before a corrective action is taken. For this reason, the NCP1396A/B includes a fast fault and a slow fault input. Upon assertion, the fast fault immediately stops all pulses and stays in the position as long as the driving signal is high. When released low (the fault has gone), the controller has several choices: in the A version, pulses are back to a level imposed by the feedback pin without soft−start, but in the B version, pulses are back through a regular soft−start sequence.
- **Skip cycle possibility:** The absence of soft−start on the NCP1396A fast fault input offers an easy way to implement skip cycle when power saving features are necessary. A simple resistive connection from the feedback pin to the fast fault input, and skip can be implemented.
- **Broken feedback loop detection:** Upon start−up or any time during operation, if the FB signal is missing, the timer starts to charge a capacitor. If the loop is really broken, the FB level does not grow−up before the timer ends counting. The controller then stops all pulses and waits that the timer pin voltage collapses to 1 V typically before a new attempt to re−start, via the soft−start. If the optocoupler is permanently broken, a hiccup takes place.
- **Finally, two circuit versions, A and B:** The A and B versions differ because of the following changes:
  1. The startup thresholds are different, the A starts to pulse for V_{CC} = 13.3 V whereas the B pulses for V_{CC} = 10.5 V. The turn off levels are the same however. The A is recommended for consumer

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products where the designer can use an external startup resistor, whereas the B is more recommended for industrial / medical applications where a 12 V auxiliary supply directly powers the chip.

2. The A version does not activate the soft−start upon release of the fast fault input. This is to let the designer implement skip cycle. To the opposite, the B version goes back to operation upon the fast fault pin release via a soft−start sequence.

Voltage−Controlled Oscillator

The VCO section features a high−speed circuitry allowing operation from 100 kHz up to 1 MHz. However, as a division by two internally creates the two Q and $\overline{Q}$ outputs, the final effective signal on output Mlower and Mupper switches between 50 kHz and 500 kHz. The VCO is configured in such a way that if the feedback pin goes up, the switching frequency also goes up. Figure 31 shows the architecture of this oscillator.

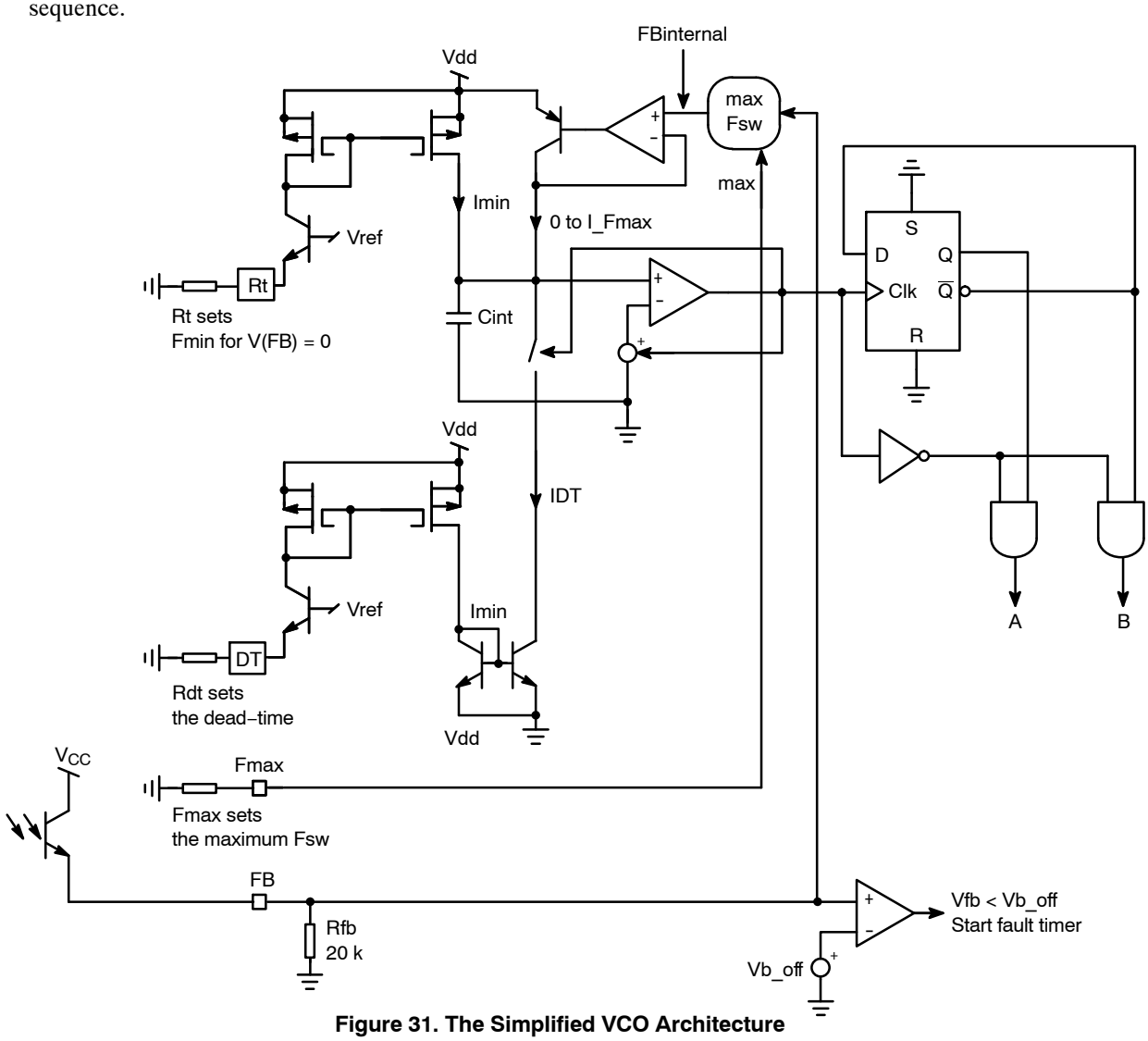


Figure 31. The Simplified VCO Architecture

The designer needs to program the maximum switching frequency and the minimum switching frequency. In LLC configurations, for circuits working above the resonant frequency, a high precision is required on the minimum frequency, hence the ±3% specification. This minimum switching frequency is actually reached when no feedback closes the loop. It can happen during the startup sequence, a strong output transient loading or in a short−circuit condition. By installing a resistor from pin 4 to GND, the minimum frequency is set. Using the same philosophy, wiring a resistor from pin 2 to GND will set the maximum frequency excursion. To improve the circuit protection features, we have purposely created a dead zone, where the feedback loop has no action. This is typically below 1.2 V. Figure 32 details the arrangement where the internal voltage (that drives the VCO) varies between 0 and 2.3 V. However, to create this swing, the feedback pin (to which the optocoupler emitter connects), will need to swing typically between 1.2 V and 5.3 V.

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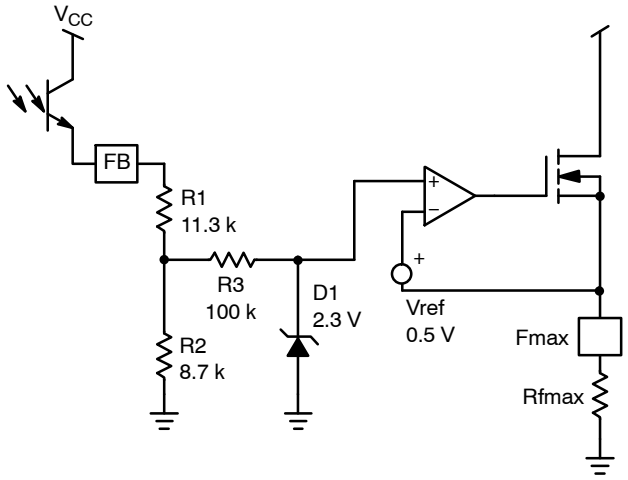


Figure 32. The OPAMP Arrangement Limits the VCO Modulation Signal between 0.5 and 2.3 V

This techniques allows us to detect a fault on the converter in case the FB pin cannot rise above 0.6 V (to actually close the loop) in less than a duration imposed by the programmable timer. Please refer to the fault section for detailed operation of this mode.

As shown on Figure 32, the internal dynamics of the VCO control voltage will be constrained between 0.5 V and 2.3 V, whereas the feedback loop will drive pin 6 (FB) between 1.2 V and 5.3 V. If we take the default FB pin excursion numbers, 1.2 V = 50 kHz, 5.3 V = 500 kHz, then the VCO maximum slope will be:

$$\frac{500\ k - 50\ k}{4.1} = 109.7\ kHz/V$$

Figures 33 and 34 portray the frequency evolution depending on the feedback pin voltage level in a different frequency clamp combination.

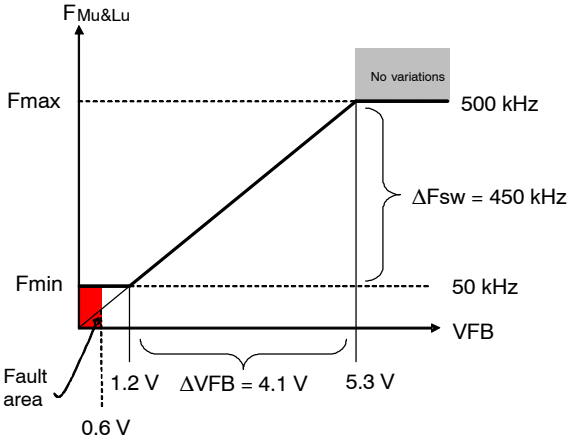


Figure 33. Maximal Default Excursion, Rt = 22 kΩ on pin 4 and Rfmax = 1.3 kΩ on pin 2

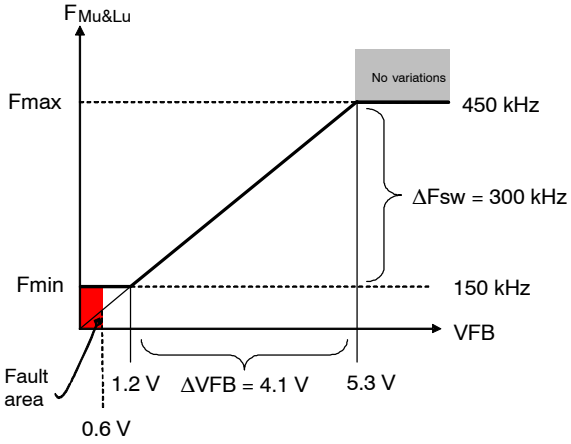


Figure 34. Here a different minimum frequency was programmed as well as a maximum frequency excursion

Please note that the previous small−signal VCO slope has now been reduced to 300 k / 4.1 = 73 kHz / V on Mupper and Mlower outputs. This offers a mean to magnify the feedback excursion on systems where the load range does not generate a wide switching frequency excursion. Thanks to this option, we will see how it becomes possible to observe the feedback level and implement skip cycle at light loads. It is important to note that the frequency evolution does not have a real linear relationship with the feedback voltage. This is due to the deadtime presence which stays constant as the switching period changes.

The selection of the three setting resistors (Fmax, Fmin deadtime) requires the usage of the selection charts displayed below:

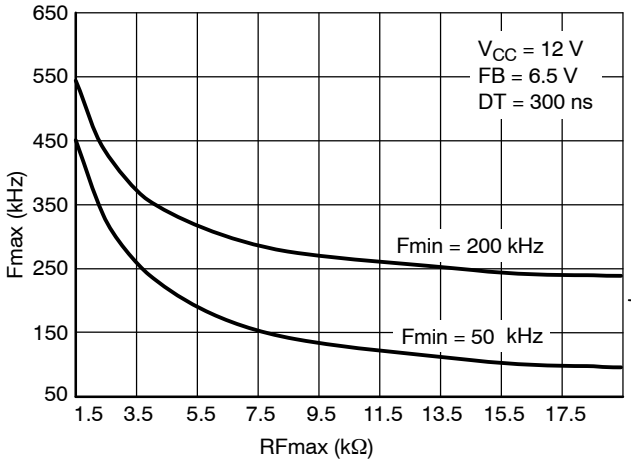


Figure 35. Maximum Switching Frequency Resistor Selection Depending on the Adopted Minimum Switching Frequency

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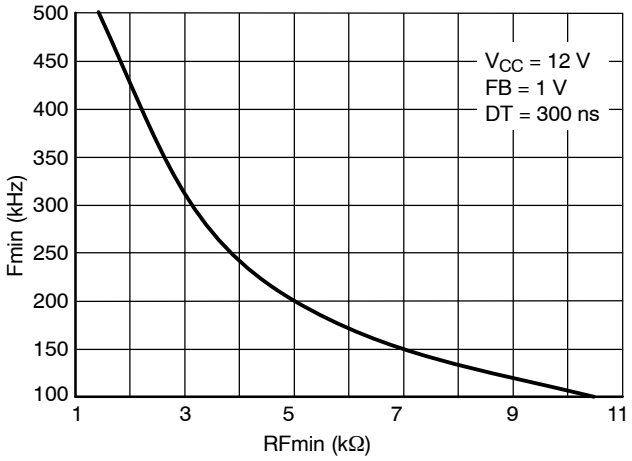


Figure 36. Minimum Switching Frequency Resistor Selection (Fmin = 100 kHz to 500 kHz)

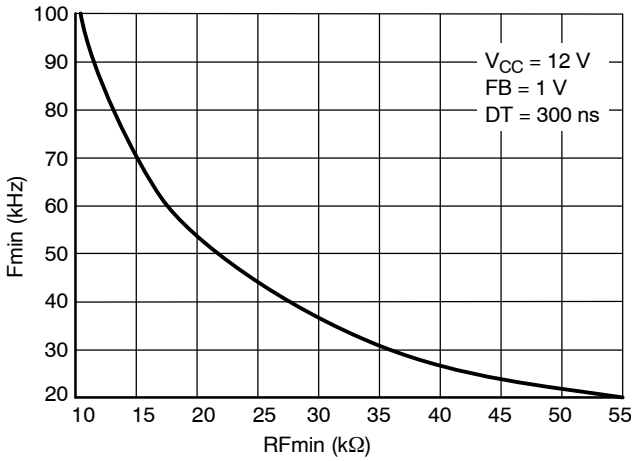


Figure 37. Minimum Switching Frequency Resistor Selection (Fmin = 20 kHz to 100 kHz)

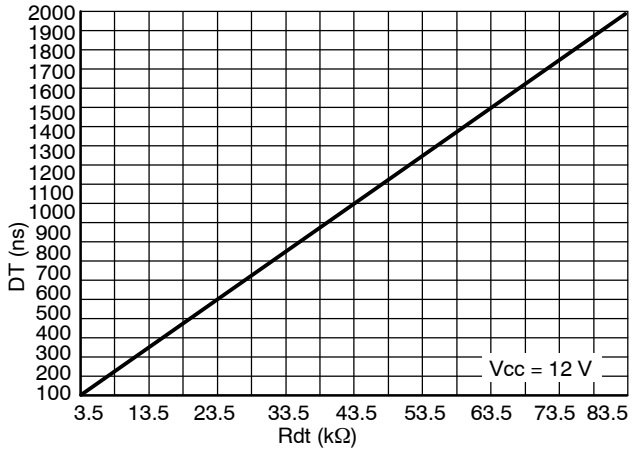


Figure 38. Dead−Time Resistor Selection

ORing Capability

If for any particular reason, there is a need for a frequency variation linked to an event appearance (instead of abruptly stopping pulses), then the FB pin lends itself very well to the addition of other sweeping loops. Several diodes can easily be used perform the job in case of reaction to a fault event or to regulate on the output current (CC operation). Figure 39 shows how to do it.

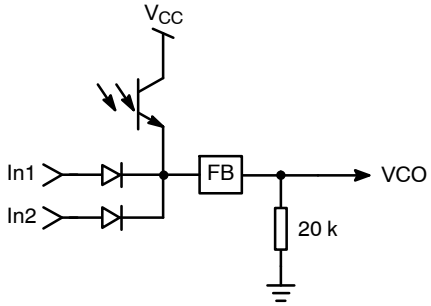


Figure 39. Thanks to the FB Configuration, Loop ORing is Easy to Implement

Dead−time Control

Dead−time control is an absolute necessity when the half−bridge configuration comes to play. The dead−time technique consists in inserting a period during which both high and low side switches are off. Of course, the dead−time amount differs depending on the switching frequency, hence the ability to adjust it on this controller. The option ranges between 100 ns and 2 μs. The dead−time is actually made by controlling the oscillator discharge current. Figure 40 portrays a simplified VCO circuit based on Figure 31.

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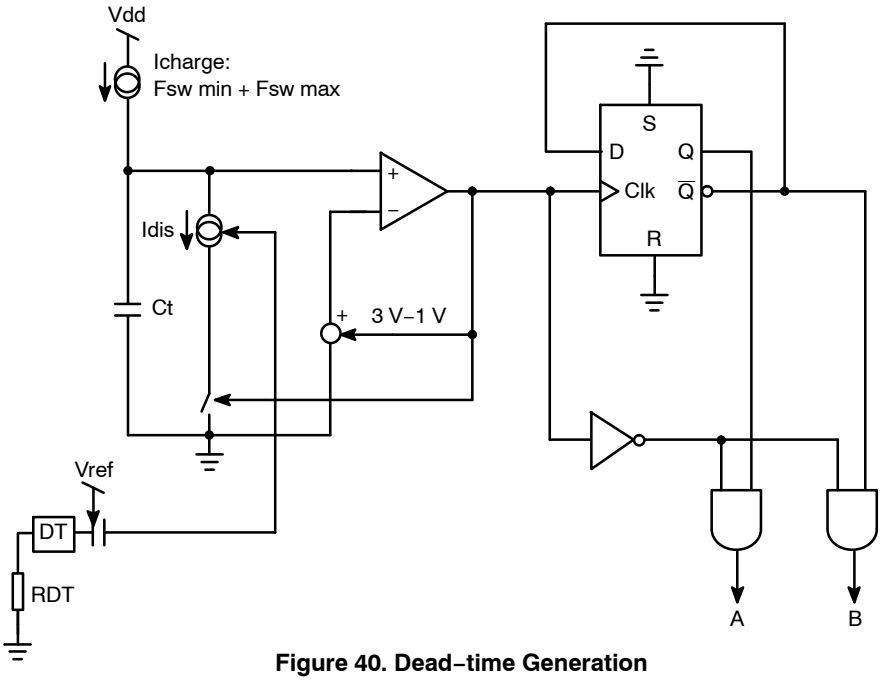


Figure 40. Dead−time Generation

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During the discharge time, the clock comparator is high and un−validates the AND gates: both outputs are low. When the comparator goes back to the low level, during the timing capacitor Ct recharge time, A and B outputs are validated. By connecting a resistor RDT to ground, it creates a current whose image serves to discharge the Ct capacitor: we control the dead−time. The typical range evolves between 100 ns (RDT = 3.5 kΩ) and 2 μs (RDT = 83.5 kΩ). Figure 43 shows the typical waveforms.

Soft−start Sequence

In resonant controllers, a soft−start is needed to avoid suddenly applying the full current into the resonating circuit. In this controller, a soft−start capacitor connects to pin 1 and offers a smooth frequency variation upon start−up: when the circuit starts to pulse, the VCO is pushed to the maximum switching frequency imposed by pin 2. Then, it linearly decreases its frequency toward the minimum frequency selected by a resistor on pin 4. Of course, practically, the feedback loop is suppose to take over the VCO lead as soon as the output voltage has reached the target. If not, then the minimum switching frequency is reached and a fault is detected on the feedback pin (typically below 600 mV). Figure 41 depicts a typical frequency evolution with soft−start.

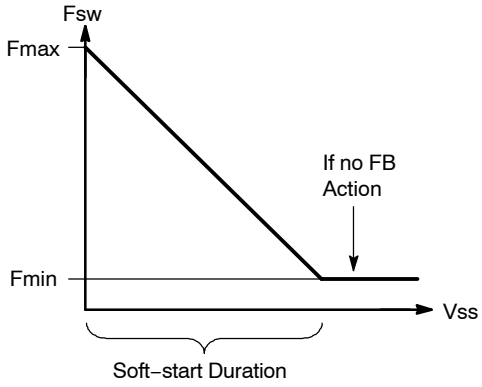


Figure 41. Soft−start Behavior

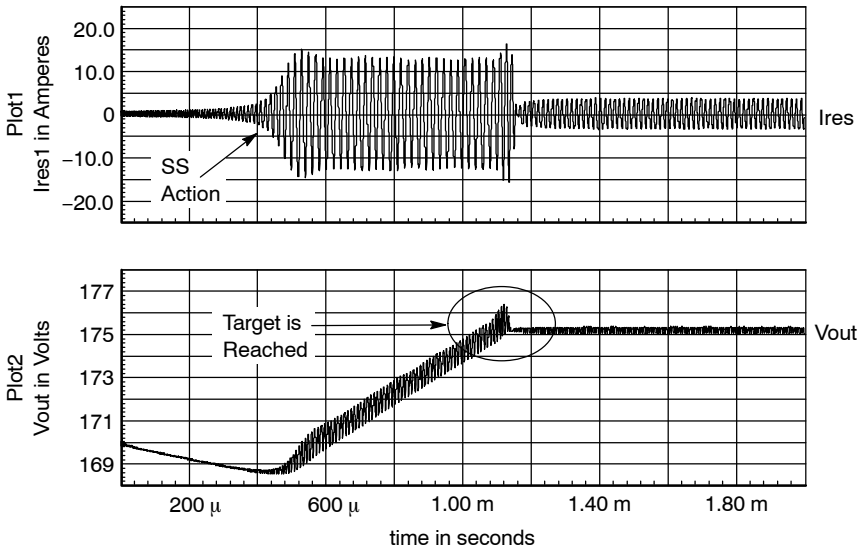


Figure 42. A Typical Start−up Sequence on a LLC Converter

Please note that the soft−start will be activated in the following conditions:

- A startup sequence
- During auto−recovery burst mode
- A brown−out recovery
- A temperature shutdown recovery

The fast fault input undergoes a special treatment. Since we want to implement skip cycle through the fast fault input on the NCP1396A, we cannot activate the soft−start every time the feedback pin stops the operations in low power mode. Therefore, when the fast fault pin is released, no soft−start occurs to offer the best skip cycle behavior. However, it is very possible to combine skip cycle and true fast fault input, e.g. via ORing diodes driving pin 6. In that case, if a signal maintains the fast fault input high long enough to bring the feedback level down (that is to say below 0.6 V) since the output voltage starts to fall down, then the soft−start is activated after the release of the pin. In the B version tailored to operate from an auxiliary 12 V power supply, the soft−start is always activated upon the fast fault input release, whatever the feedback condition is.

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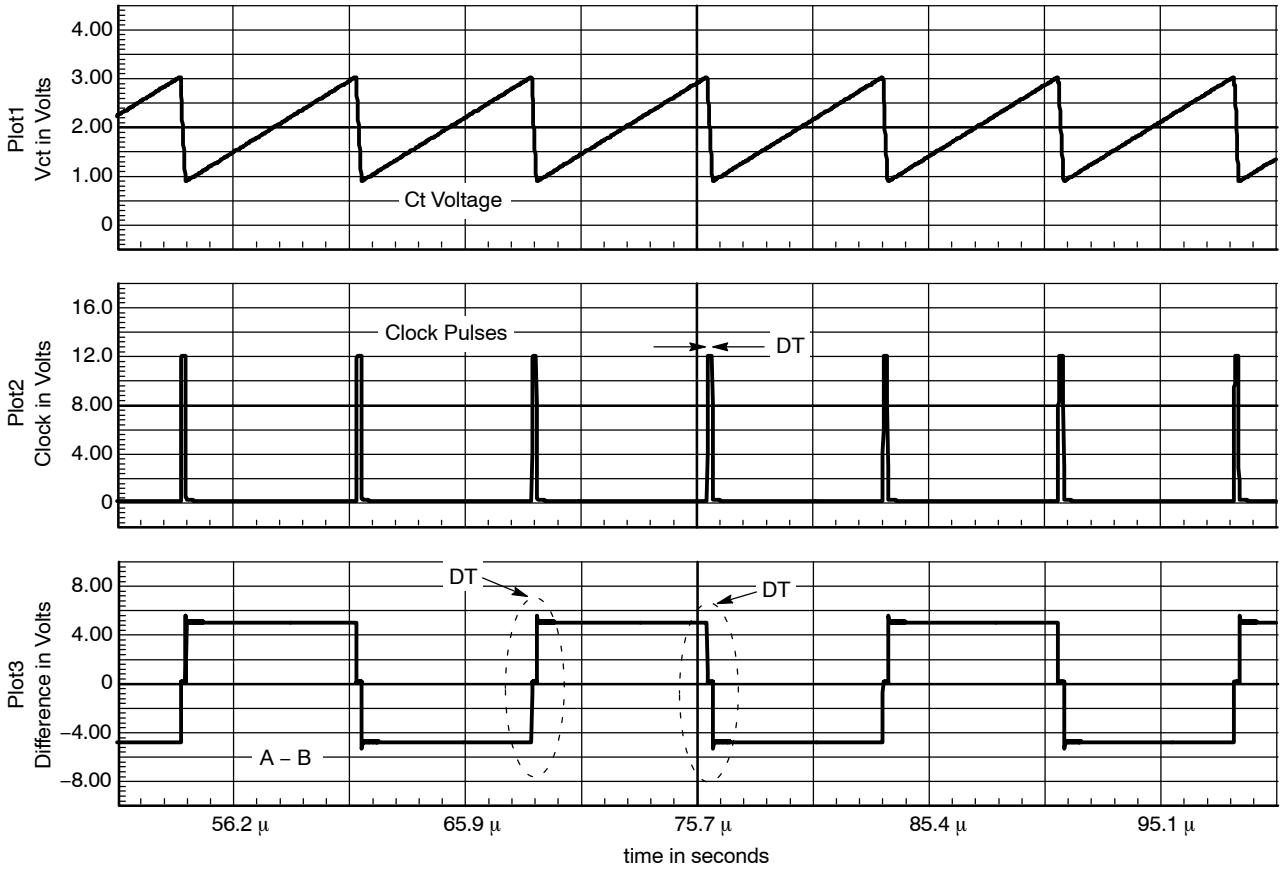


Figure 43. Typical Oscillator Waveforms

Brown−Out Protection

The Brown−Out circuitry (BO) offers a way to protect the resonant converter from low DC input voltages. Below a given level, the controller blocks the output pulses, above it, it authorizes them. The internal circuitry, depicted by Figure 44, offers a way to observe the high−voltage (HV) rail. A resistive divider made of Rupper and Rlower, brings a portion of the HV rail on pin 5. Below the turn−on level, the 26.5 µA current source IBO is off. Therefore, the turn−on level solely depends on the division ratio brought by the resistive divider.

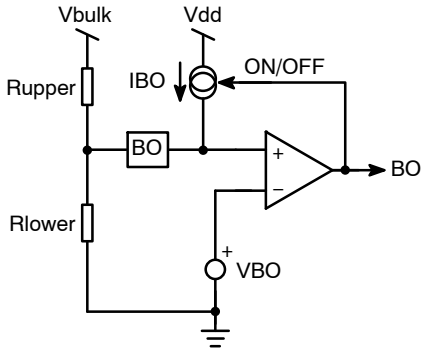


Figure 44. The Internal Brown−out Configuration with an Offset Current Source

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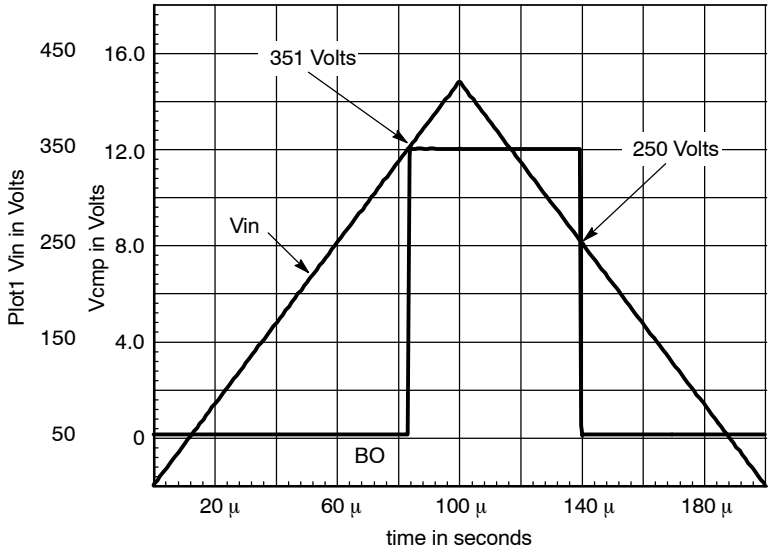


Figure 45. Simulation Results for 350 / 250 ON / OFF Levels

To the contrary, when the internal BO signal is high (Mlower and Mupper pulse), the IBO source is activated and creates a hysteresis. As a result, it becomes possible to select the turn−on and turn−off levels via a few lines of algebra:

IBO is off

$$V(+) = V_{bulk1} \times \frac{R_{lower}}{R_{lower} + R_{upper}} \qquad \text{(eq. 1)}$$

IBO is on

$$V(+) = V_{bulk2} \times \frac{R_{lower}}{R_{lower} + R_{upper}} + IBO \times \left(\frac{R_{lower} \times R_{upper}}{R_{lower} + R_{upper}} \right) \qquad \text{(eq. 2)}$$

We can now extract Rlower from equation 1 and plug it into equation 2, then solve for Rupper:

$$R_{upper} = R_{lower} \times \frac{V_{bulk1} - VBO}{VBO} \qquad \text{(eq. 3)}$$

$$R_{lower} = VBO \times \frac{V_{bulk1} - V_{bulk2}}{IBO \times (V_{bulk1} - VBO)} \qquad \text{(eq. 4)}$$

If we decide to turn−on our converter for Vbulk1 equals 350 V and turn it off for Vbulk2 equals 250 V, then for A version (IBO_A = 26.5 µA, VBO = 1.04 V) we obtain:

Rupper = 3.77 MΩ

Rlower = 11.25 kΩ

The bridge power dissipation is 400^2 / 3.781 MΩ = 42 mW when front−end PFC stage delivers 400 V.

Figure 45 simulation result confirms our calculations.

Latch−off Protection

There are some situations where the converter shall be fully turned−off and stay latched. This can happen in presence of an over−voltage (the feedback loop is drifting) or when an over temperature is detected. Thanks to the addition of a comparator on the BO pin, a simple external circuit can lift up this pin above VLATCH (4 V typical) and permanently disable pulses. The V_{CC} needs to be cycled down below 6.5 V typically to reset the controller.

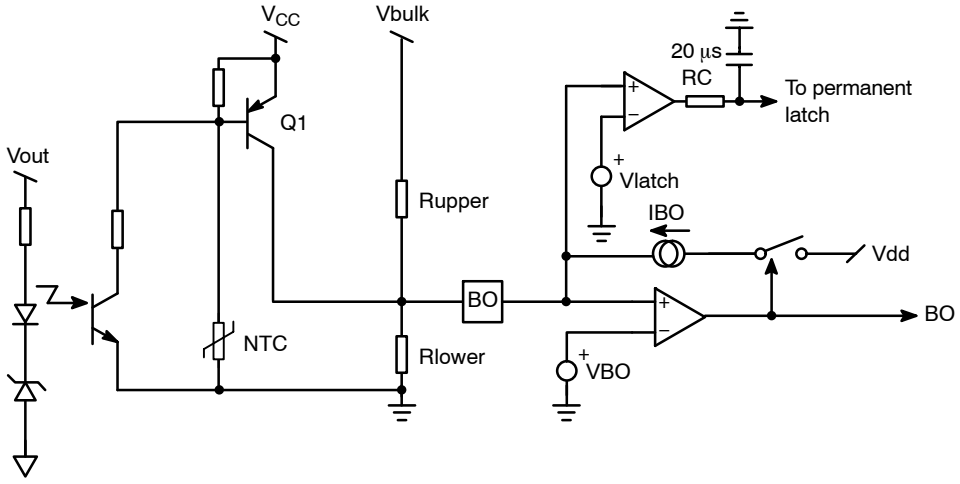


Figure 46. Adding a comparator on the BO pin offers a way to latch−off the controller

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On Figure 46, Q1 is blocked and does not bother the BO measurement as long as the NTC and the optocoupler are not activated. As soon as the secondary optocoupler senses an OVP condition, or the NTC reacts to a high ambient temperature, Q1 base is brought to ground and the BO pin goes up, permanently latching off the controller.

Protection Circuitry

This resonant controller differs from competitors thanks to its protection features. The device can react to various inputs like:

– *Fast events input:* like an over−current condition, a need to shut down (sleep mode) or a way to force a controlled burst mode (skip cycle at low output power): as soon as the input level exceeds 1 V typical, pulses are immediately stopped. When the input is released, the controller performs a clean startup sequence including a soft−start period.

– *Slow events input:* this input serves as a delayed shutdown, where an event like a transient overload does not immediately stopped pulses but start a timer. If the event duration lasts longer than what the timer imposes, then all pulses are disabled. The voltage on the timer capacitor (pin 3) starts to decrease until it reaches 1 V. The decrease rate is actually depending on the resistor the user will put in parallel with the capacitor, giving another flexibility during design.

Figure 47 depicts the architecture of the fault circuitry.

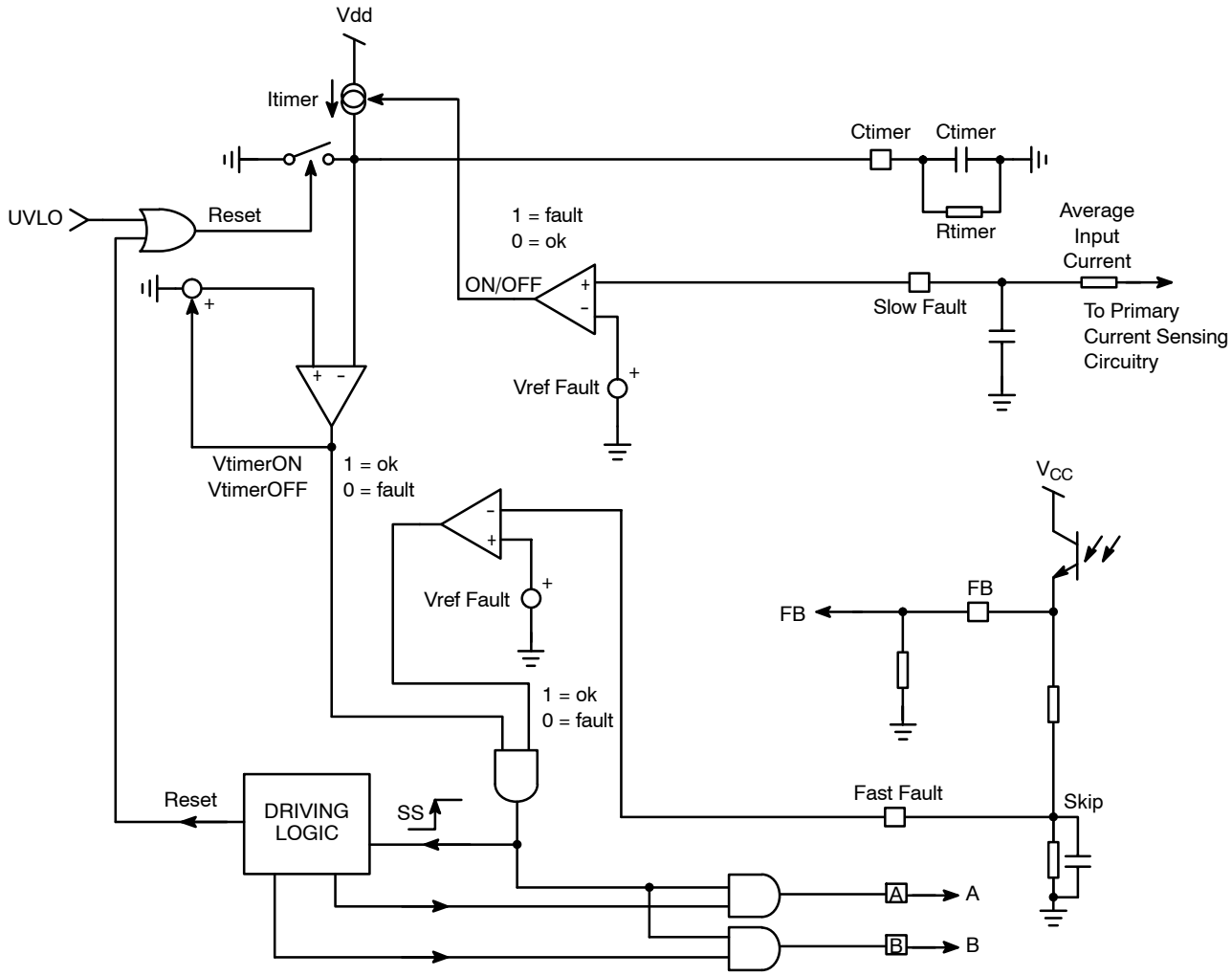


Figure 47. This circuit combines a slow and fast input for improved protection features

Slow Input

On this circuit, the slow input goes to a comparator. When this input exceeds 1 V typical, the current source Itimer turns on, charging the external capacitor Ctimer. If the fault duration is long enough, when Ctimer voltage

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reaches the VtimerON level (4 V typical), then all pulses are stopped. If the fault input signal is still present, then the controller permanently stays off and the voltage on the timer capacitor does not move (Itimer is on and the voltage is clamped to 5 V). If the fault input signal is removed (because pulses are off for instance), Itimer turns off and the capacitor slowly discharges to ground via a resistor installed in parallel with it. As a result, the designer can easily determine the time during which the power supply stays locked by playing on Rtimer. Now, when the timer capacitor voltage reaches 1 V typical (VtimerOFF), the comparator instructs the internal logic to issues pulses as on a clean soft−start sequence (soft−start is activated). Please note that the discharge resistor can not be lower than 4 V / Itimer otherwise the voltage on Ctimer will not reach the turn−off voltage of 4 V.

In both cases, when the fault is validated, both outputs Mlower and Mupper are internally pulled down to ground.

On Figure 46 example, a voltage proportional to primary current, once averaged, gives an image of the input power in case Vin is kept constant via a PFC circuit. If the output loading increases above a certain level, the voltage on this pin will pass the 1 V threshold and start the timer. If the overload stays there, after a few tens of milli−seconds, switching pulses will disappear and a protective auto−recovery cycle will take place. Adjusting the resistor R in parallel with the timer capacitor will give the flexibility to adjust the fault burst mode.

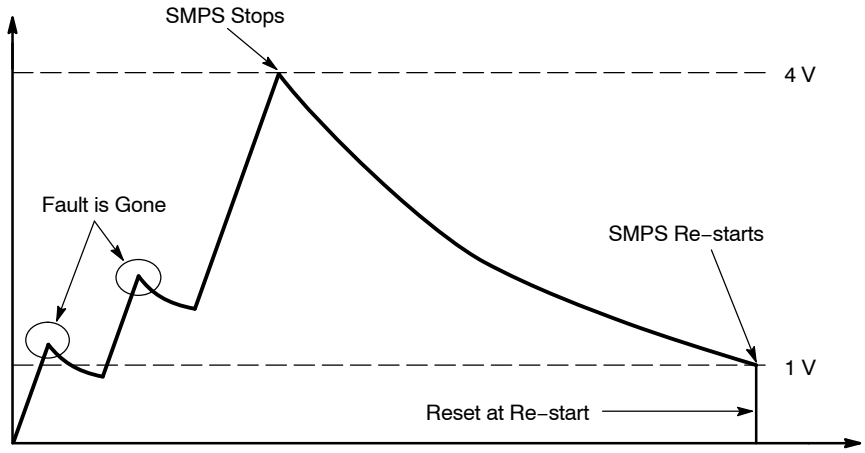


Figure 48. A resistor can easily program the capacitor discharge time

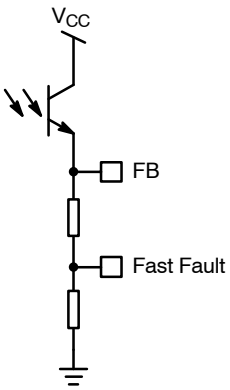


Figure 49. Skip cycle can be implemented via two resistors on the FB pin to the Fast fault input

Fast Input

The fast input is not affected by a delayed action. As soon as its voltage exceeds 1 V typical, all pulses are off and maintained off as long as the fault is present. When the pin is released, pulses come back and the soft−start is activated.

Thanks to the low activation level of 1 V, this pin can observe the feedback pin via a resistive divided and thus implement skip cycle operation. The resonant converter can be designed to lose regulation in light load conditions, forcing the FB level to increase. When it reaches the programmed level, it triggers the fast fault input and stops pulses. Then Vout slowly drops, the loop reacts by decreasing the feedback level which, in turn, unlocks the pulses, Vout goes up again and so on: we are in *skip cycle* mode.

Startup Behavior

When the V_{CC} voltage grows−up, the internal current consumption is kept to Istrup, allowing to crank−up the converter via a resistor connected to the bulk capacitor. When V_{CC} reaches the $V_{CC(on)}$ level, output Mlower goes high first and then output Mupper. This sequence will always be the same whatever triggers the pulse delivery: fault, OFF to ON etc… Pulsing the output Mlower high first gives an immediate charge of the bootstrap capacitor. Then, the rest of pulses follow, delivered at the highest switching value, set by the resistor on pin 2. The soft−start capacitor ensures a smooth frequency decrease to either the programmed minimum value (in case of fault) or to a value corresponding to the operating point if the feedback loop closes first. Figure 50 shows typical signals evolution at power on.

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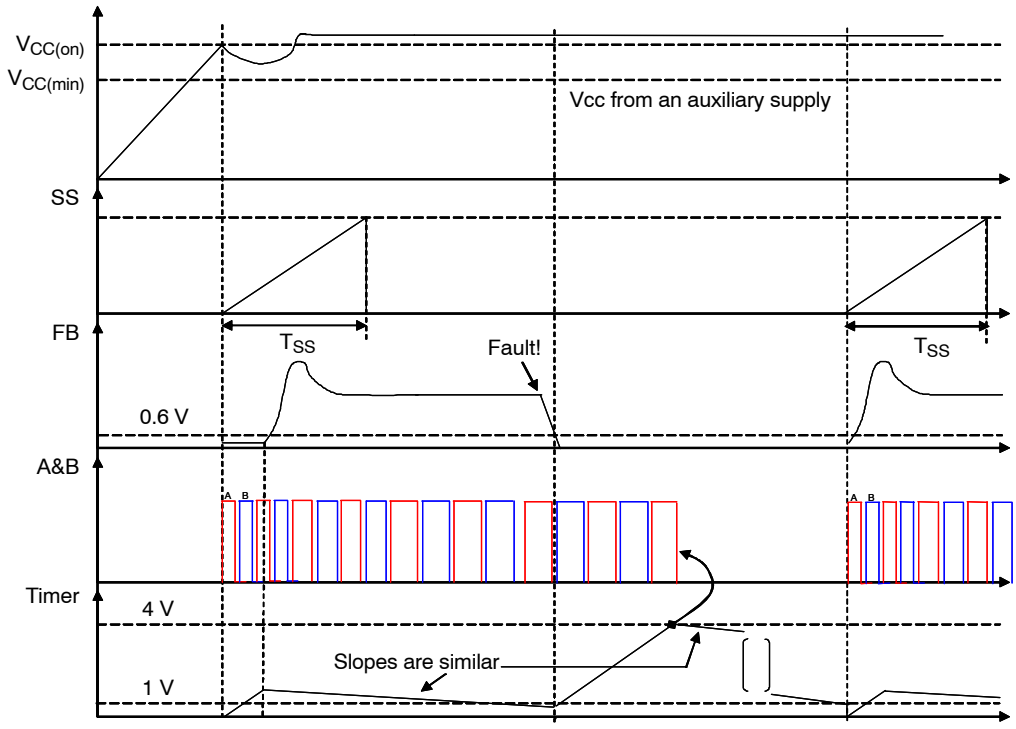


Figure 50. At power on, output A is first activated and the frequency slowly decreases via the soft−start capacitor

Figure 50 depicts an auto−recovery situation, where the timer has triggered the end of output pulses. In that case, the V_{CC} level was given by an auxiliary power supply, hence its stability during the hiccup. A similar situation can arise if the user selects a more traditional startup method, with an auxiliary winding. In that case, the $V_{CC(min)}$ comparator stops the output pulses whenever it is activated, that is to say, when V_{CC} falls below 10 V typical. At this time, the V_{CC} pin still receives its bias current from the startup resistor and heads toward $V_{CC(on)}$ via the V_{CC} capacitor. When the voltage reaches $V_{CC(on)}$, a standard sequence takes place, involving a soft−start. Figure 51 portrays this behavior.

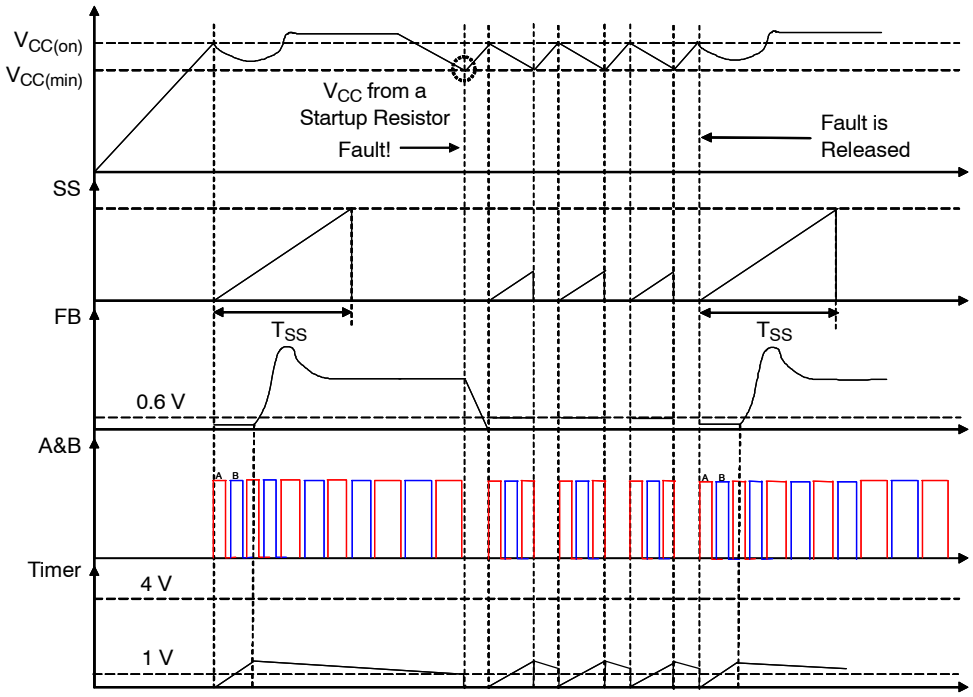


Figure 51. When the V_{CC} is too low, all pulses are stopped until V_{CC} goes back to the startup voltage

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As described in the data−sheet, two startup levels $V_{CC(on)}$ are available, via two circuit versions. The NCP1396 features sufficient hysteresis (3 V typically) to allow a classical startup method with a resistor connected to the bulk capacitor. Then, at the end of the startup sequence, an auxiliary winding is supposed to take over the controller supply voltage. To the opposite, for applications where the resonant controller is powered from a standby power supply, the startup level is 10 V typically and allows for the direct a connection from a 12 V source. Thanks to this NCP1396B, simple ON/OFF operation is therefore feasible.

The High−voltage Driver

The driver features a traditional bootstrap circuitry, requiring an external high−voltage diode for the capacitor refueling path. Figure 52 shows the internal architecture of the high−voltage section.

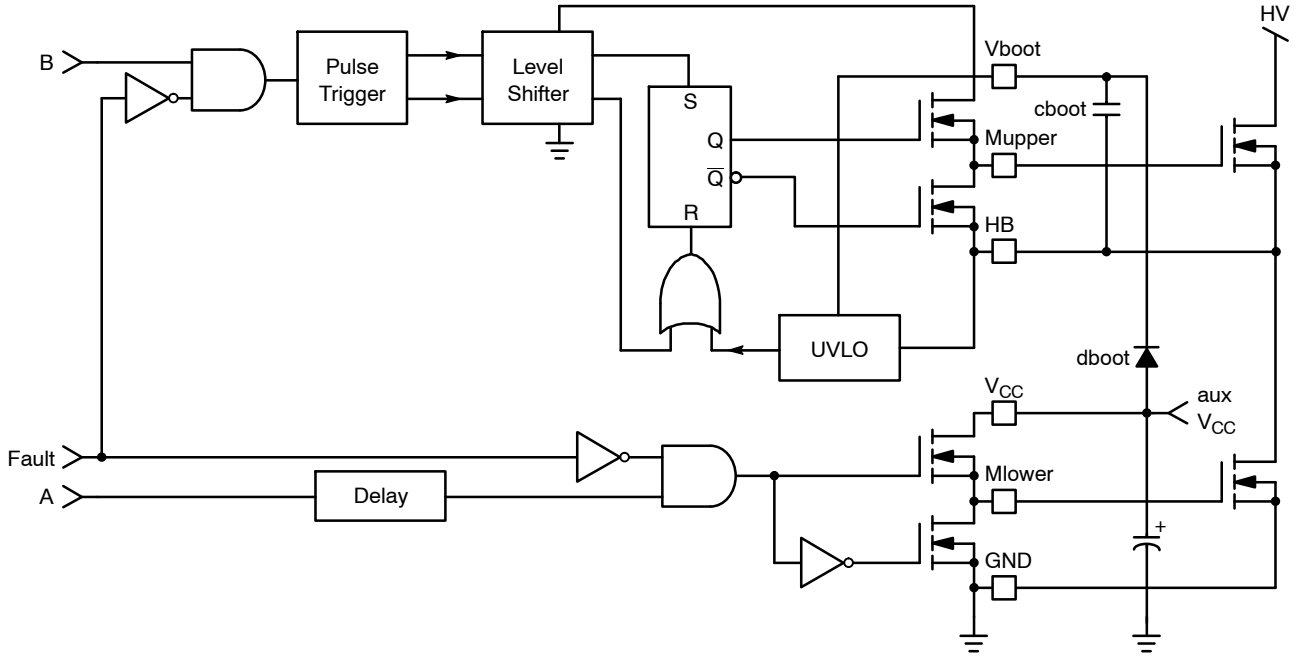


Figure 52. The Internal High−voltage Section of the NCP1396

The device incorporates an upper UVLO circuitry that makes sure enough Vgs is available for the upper side MOSFET. The B and A outputs are delivered by the internal logic, as Figure 47 testifies. A delay is inserted in the lower rail to ensure good matching between these propagating signals.

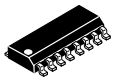
As stated in the maximum rating section, the floating portion can go up to 600 VDC and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front−end stage.

ORDERING INFORMATION

Device	Package	Shipping†
NCP1396ADR2G	SOIC−16, Less Pin 13 (Pb−Free)	2500 / Tape & Reel
NCP1396BDR2G	SOIC−16, Less Pin 13 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

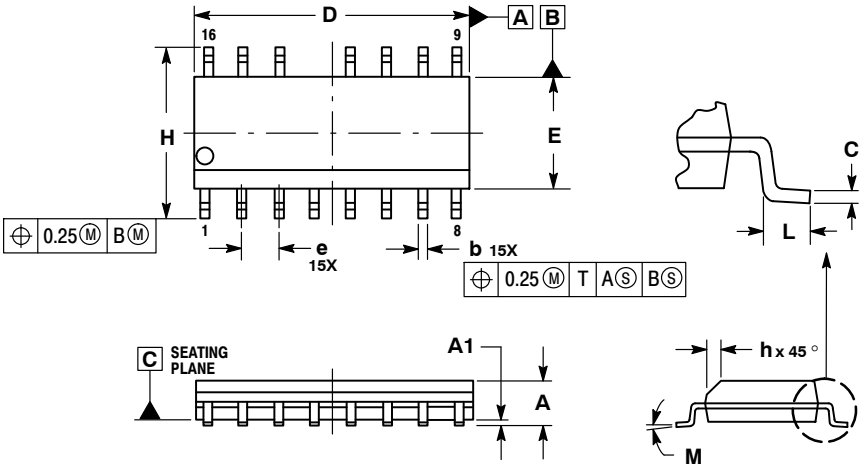
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SCALE 1:1

SOIC−16 NB, LESS PIN 13
CASE 751AM
ISSUE O

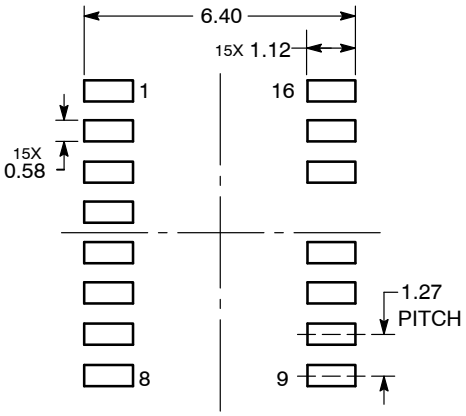
DATE 20 AUG 2007



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

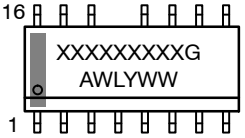
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
M	0 °	7 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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