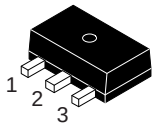
Bipolar Transistor

(−)50 V, (−)4 A, Low VCE(sat), (PNP) NPN Single PCP

2SA2013, 2SC5566



SOT−89 / PCP−1
CASE 419AU

Features

- Adoption of FBET and MBIT Processes
- Low Collector−to−Emitter Saturation Voltage
- Ultrasmall Package Facilitales Miniaturization in End Products
- High Allowable Power Dissipation
- Large Current Capacity
- High−speed Switching

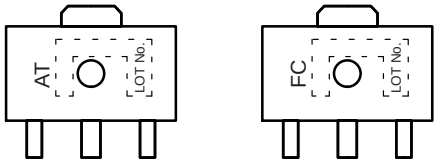
Applications

- Relay Drivers, Lamp Drivers, Motor Drivers, Flash

Specifications

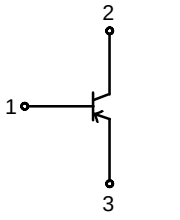
( ): 2SA2013

MARKING DIAGRAM

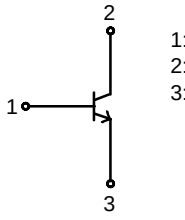


2SA2013 2SC5566

ELECTRICAL CONNECTION



2SA2013



2SC5566

1: Base
2: Collector
3: Emitter

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Collector−to−Base Voltage	V_{CBO}		(−50) 100	V
Collector−to−Emitter Voltage	V_{CES}		(−50) 100	V
Collector−to−Emitter Voltage	V_{CEO}		(−)50	V
Emitter−to−Base Voltage	V_{EBO}		(−)6	V
Collector Current	I_C		(−)4	A
Collector Current (Pulse)	I_{CP}		(−)7	A
Base Current	I_B		(−)600	mA
Collector Dissipation	P_C	When mounted on ceramic substrate (250 mm^2 x 0.8 mm)	1.3	W
		Tc = 25°C	3.5	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package Type (JEITA, JEDEC)	Shipping†
2SA2013−TD−E	PCP (Pb−Free)	1000 / Tape & Reel
2SC5566−TD−E		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

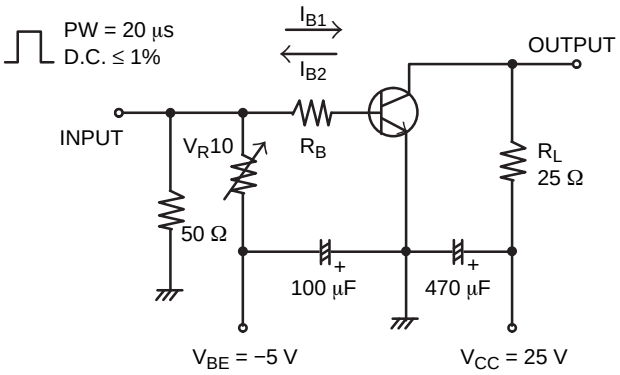
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Collector Cutoff Current	I_{CBO}	V_{CB} = (−)40 V, I_E = 0 A	−	−	(−)1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = (−)4 V, I_C = 0 A	−	−	(−)1	μA
DC Current Gain	h_{FE}	V_{CE} = (−)2 V, I_C = (−)500 mA	200	−	560	
Gain−Bandwidth Product	f_T	V_{CE} = (−)10 V, I_C = (−)500 mA	−	(360) 400	−	MHz
Output Capacitance	Cob	V_{CB} = (−)10 V, f = 1 MHz	−	(24) 15	−	pF
Collector−to−Emitter Saturation Voltage	V_{CE}(sat)1	I_C = (−)1 A, I_B = (−)50 mA	−	(−105) 85	(−180) 130	mV
	V_{CE}(sat)2	I_C = (−)2 A, I_B = (−)100 mA	−	(−200) 150	(−340) 225	mV
Base−to−Emitter Saturation Voltage	V_{BE}(sat)	I_C = (−)2 A, I_B= (−)100 mA	−	(−) 0.89	(−)1.2	V
Collector−to−Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = (−)10 μA, I_E = 0 A	(−50) 100	−	−	V
Collector−to−Emitter Breakdown Voltage	$V_{(BR)CES}$	I_C = (−)100 μA, R_{BE} = 0 Ω	(−50) 100	−	−	V
Collector−to−Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = (−)1 mA, R_{BE} = ∞	(−)50	−	−	V
Emitter−to−Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = (−)10 μA, I_C = 0 A	(−)6	−	−	V
Turn−ON Time	t_{on}	See specified Test Circuit.	−	(30) 35	−	ns
Storage Time	t_{stg}		−	(230) 300	−	ns
Fall Time	t_f		−	(15) 20	−	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Switching Time Test Circuit



I_C = 10I_{B1} = −10I_{B2} = 1 A
For PNP, the polarity is reversed.

Figure 1. Switching Time Test Circuit

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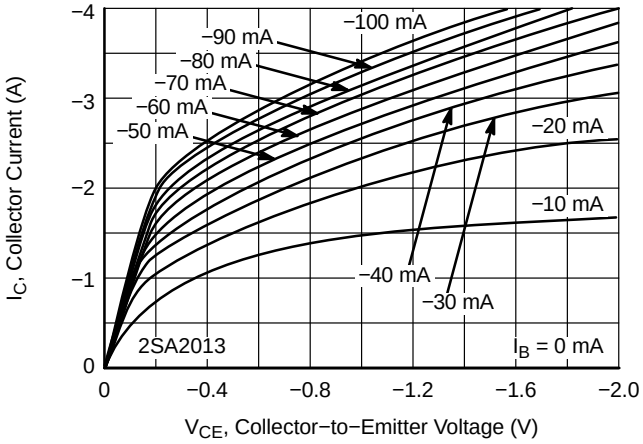


Figure 2. $I_C - V_{CE}$

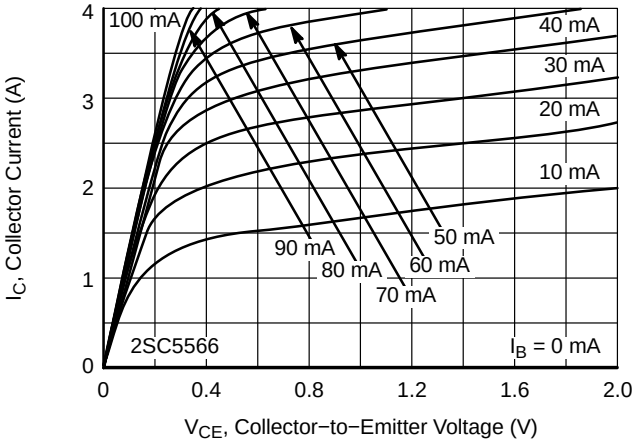


Figure 3. $I_C - V_{CE}$

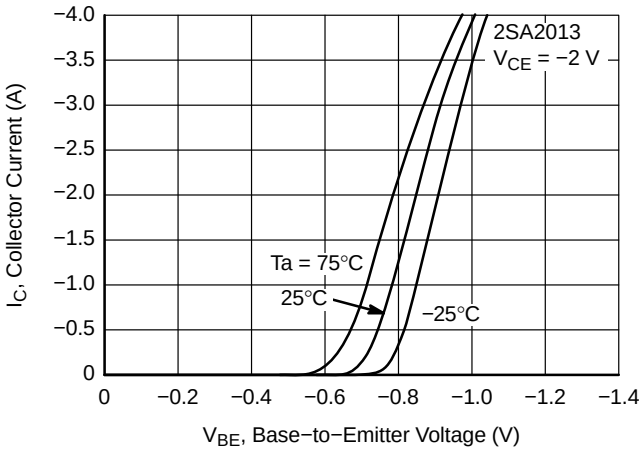


Figure 4. $I_C - V_{BE}$

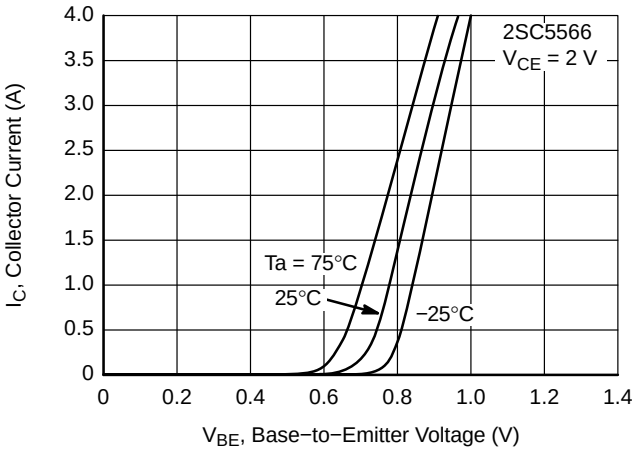


Figure 5. $I_C - V_{BE}$

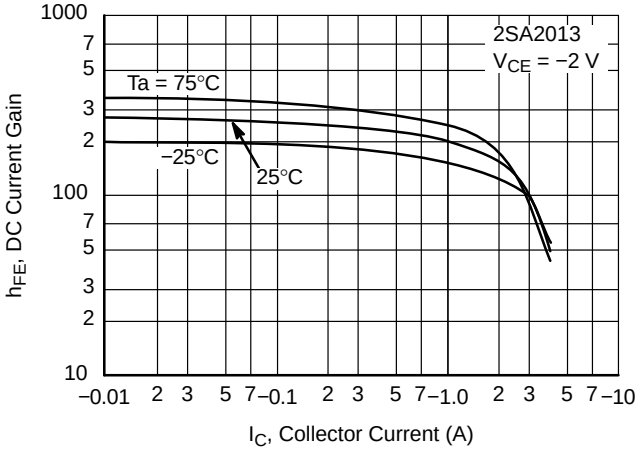


Figure 6. $h_{FE} - I_C$

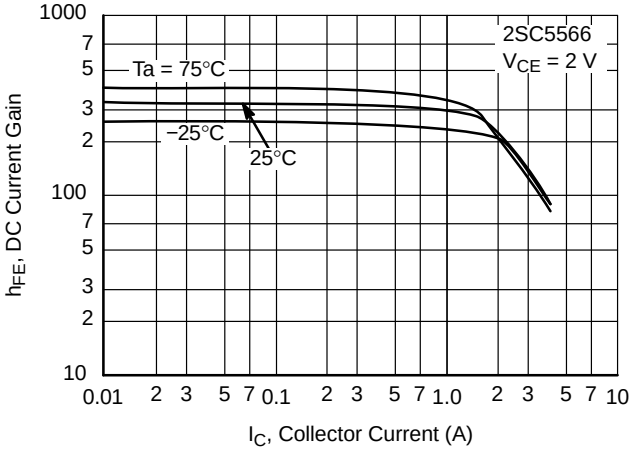


Figure 7. $h_{FE} - I_C$

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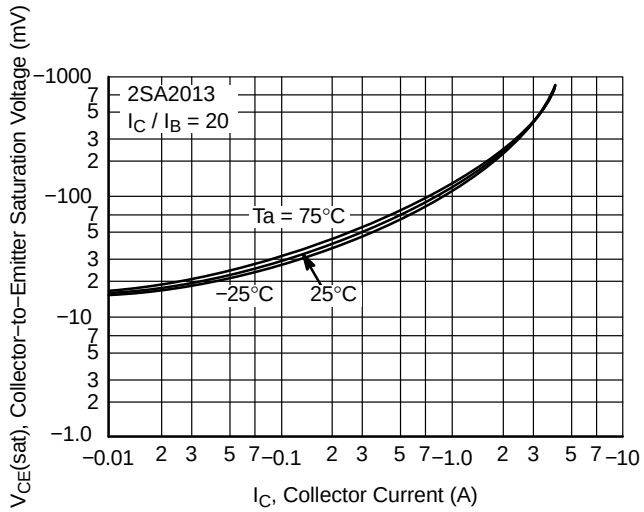


Figure 8. V_{CE}(sat) − I_C

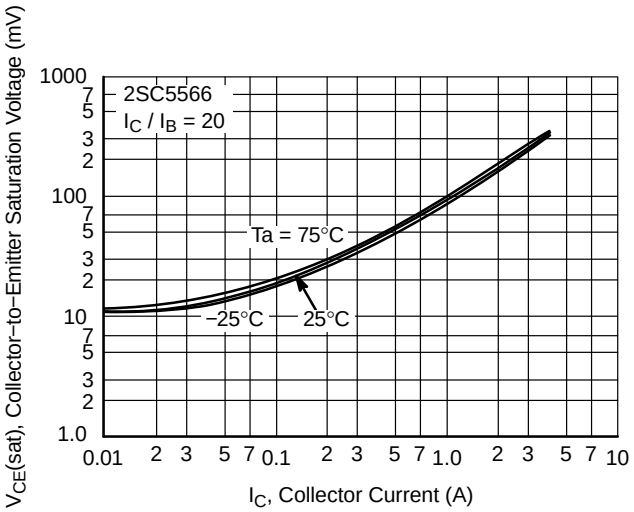


Figure 9. V_{CE}(sat) − I_C

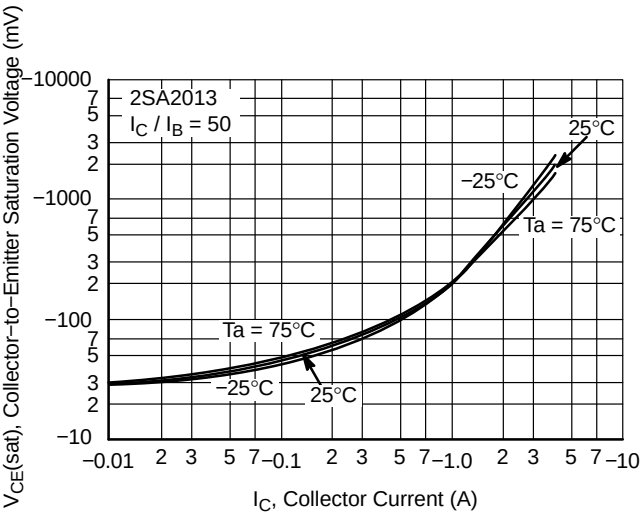


Figure 10. V_{CE}(sat) − I_C

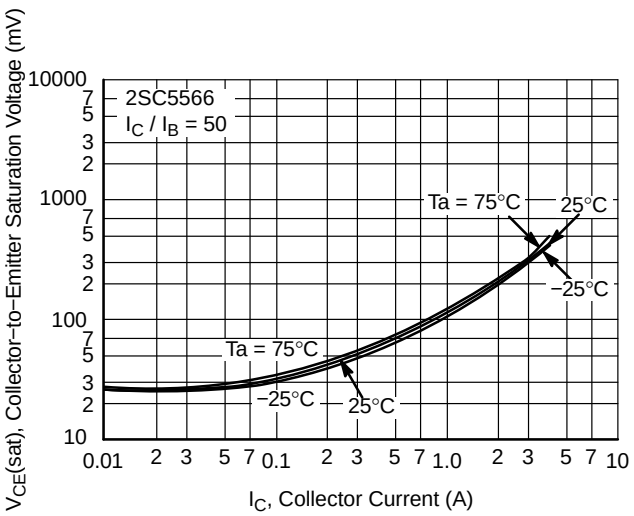


Figure 11. V_{CE}(sat) − I_C

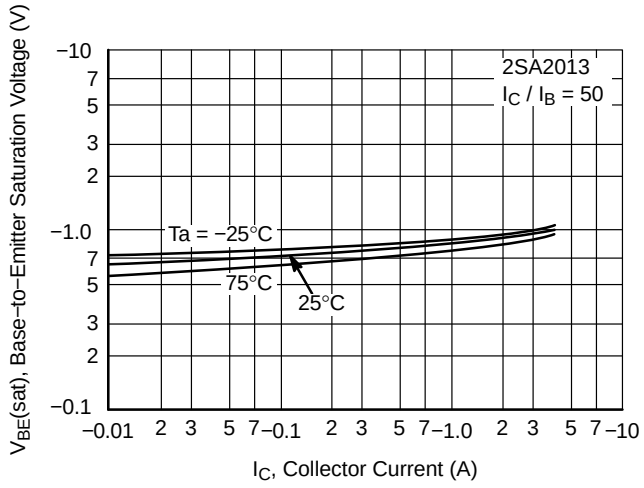


Figure 12. V_{BE}(sat) − I_C

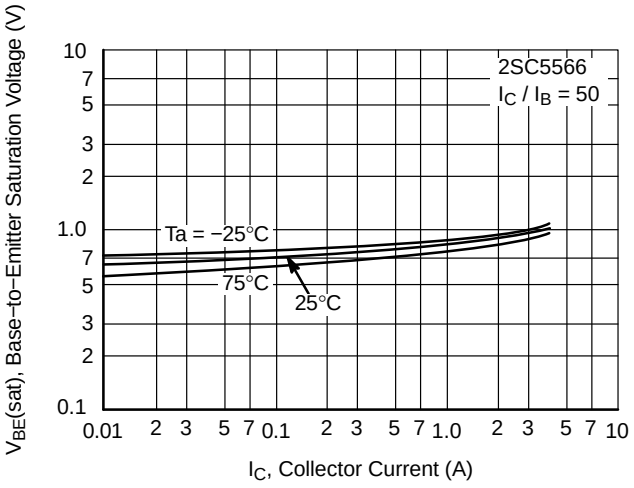


Figure 13. V_{BE}(sat) − I_C

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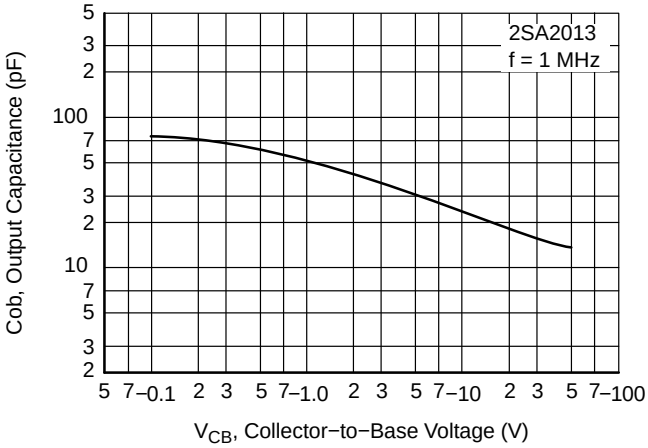


Figure 14. Cob − V_{CB}

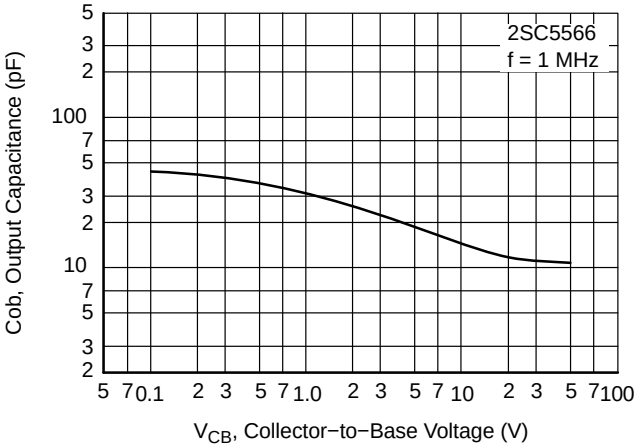


Figure 15. Cob − V_{CB}

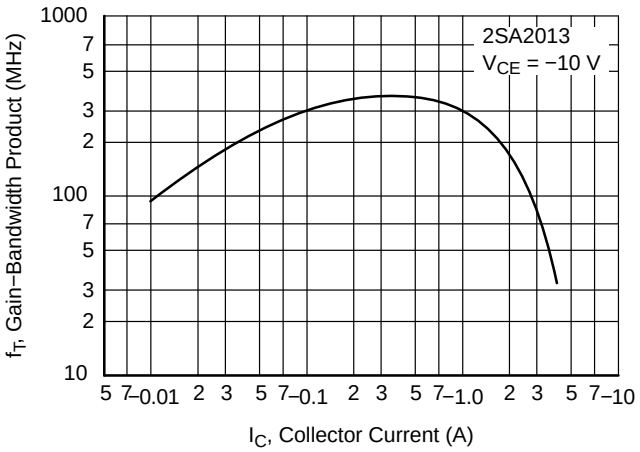


Figure 16. f_T − I_C

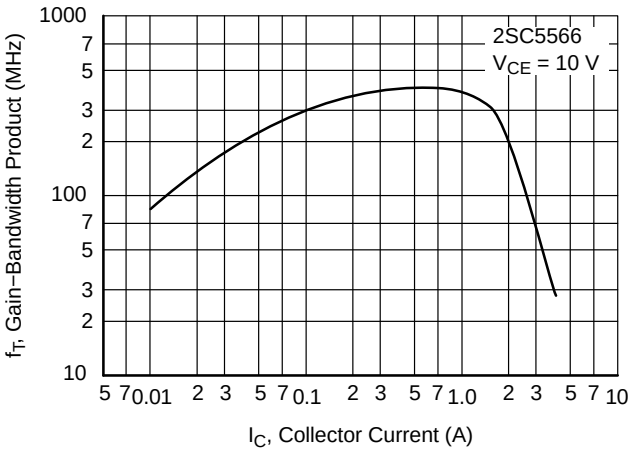


Figure 17. f_T − I_C

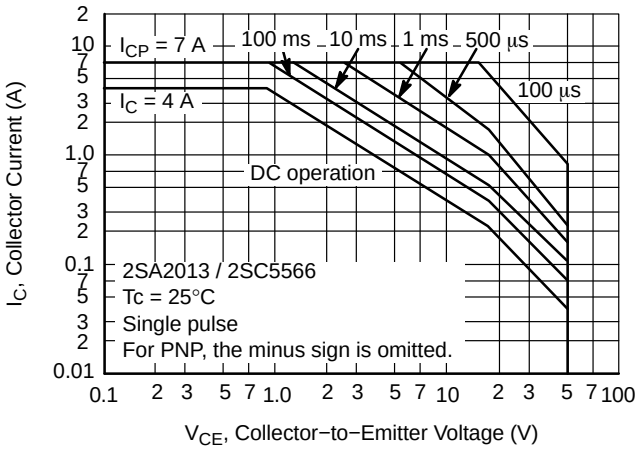


Figure 18. ASO

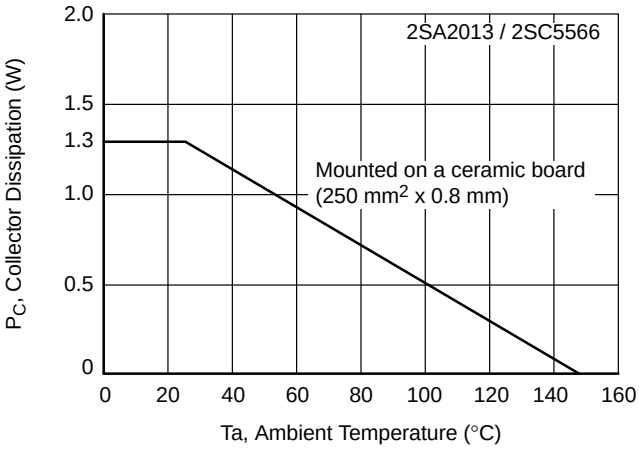


Figure 19. P_C − Ta

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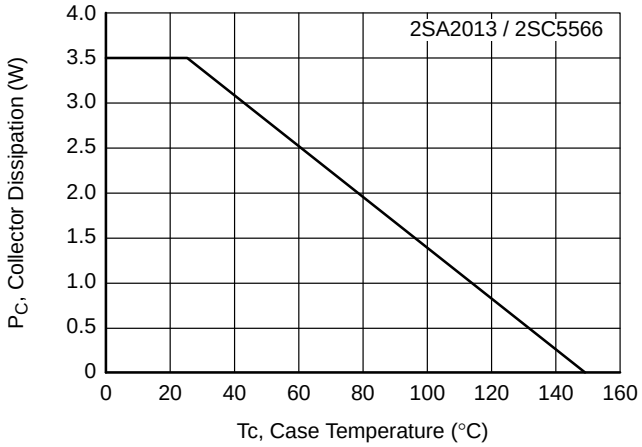
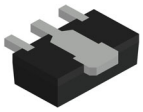


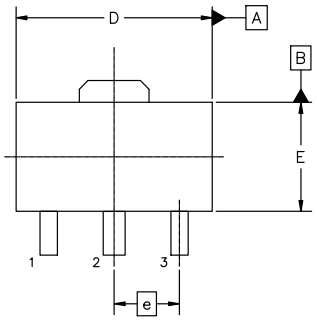
Figure 20. P_C − Tc

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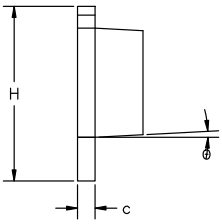


SOT−89 4.50x2.50x1.50 1.50P
CASE 419AU
ISSUE A

DATE 21 MAY 2025



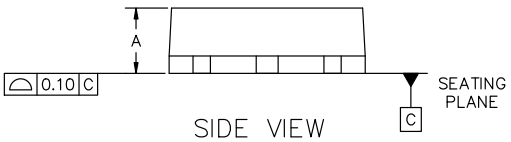
TOP VIEW



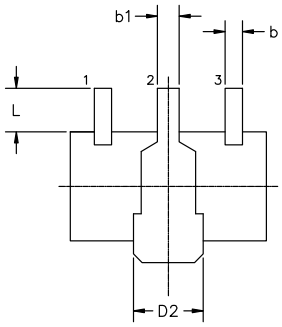
END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS INCLUDES LEAD FINISH.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

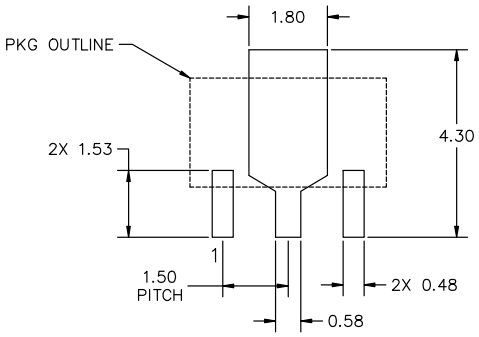
MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.40	1.50	1.60
b	0.35	0.40	0.48
b1	0.40	0.50	0.55
c	0.37	0.40	0.43
D	4.40	4.50	4.60
D2	1.40	1.60	1.80
E	2.40	2.50	2.60
e	1.50 BSC		
H	3.80	4.00	4.20
L	0.80	1.00	1.20
θ	0°	−−−	3°



SIDE VIEW



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**SOT−89 4.50x2.50x1.50 1.50P**		**PAGE 1 OF 1**

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