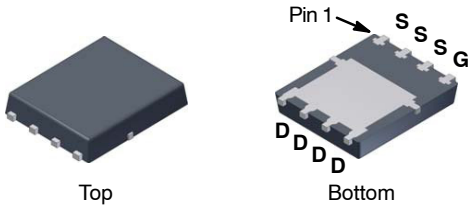
MOSFET – N-Channel, POWERTRENCH®, Shielded Gate

150 V, 16 A, 51 mΩ

FDMS86252, FDMS86252-NC

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
150 V	51 mΩ @ 10 V	16 A
	70 mΩ @ 6 V	



PQFN8 5 × 6, 1.27P
(Power 56)
CASE 483AE

General Description

This N-Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

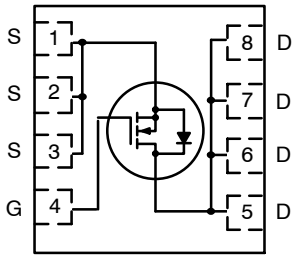
Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 51 mΩ at V_{GS} = 10 V, I_D = 4.6 A
- Max $R_{DS(on)}$ = 70 mΩ at V_{GS} = 6 V, I_D = 3.9 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

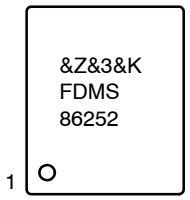
Applications

- DC-DC Conversion

ELECTRICAL CONNECTION



MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3-Digit Date Code (Year and Week)
&K	= 2-Digit Lot Run Code
FDMS86252	= Specific Device Code

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: – Continuous (T_C = 25 °C) – Continuous (T_A = 25 °C (Note 1a)) – Pulsed	 16 4.6 20	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	50	mJ
P_D	Power Dissipation: (T_C = 25 °C) (T_A = 25 °C (Note 1a))	 69 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
FDMS86252	PQFN8	3000 / Tape & Reel
FDMS86252-NC		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	150	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25 °C	–	106	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	2.8	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25 °C	–	–9	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4.6 A	–	43.9	51	mΩ
		V_{GS} = 6 V, I_D = 3.9 A	–	50.5	70	
		V_{GS} = 10 V, I_D = 4.6 A, T_J = 125 °C	–	83	96	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.6 A	–	15	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 75 V, V_{GS} = 0 V, f = 1 MHz	–	678	905	pF
C_{oss}	Output Capacitance		–	74	115	pF
C_{rss}	Reverse Transfer Capacitance		–	4.3	10	pF
R_g	Gate Resistance		0.1	0.4	1.8	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 75 V, I_D = 4.6 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	7.7	16	ns
t_r	Rise Time		–	2.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	15	27	ns
t_f	Fall Time		–	3.2	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 75 V, I_D = 4.6 A	–	11	15	nC
		V_{GS} = 0 V to 5 V, V_{DD} = 75 V, I_D = 4.6 A	–	6.1	8.6	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 75 V, I_D = 4.6 A	–	2.8	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 75 V, I_D = 4.6 A	–	2.4	–	nC

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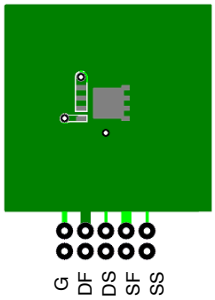
ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.75	1.2	V
		V_{GS} = 0 V, I_S = 4.6 A (Note 2)	–	0.80	1.3	
t_{rr}	Reverse Recovery Time	I_F = 4.6 A, di/dt = 100 A/μs	–	56	90	ns
Q_{rr}	Reverse Recovery Charge		–	61	98	nC

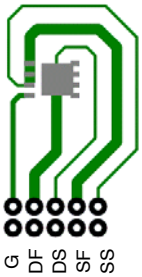
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25 °C, L = 1 mH, I_{AS} = 10 A, V_{DD} = 135 V, V_{GS} = 10 V.

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TYPICAL CHARACTERISTICS

(T_J = 25 °C unless otherwise noted)

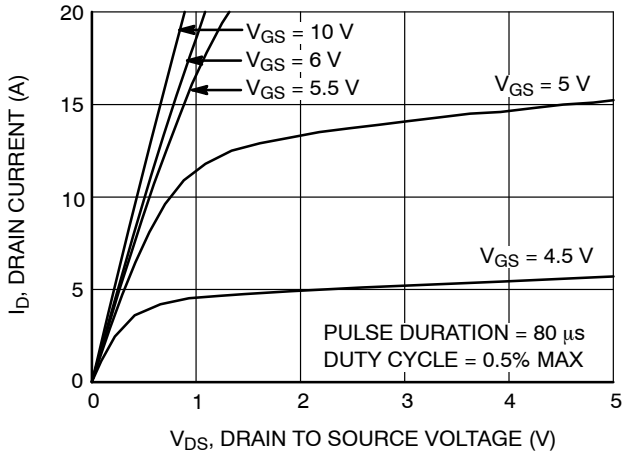


Figure 1. On Region Characteristics

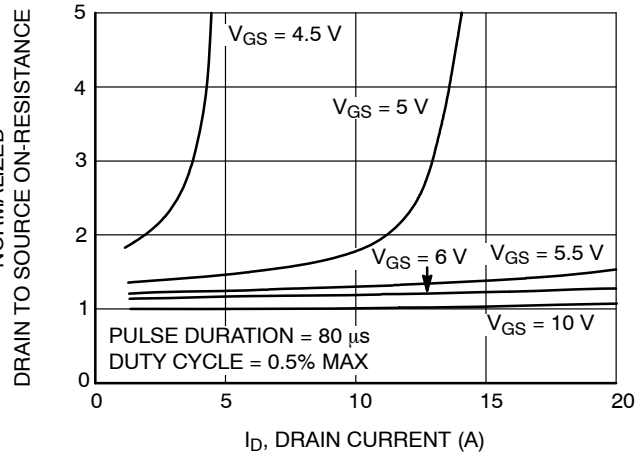


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

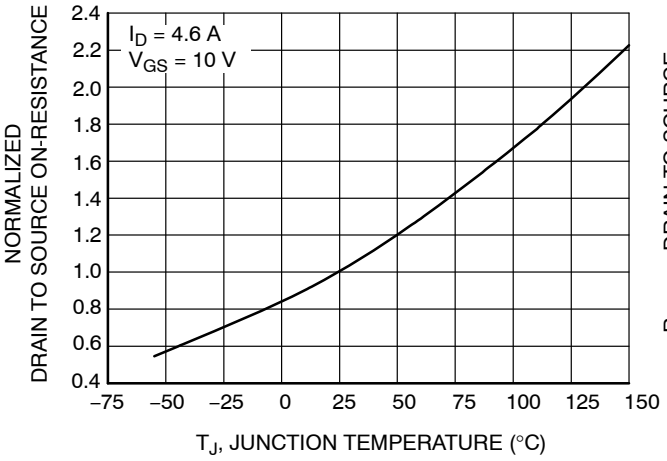


Figure 3. Normalized On Resistance vs. Junction Temperature

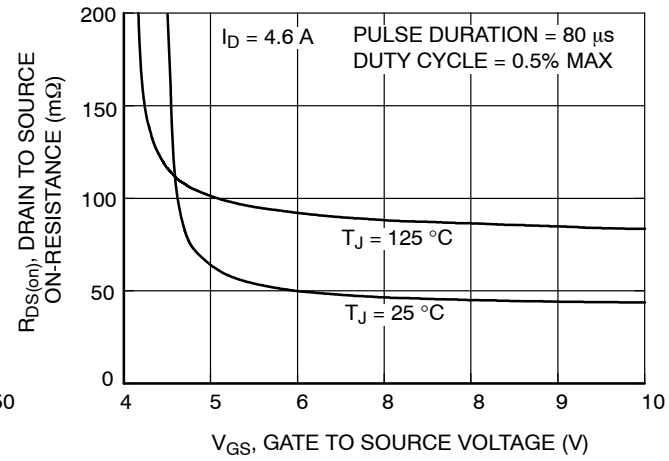


Figure 4. On-Resistance vs. Gate to Source Voltage

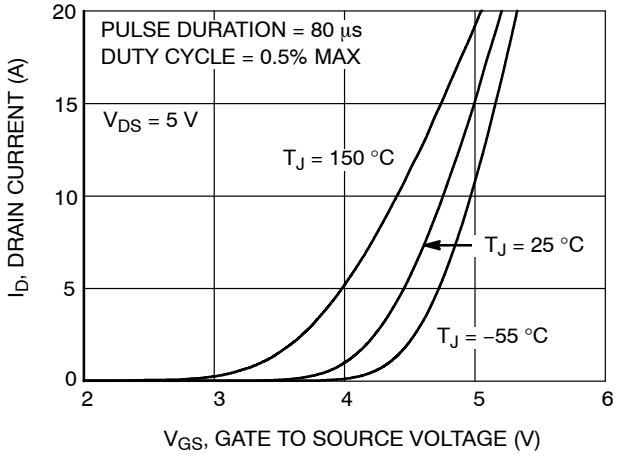


Figure 5. Transfer Characteristics

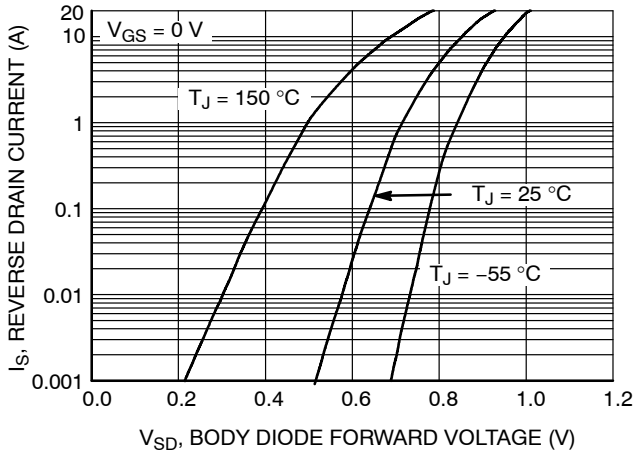


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS (continued)

(T_J = 25 °C unless otherwise noted)

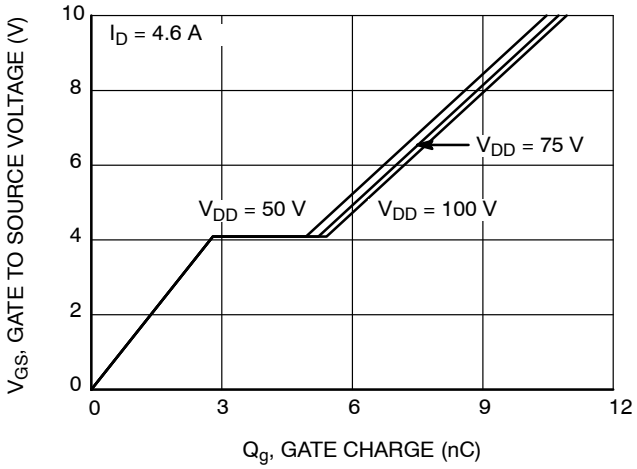


Figure 7. Gate Charge Characteristics

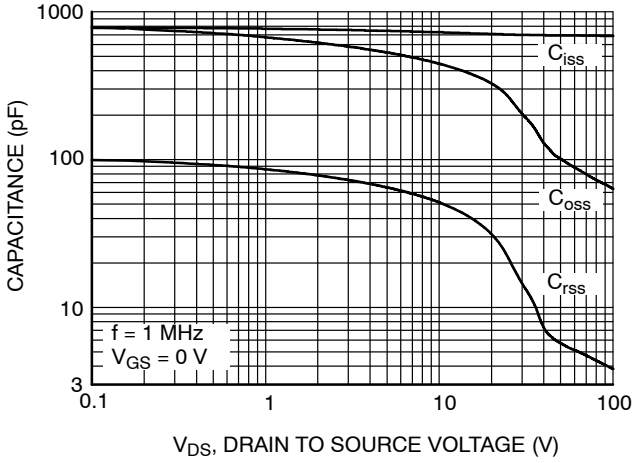


Figure 8. Capacitance vs. Drain to Source Voltage

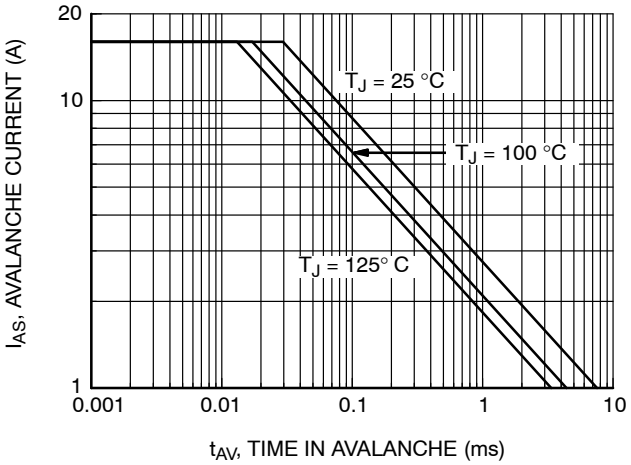


Figure 9. Unclamped Inductive Switching Capability

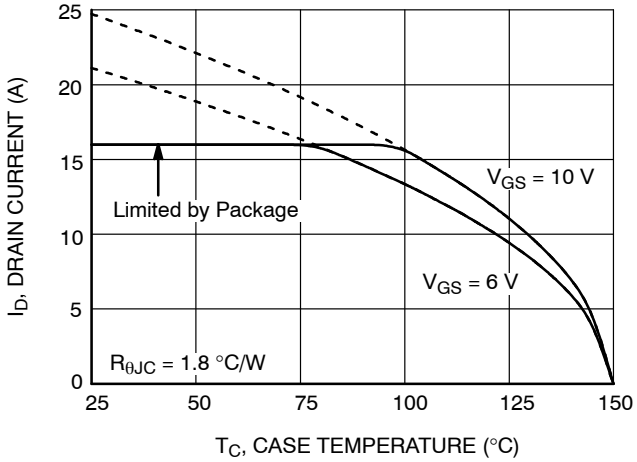


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

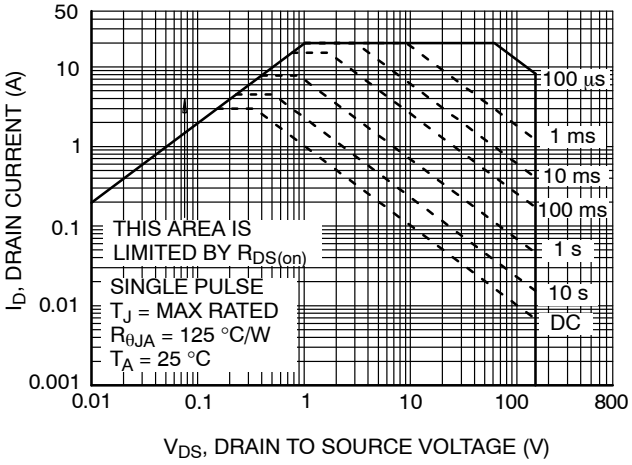


Figure 11. Forward Bias Safe Operating Area

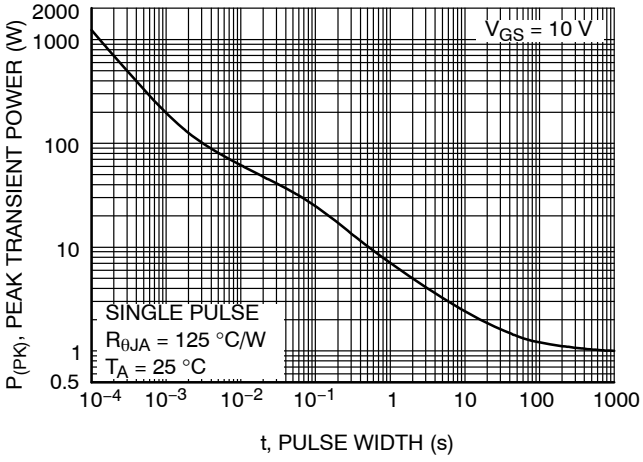


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (continued)

(T_J = 25 °C unless otherwise noted)

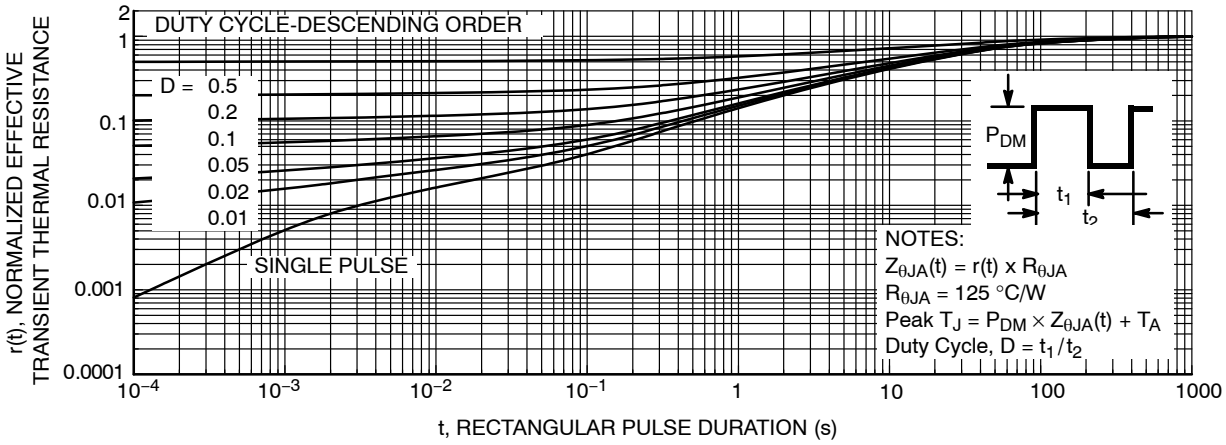


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

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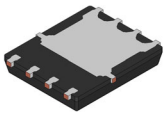
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REVISION HISTORY

Revision	Description of Changes	Date
3	Document converted to **onsemi** format. Added new OPN FDMS86252-NC.	4/22/2026

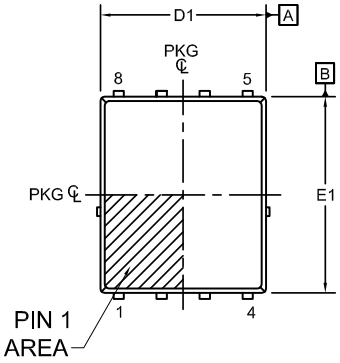
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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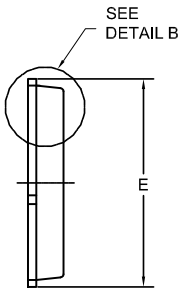


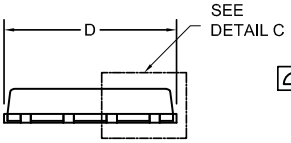
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CASE 483AE
ISSUE C

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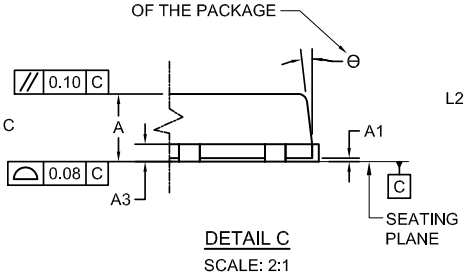


TOP VIEW

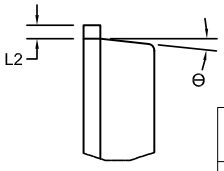




SIDE VIEW



DETAIL C
SCALE: 2:1

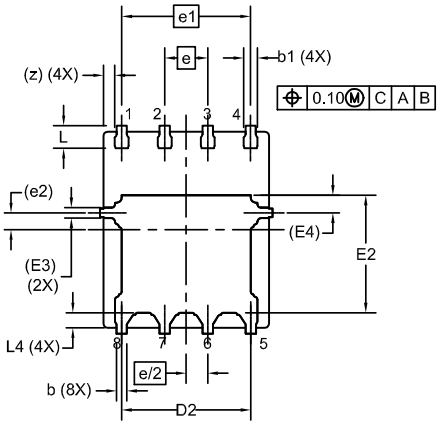


DETAIL B
SCALE: 2:1

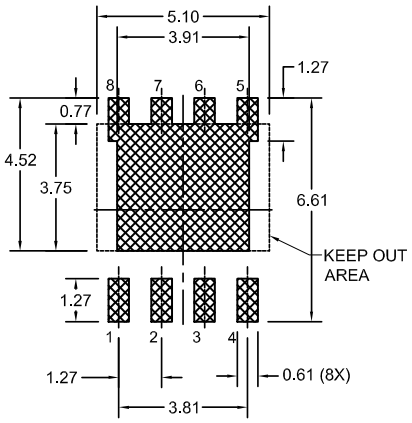
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

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DESCRIPTION:	**PQFN8 5X6, 1.27P**		**PAGE 1 OF 1**

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