# TinyLogic UHS Two-Input NOR Gate

# NC7SZ02

### Description

The NC7SZ02 is a single two−input NOR gate from **onsemi**'s Ultra−High Speed (UHS) series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra−high speed with high output drive while maintaining low static power dissipation over a broad $V_{CC}$ operating range. The device is specified to operate over the 1.65 V to 5.5 V $V_{CC}$ operating range. The inputs and output are high−impedance when $V_{CC}$ is 0 V. Inputs tolerate voltages up to 5.5 V, independent of $V_{CC}$ operating range.

### Features

- Ultra−High Speed: $t_{PD}$ = 2.4 ns (Typical) into 50 pF at 5 V $V_{CC}$
- High Output Drive: ±24 mA at 3 V $V_{CC}$
- Broad $V_{CC}$ Operating Range: 1.65 V to 5.5 V
- Matches Performance of LCX Operated at 3.3 V $V_{CC}$
- Power Down High−Impedance Inputs / Outputs
- Over−Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry
- Ultra−Small MicroPak™ Packages
- Space−Saving SOT23−5, SC−74A and SC−88A Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

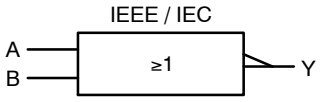
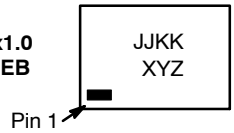



**Figure 1. Logic Symbol**

## MARKING DIAGRAMS

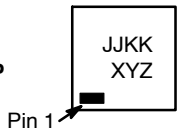


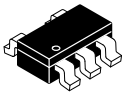
**SIP6 1.45x1.0**
**CASE 127EB**



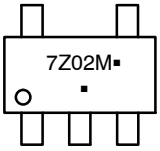


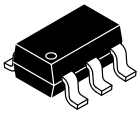

**UDFN6**
**1.0X1.0, 0.35P**
**CASE 517DP**



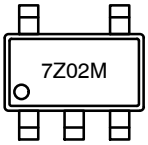



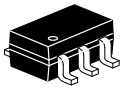
**SC−74A**
**CASE 318BQ**



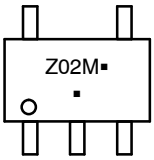



**SOT23−5**
**CASE 527AH**



**SC−88A**
**CASE 419A−02**




| | |
|---|---|
| JJ, 7Z02, Z02 | = Specific Device Code |
| KK | = 2−Digit Lot Run Traceability Code |
| XY | = 2−Digit Date Code Format |
| Z | = Assembly Plant Code |
| M | = Date Code* |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

* Date Code orientation and/or position may vary depending upon manufacturing location.

## ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

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## Pin Configurations

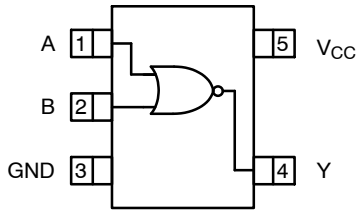



**Figure 2. SOT23−5, SC−88A and SC−74A (Top View)**

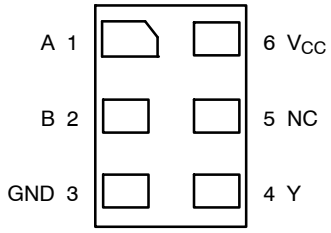



**Figure 3. MicroPak (Top Through View)**

### PIN DEFINITIONS

| Pin # SOT23−5, SC−88A / SC74A | Pin # MicroPak | Name | Description |
|---|---|---|---|
| 1 | 1 | A | Input |
| 2 | 2 | B | Input |
| 3 | 3 | GND | Ground |
| 4 | 4 | Y | Output |
| 5 | 6 | $V_{CC}$ | Supply Voltage |
| | 5 | NC | No Connect |

### FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = HIGH Logic Level
L = LOW Logic Level

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | −0.5 | 6.5 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 | 6.5 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 | 6.5 | V |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < 0 V | − | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < 0 V | − | −50 | mA |
| $I_{OUT}$ | DC Output Current | | − | ±50 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | | − | ±50 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 | +150 | °C |
| $T_J$ | Junction Temperature Under Bias | | − | +150 | °C |
| $T_L$ | Junction Lead Temperature (Soldering, 10 Seconds) | | − | +260 | °C |
| $P_D$ | Power Dissipation in Still Air | SC−74A / SOT23−5 | − | 390 | mW |
| | | SC−88A | − | 332 | |
| | | MicroPak−6 | − | 812 | |
| | | MicroPak2™−6 | − | 812 | |
| ESD | Human Body Model, JEDEC: JESD22−A114 | | − | 4000 | V |
| | Charge Device Model, JEDEC: JESD22−C101 | | − | 2000 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage Operating | | 1.65 | 5.5 | V |
| | Supply Voltage Data Retention | | 1.5 | 5.5 | |



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## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | Output Voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature | | −40 | +85 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Times | $V_{CC}$ at 1.8 V, 2.5 V ±0.2 V | 0 | 20 | ns/V |
| | | $V_{CC}$ at 3.3 V ±0.3 V | 0 | 10 | |
| | | $V_{CC}$ at 5.0 V ±0.5 V | 0 | 5 | |
| $\theta_{JA}$ | Thermal Resistance | SC−74A / SOT23−5 | – | 320 | °C/W |
| | | SC−88A | – | 377 | |
| | | MicroPak−6 | – | 154 | |
| | | MicroPak2−6 | – | 154 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.



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## DC ELECTICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = +25°C | | | $T_A$ = −40 to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | 1.65 to 1.95 | | 0.65 $V_{CC}$ | – | – | 0.65 $V_{CC}$ | – | V |
| | | 2.30 to 5.50 | | 0.70 $V_{CC}$ | – | – | 0.70 $V_{CC}$ | – | |
| $V_{IL}$ | LOW Level Input Voltage | 1.65 to 1.95 | | – | – | 0.35 $V_{CC}$ | – | 0.35 $V_{CC}$ | V |
| | | 2.30 to 5.50 | | – | – | 0.30 $V_{CC}$ | – | 0.30 $V_{CC}$ | |
| $V_{OH}$ | HIGH Level Output Voltage | 1.65 | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = −100 μA | 1.55 | 1.65 | – | 1.55 | – | V |
| | | 1.80 | | 1.70 | 1.80 | – | 1.70 | – | |
| | | 2.30 | | 2.20 | 2.30 | – | 2.20 | – | |
| | | 3.00 | | 2.90 | 3.00 | – | 2.90 | – | |
| | | 4.50 | | 4.40 | 4.50 | – | 4.40 | – | |
| | | 1.65 | $I_{OH}$ = −4 mA | 1.29 | 1.52 | – | 1.29 | – | |
| | | 2.30 | $I_{OH}$ = −8 mA | 1.90 | 2.15 | – | 1.90 | – | |
| | | 3.00 | $I_{OH}$ = −16 mA | 2.40 | 2.80 | – | 2.40 | – | |
| | | 3.00 | $I_{OH}$ = −24 mA | 2.30 | 2.68 | – | 2.30 | – | |
| | | 4.50 | $I_{OH}$ = −32 mA | 3.80 | 4.20 | – | 3.80 | – | |
| $V_{OL}$ | LOW Level Output Voltage | 1.65 | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 100 μA | – | 0.00 | 0.10 | – | 0.10 | V |
| | | 1.80 | | – | 0.00 | 0.10 | – | 0.10 | |
| | | 2.30 | | – | 0.00 | 0.10 | – | 0.10 | |
| | | 3.00 | | – | 0.00 | 0.10 | – | 0.10 | |
| | | 4.50 | | – | 0.00 | 0.10 | – | 0.10 | |
| | | 1.65 | $I_{OL}$ = 4 mA | – | 0.08 | 0.24 | – | 0.24 | |
| | | 2.30 | $I_{OL}$ = 8 mA | – | 0.10 | 0.30 | – | 0.30 | |
| | | 3.00 | $I_{OL}$ = 16 mA | – | 0.15 | 0.40 | – | 0.40 | |
| | | 3.00 | $I_{OL}$ = 24 mA | – | 0.22 | 0.55 | – | 0.55 | |
| | | 4.50 | $I_{OL}$ = 32 mA | – | 0.22 | 0.55 | – | 0.55 | |
| $I_{IN}$ | Input Leakage Current | 1.65 to 5.50 | $V_{IN}$ = 5.5 V, GND | – | – | ±1 | – | ±10 | μA |
| $I_{OFF}$ | Power Off Leakage Current | 0 | $V_{IN}$ or $V_{OUT}$ = 5.5 V | – | – | 1 | – | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | 1.65 to 5.50 | $V_{IN}$ = 5.5 V, GND | – | – | 2.0 | – | 20 | μA |



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## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = +25°C | | | $T_A$ = −40 to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay (Figure 4, 5) | 1.65 | $C_L$ = 15 pF, $R_L$ = 1 MΩ | – | 5.3 | 11.5 | – | 12.0 | ns |
| | | 1.80 | | – | 4.4 | 9.5 | – | 10.0 | |
| | | 2.50 ±0.20 | | – | 2.9 | 6.5 | – | 7.0 | |
| | | 3.30 ±0.30 | | – | 2.3 | 4.5 | – | 4.7 | |
| | | 5.00 ±0.50 | | – | 1.9 | 3.9 | – | 4.1 | |
| | | 3.30 ±0.30 | $C_L$ = 50 pF, $R_L$ = 500 Ω | – | 2.9 | 5.0 | – | 5.2 | |
| | | 5.00 ±0.50 | | – | 2.4 | 4.3 | – | 4.5 | |
| $C_{IN}$ | Input Capacitance | 0 | | – | 4 | – | – | – | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 2) (Figure 6) | 3.30 | | – | 23 | – | – | – | pF |
| | | 5.00 | | – | 30 | – | – | – | |

2. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading and operating at 50% duty cycle. $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

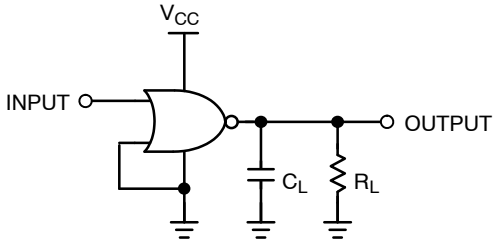



**Figure 4. AC Test Circuit**

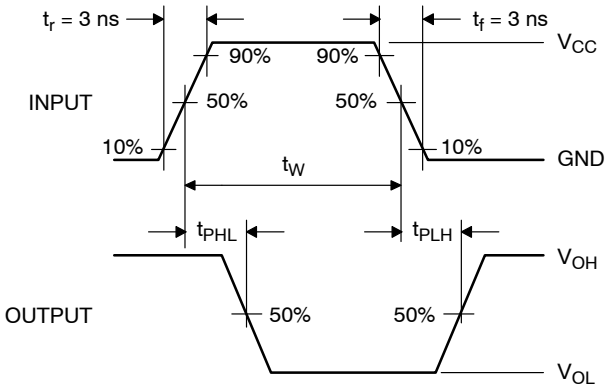
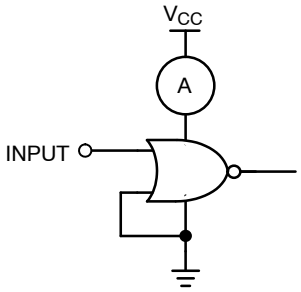



**Figure 5. AC Waveforms**




NOTE:
3. Input = AC Waveform; $t_r = t_f$ = 1.8 ns; PRR = 10 MHz; Duty Cycle = 50%.

**Figure 6. $I_{CC}$D Test Circuit**



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## ORDERING INFORMATION

| Part Number | Top Mark | Packages | Shipping† |
|---|---|---|---|
| NC7SZ02M5X | 7Z02 | SC−74A | 3000 / Tape & Reel |
| NC7SZ02P5X | Z02 | SC−88A | 3000 / Tape & Reel |
| NC7SZ02L6X | JJ | SIP6, MicroPak | 5000 / Tape & Reel |
| NC7SZ02FHX | JJ | UDFN6, MicroPak2 | 5000 / Tape & Reel |

**DISCONTINUED** (Note 4)

| | | | |
|---|---|---|---|
| NC7SZ02M5X−L22090 | 7Z02 | SOT23−5 | 3000 / Tape & Reel |
| NC7SZ02L6X−L22175 | JJ | SIP6, MicroPak | 5000 / Tape & Reel |
| NC7SZ02FHX−L22175 | JJ | UDFN6, MicroPak2 | 5000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

4. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

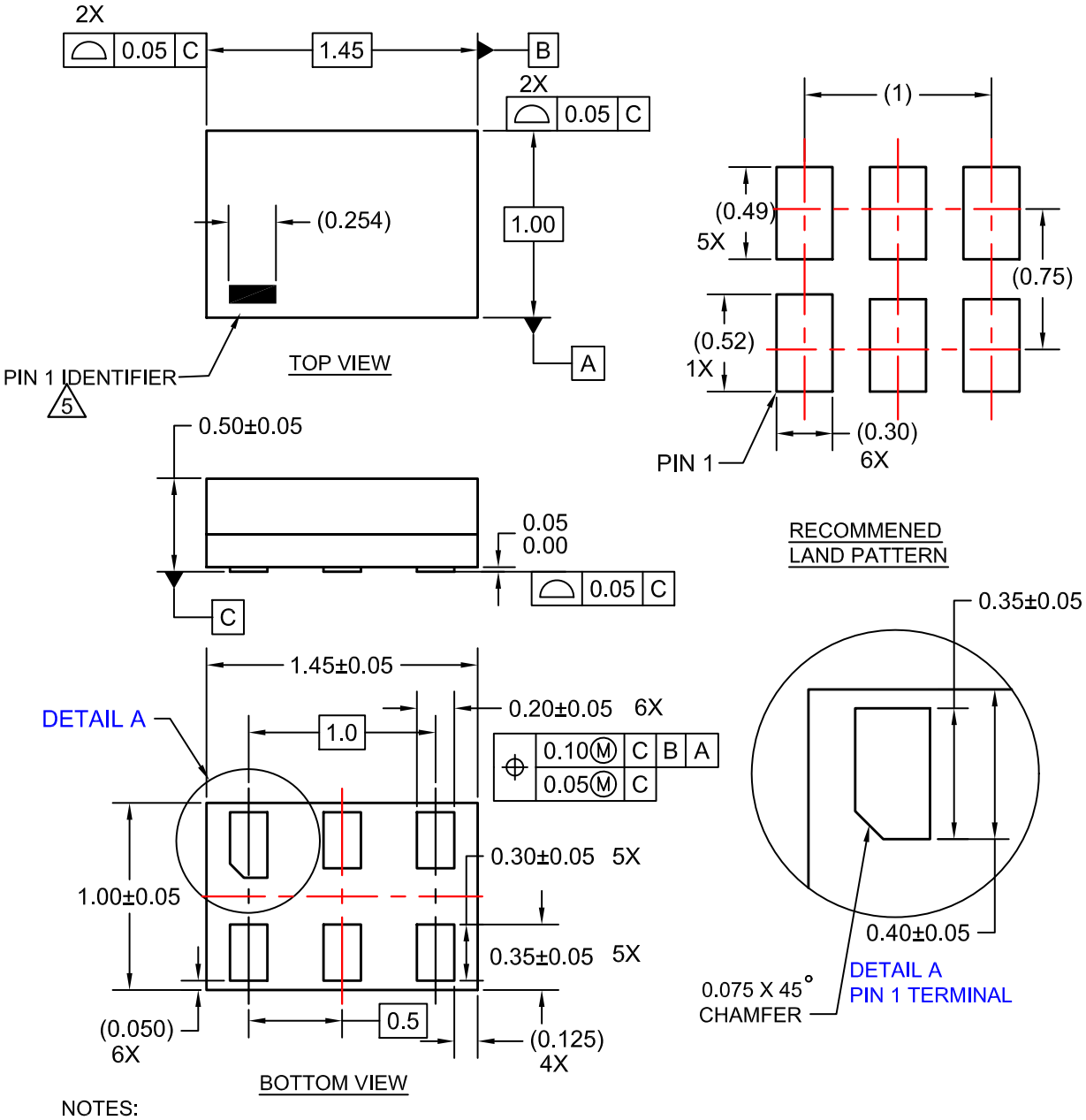
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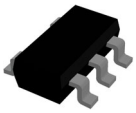



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

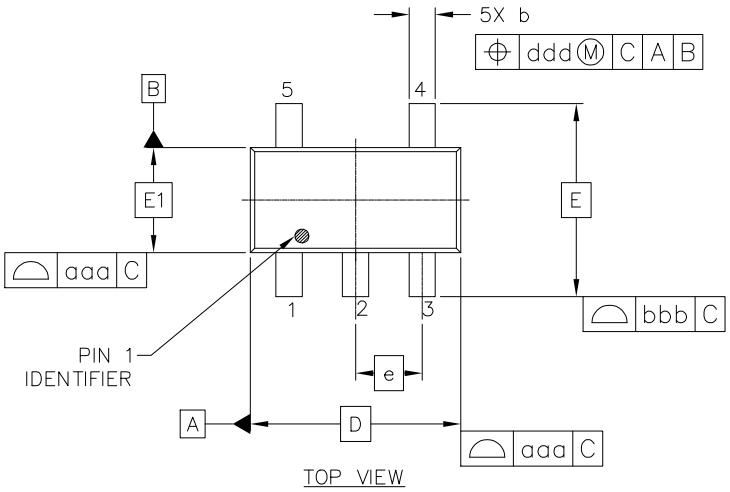
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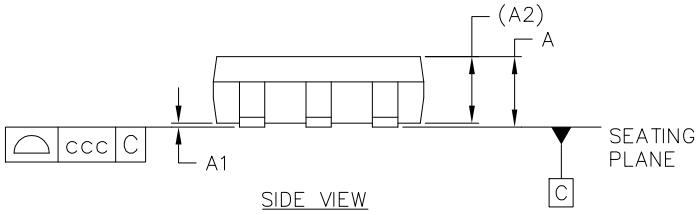
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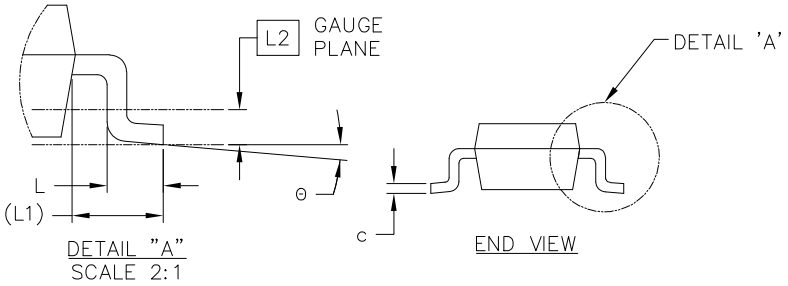


**SC−74A−5 3.00x1.50x0.95, 0.95P**
CASE 318BQ
ISSUE D

DATE 13 APR 2026

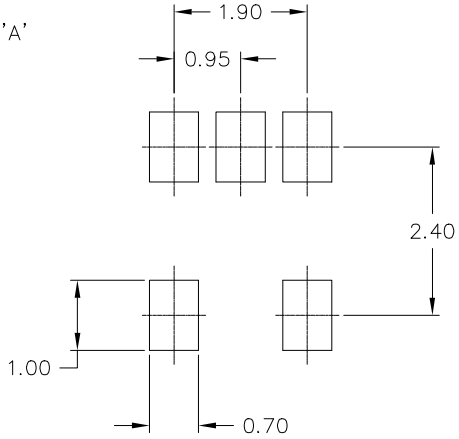


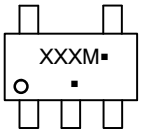

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.01 | 0.05 | 0.10 |
| A2 | | 0.95 REF | |
| b | 0.25 | 0.37 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | | 3.00 BSC | |
| E | | 2.75 BSC | |
| E1 | | 1.50 BSC | |
| e | | 0.95 BSC | |
| L | 0.20 | 0.40 | 0.60 |
| L1 | | 0.60 REF | |
| L2 | | 0.25 BSC | |
| θ | 0° | 5° | 10° |
| TOLERANCE FORM AND POSITION | | | |
| aaa | | 0.15 | |
| bbb | | 0.15 | |
| ccc | | 0.05 | |
| ddd | | 0.20 | |

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.




RECOMMENDED MOUNTING FOOTPRINT
*For additional information in our Pb−Free Strategy and Soldering details, Please download the onsemi Soldering and Mounting Techniques Reference manual. SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

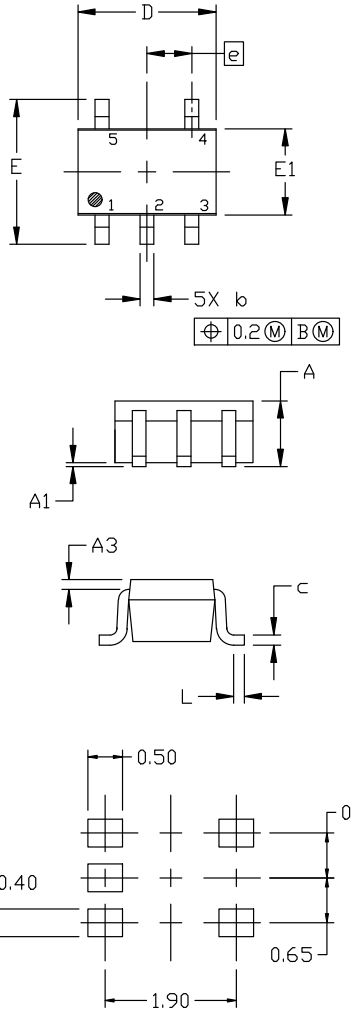
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| **DESCRIPTION:** | **SC−74A−5 3.00x1.50x0.95, 0.95P** | **PAGE 1 OF 1** |

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**SC−88A (SC−70−5/SOT−353)**
CASE 419A−02
ISSUE M

DATE 11 APR 2023

**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

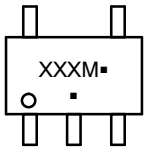
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.95 | 1.10 |
| A1 | --- | --- | 0.10 |
| A3 | 0.20 REF | | |
| b | 0.10 | 0.20 | 0.30 |
| c | 0.10 | --- | 0.25 |
| D | 1.80 | 2.00 | 2.20 |
| E | 2.00 | 2.10 | 2.20 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.10 | 0.15 | 0.30 |




RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

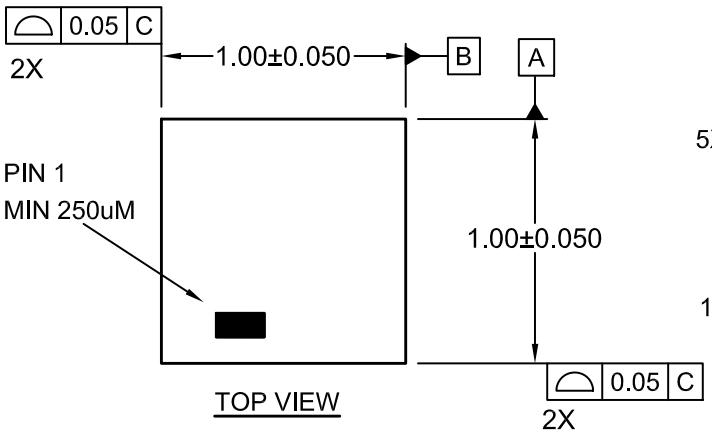
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SC−88A (SC−70−5/SOT−353)** | **PAGE 1 OF 1** |

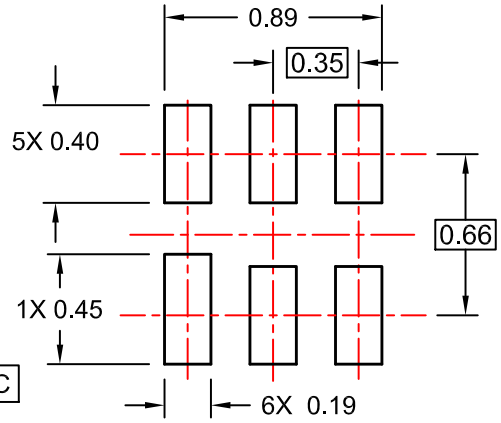
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**UDFN6 1.0X1.0, 0.35P**
CASE 517DP
ISSUE O

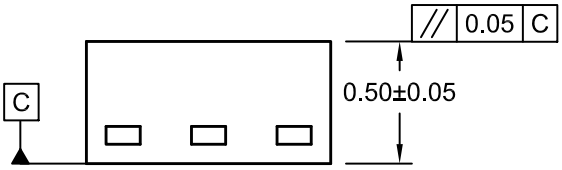
DATE 31 AUG 2016



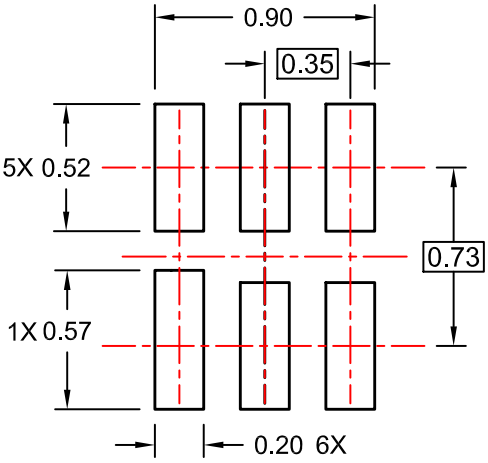

TOP VIEW



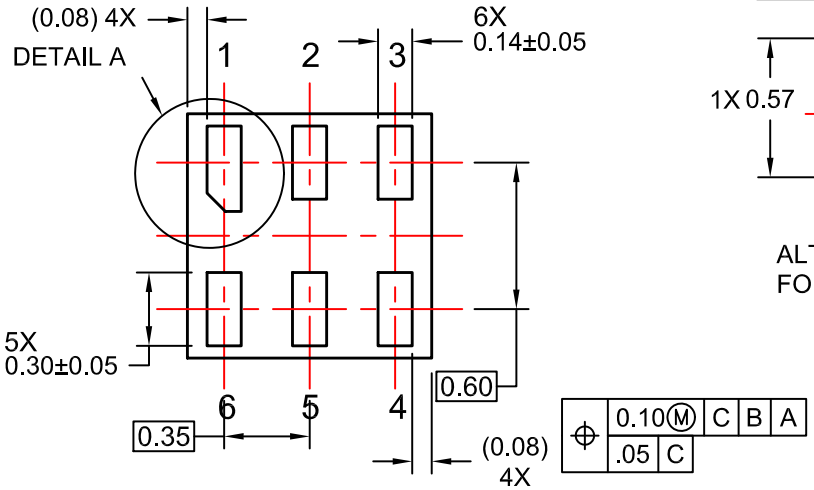

RECOMMENDED LAND PATTERN
FOR SPACE CONSTRAINED PCB



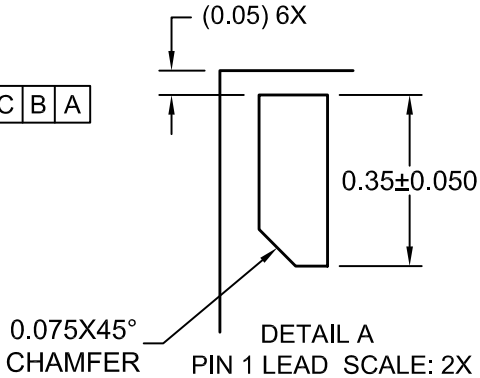

SIDE VIEW




ALTERNATIVE LAND PATTERN
FOR UNIVERSAL APPLICATION




BOTTOM VIEW



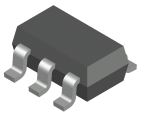

DETAIL A
PIN 1 LEAD SCALE: 2X

NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

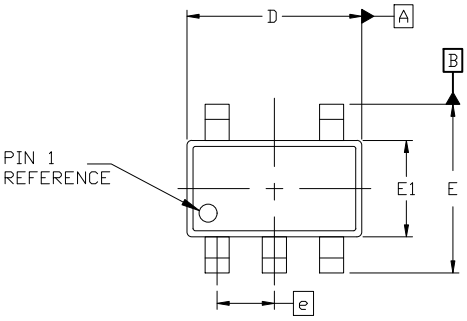
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| **DESCRIPTION:** | **UDFN6 1.0X1.0, 0.35P** | **PAGE 1 OF 1** |

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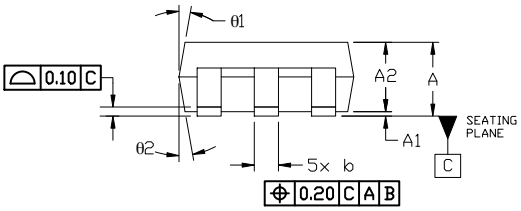


**SOT−23, 5 Lead**
CASE 527AH
ISSUE A

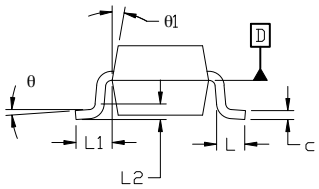
DATE 09 JUN 2021




TOP VIEW




SIDE VIEW

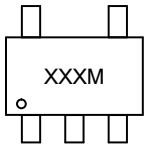



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

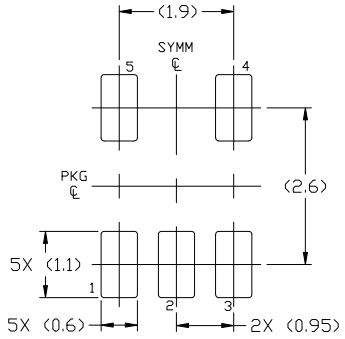
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | — | 1.45 |
| A1 | 0.00 | — | 0.15 |
| A2 | 0.90 | 1.15 | 1.30 |
| b | 0.30 | — | 0.50 |
| c | 0.08 | — | 0.22 |
| D | 2.90 BSC | | |
| E | 2.80 BSC | | |
| E1 | 1.60 BSC | | |
| e | 0.95 BSC | | |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.60 REF | | |
| L2 | 0.25 REF | | |
| θ | 0° | 4° | 8° |
| θ1 | 0° | 10° | 15° |
| θ2 | 0° | 10° | 15° |

## GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.




## RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | | |
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| **DESCRIPTION:** | **SOT−23, 5 LEAD** | | **PAGE 1 OF 1** |

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