MOSFET - Single, P-Channel, Small Signal, Gate Zener, SC-75, SC-89

-20 V, -760 mA

NTA4151P, NTE4151P

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−20 V	0.26 Ω @ −4.5 V	−760 mA
	0.35 Ω @ −2.5 V	
	0.49 Ω @ −1.8 V	

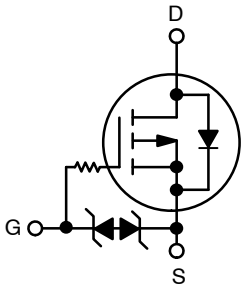
Features

- Low $R_{DS(on)}$ for Higher Efficiency and Longer Battery Life
- Small Outline Package (1.6 x 1.6 mm)
- SC-75 Standard Gullwing Package
- ESD Protected Gate
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Side Load Switch
- DC-DC Conversion
- Small Drive Circuits
- Battery Operated Systems such as Cell Phones, PDAs, Digital Cameras, etc.

P-CHANNEL MOSFET



MAXIMUM RATINGS (T_J = 25 °C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	−20	V
Gate-to-Source Voltage		V_{GS}	±6.0	V
Continuous Drain Current (Note 1)	Steady State	I_D	−760	mA
Power Dissipation (Note 1) SC-75 SC-89	Steady State	P_D	301 313	mW
Pulsed Drain Current	tp =10 μs	I_{DM}	±1000	mA
Operating Junction and Storage Temperature		T_J, T_{STG}	−55 to 150	°C
Continuous Source Current (Body Diode)		I_S	−250	mA
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)		T_L	260	°C
Gate-to-Source ESD Rating – (Human Body Model, Method 3015)		ESD	1800	V

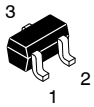
THERMAL RESISTANCE RATINGS

Junction-to-Ambient – Steady State (Note 1) SC-75 SC-89	$R_{\theta JA}$	415 400	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

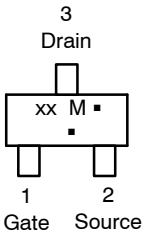
MARKING DIAGRAM & PIN ASSIGNMENT



SC-75 / SOT-416
CASE 463
STYLE 5



SC-89
CASE 463C



xx = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

* Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −16 V		−1.0	−100	nA
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V		±1.0	±10	μA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = −250 μA	−0.45		−1.2	V
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −350 mA		0.26	0.36	Ω
		V_{GS} = −2.5 V, I_D = −300 mA		0.35	0.45	
		V_{GS} = −1.8 V, I_D = −150 mA		0.49	1.0	
Forward Transconductance	g_{FS}	V_{DS} = −10 V, I_D = −250 mA		0.4		S
CHARGES AND CAPACITANCES						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −5.0 V		156		pF
Output Capacitance	C_{OSS}			28		
Reverse Transfer Capacitance	C_{RSS}			18		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −0.3 A		2.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.125		
Gate-to-Source Charge	Q_{GS}			0.325		
Gate-to-Drain Charge	Q_{GD}			0.5		
SWITCHING CHARACTERISTICS (Note 3)						
Turn-On Delay Time	$td_{(ON)}$	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −200 mA, R_G = 10 Ω		8.0		ns
Rise Time	t_r			8.2		
Turn-Off Delay Time	$td_{(OFF)}$			29		
Fall Time	t_f			20.4		
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −250 mA		−0.72	−1.1	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTA4151PT1G	TN	SC-75 (Pb-Free)	3000 / Tape & Reel
NTE4151PT1G	TM	SC-89 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL ELECTRICAL CHARACTERISTICS

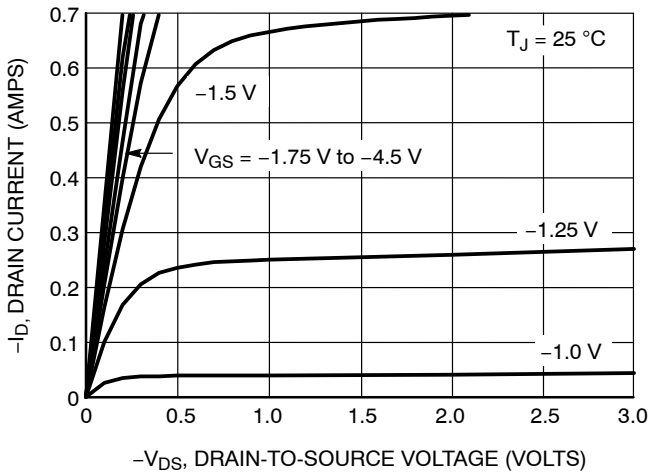


Figure 1. On-Region Characteristics

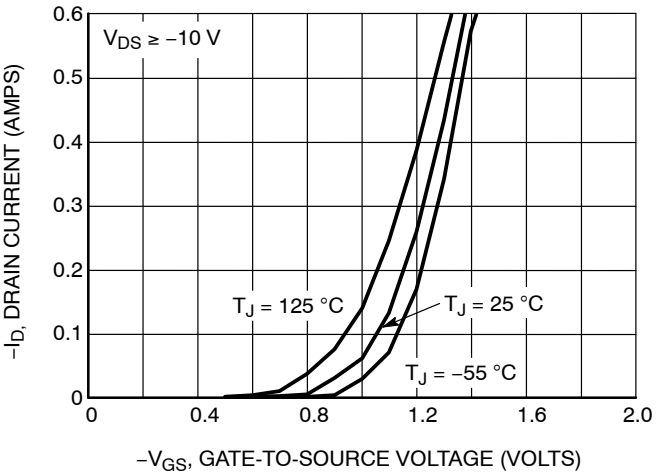


Figure 2. Transfer Characteristics

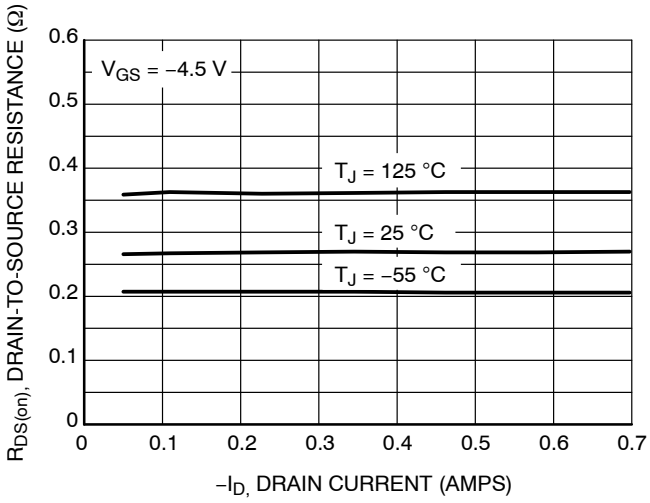


Figure 3. On-Resistance vs. Drain Current and Temperature

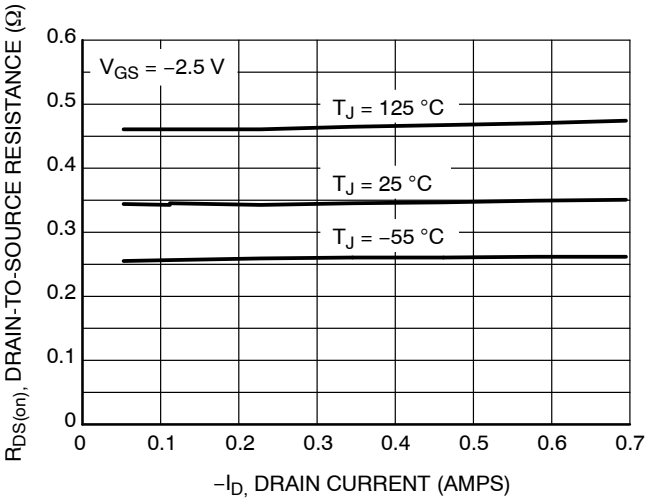


Figure 4. On-Resistance vs. Drain Current and Temperature

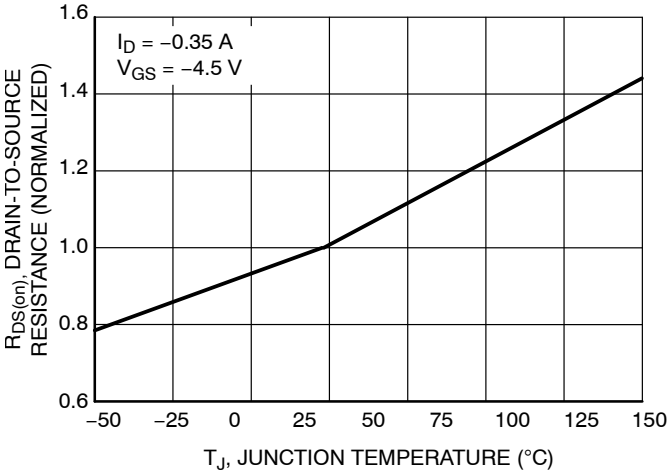


Figure 5. On-Resistance Variation with Temperature

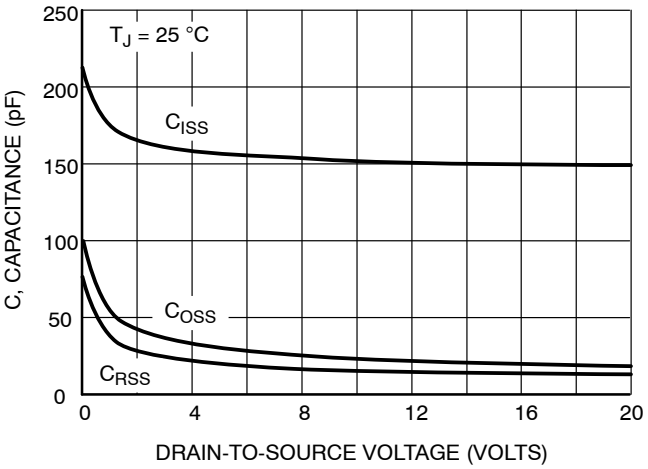


Figure 6. Capacitance Variation

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Your Opinion Matters

TYPICAL ELECTRICAL CHARACTERISTICS

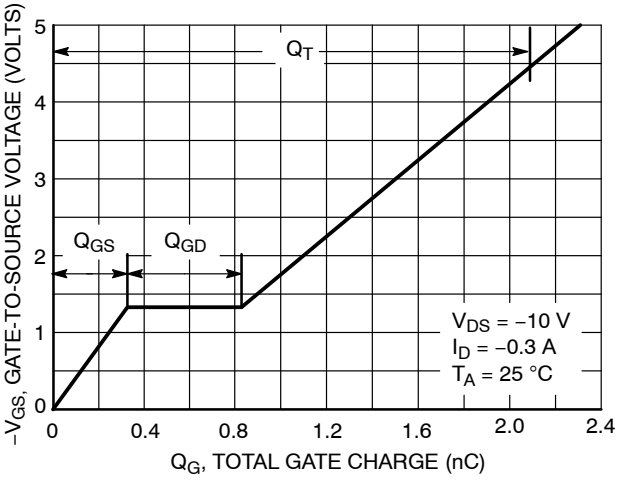


Figure 7. Gate-to-Source Voltage vs. Total Gate Charge

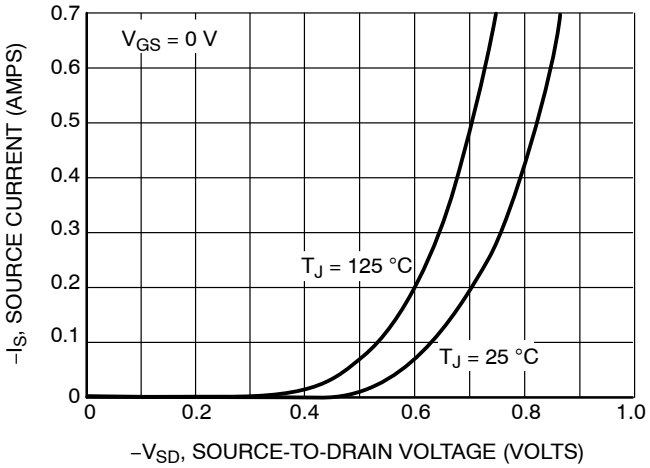


Figure 8. Diode Forward Voltage vs. Current

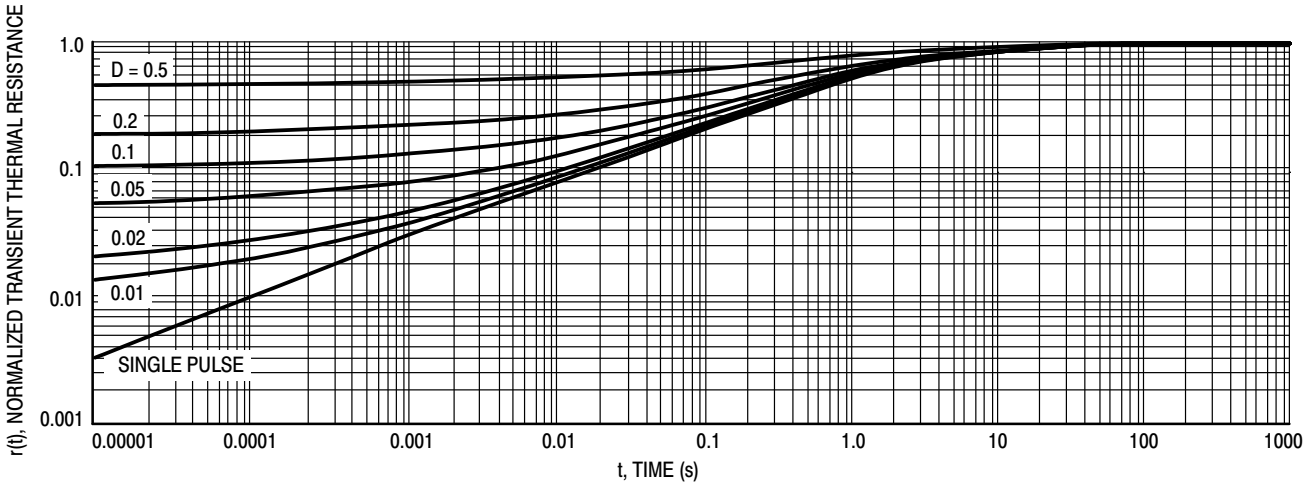


Figure 9. Normalized Thermal Response

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REVISION HISTORY

Revision	Description of Changes	Date
9	Rebranded the Data Sheet to **onsemi** format.	10/29/2025

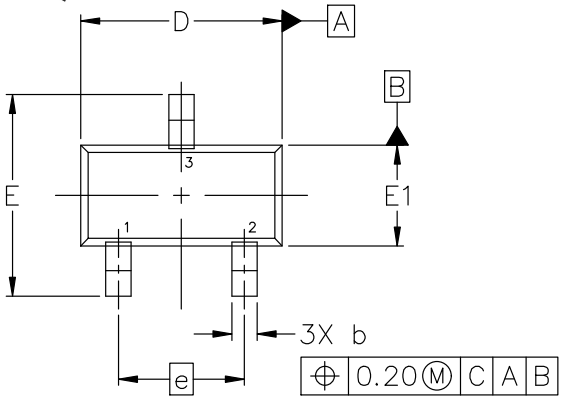
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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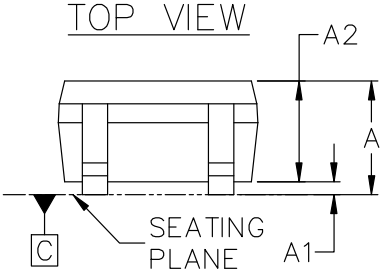
SC75−3 1.60x0.80x0.80, 1.00P
CASE 463
ISSUE H

DATE 01 FEB 2024

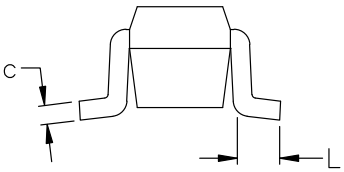




TOP VIEW



SIDE VIEW



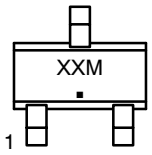
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
A1	0.00	0.05	0.10
A2		0.80 REF.	
b	0.15	0.20	0.30
c	0.10	0.15	0.25
D	1.55	1.60	1.65
E	1.50	1.60	1.70
E1	0.70	0.80	0.90
e		1.00 BSC	
L	0.10	0.15	0.20

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

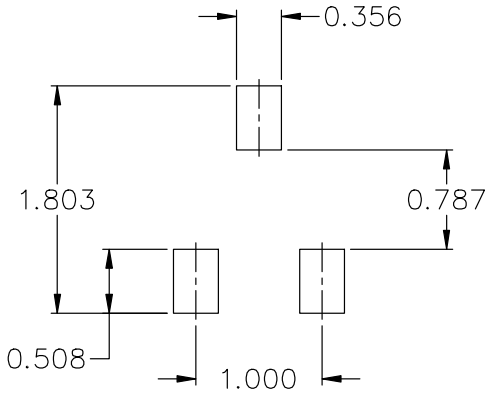
STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN



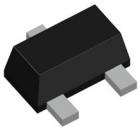
RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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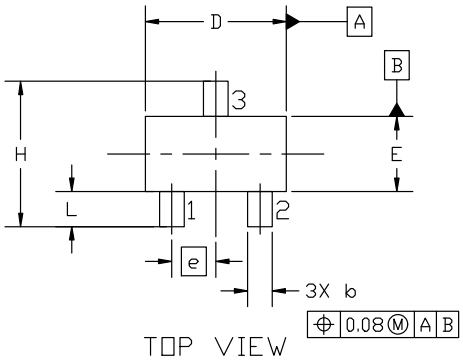
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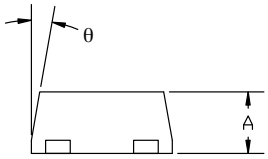


SC−89 3−LEAD, 1.60x0.85x0.70, 0.50P
CASE 463C
ISSUE D

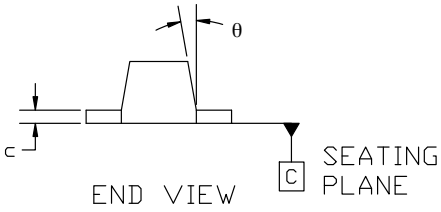
DATE 20 FEB 2024



TOP VIEW



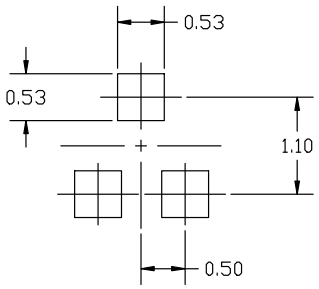
SIDE VIEW



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

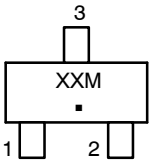
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
b	0.23	0.28	0.33
c	0.10	0.15	0.20
D	1.50	1.60	1.70
E	0.75	0.85	0.95
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.30	0.40	0.50
θ	---	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

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