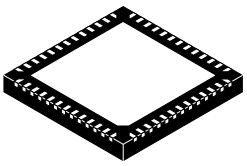
Multi-Phase Controller with I²C Interface for DrMOS

NCP81233

The NCP81233, a multi-phase synchronous buck controller with an I²C interface, provides power management solutions for applications supported by DrMOS. It supports 1-, 2-, 3-, 4-, or 6-phase operation and provides differential voltage and current sense, flexible programming, and comprehensive protections.



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GFN52 6x6, O.4P
CASE 485BE

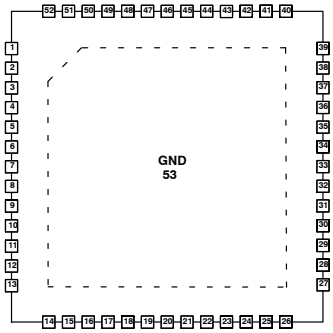
Features

- Selectable 1-, 2-, 3-, 4-, or 6-Phase Operation
- Support up to 12-Phase Operation with Phase Doublers
- I²C Interface with 8 Programmable Addresses
- Vin = 4.5 V ~ 20 V with Input Feedforward
- Integrated 5.35 V LDO and 3.3 V LDO
- Fsw = 200 k ~ 1.2 MHz
- Vout = 0.6 V ~ 5.3 V with 0.25 V~1.52 V DAC (5 mV/step)
- Programmable Vboot Voltage 0.6V ~ 1.23V (10mV/step) with Restore Function
- DVID Slew Rate Options (0.125 mV/us, 0.25 mV/us, 0.5 mV/us, 1 mV/us, 2 mV/us, 4 mV/us, 8 mV/us, 16 mV/us)
- Programmable External Reference Input
- PWM Output Compatible to 3.3 V and 5 V DrMOS
- Differential Output Voltage Sense
- Differential Current Sense Compatible for both Inductor DCR Sense and DrMOS Iout Signal
- Programmable Load Line
- Report of Vout and Iout
- Enable with Programmable Input UVLO
- DrMOS Power Ready Detection (DRVON)
- Externally Programmable Soft Start
- Power Saving Interface
- Power Good Indicator
- Programmable Over Current Protection
- Programmable Over/Under Voltage Protection
- Hiccup Over Temperature Protection
- Thermal Shutdown Protection
- This is a Pb-Free Device

Typical Applications

- Telecom Applications
- Server and Storage System
- Graphics Card Applications
- Multiphase DC-DC Power Management

PINOUT
52 PIN, QFN



For more details see Figure 1.

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “ ▪”, may or may not be present.

ORDERING INFORMATION

Device	Package	Shipping†
NCP81233MNTXG	QFN52 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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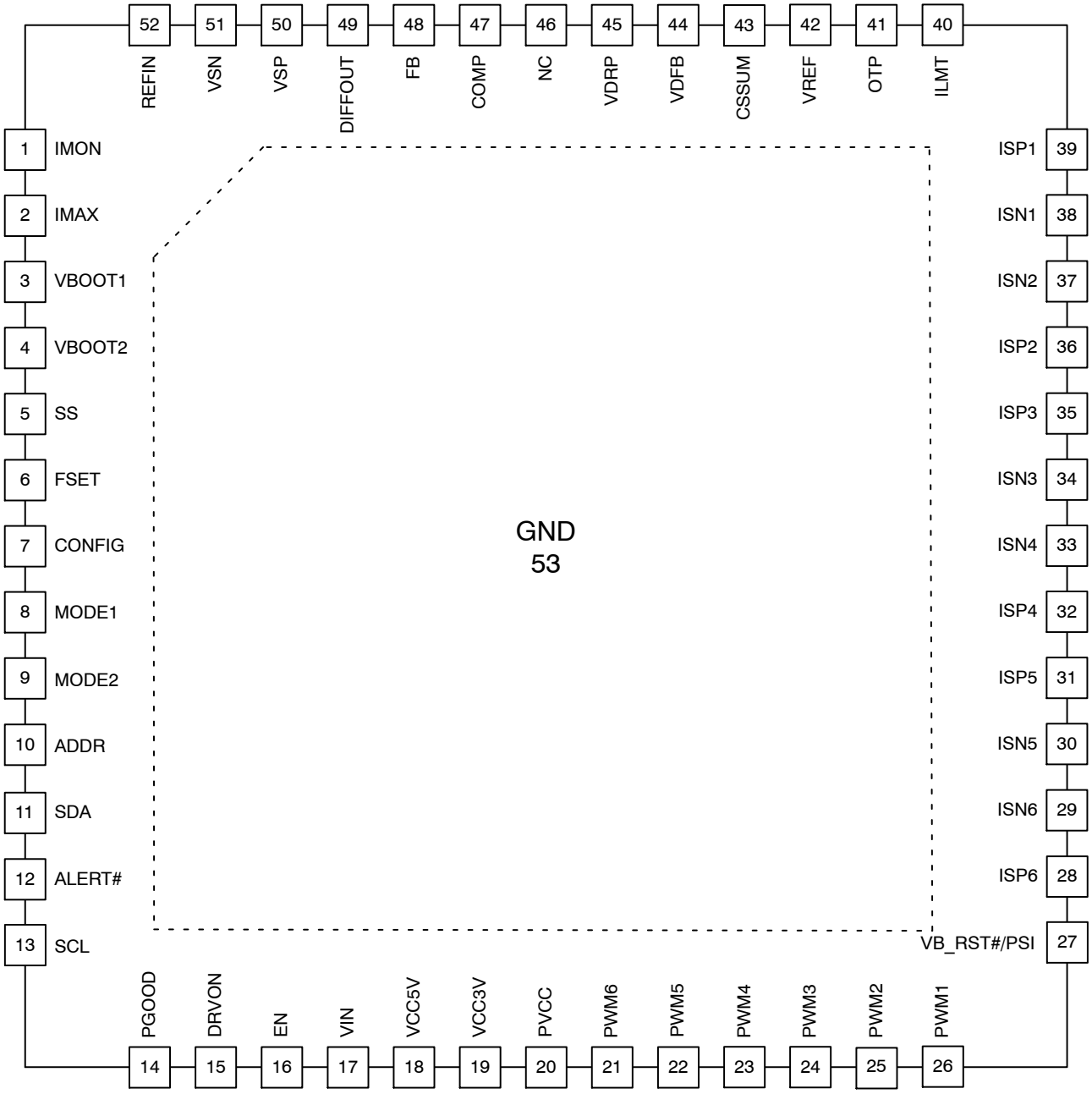

Figure 1. Pin Configuration

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TABLE 1. PIN DESCRIPTION

Pin	Name	Type	Description
1	IMON	Analog Output	OUT Current Monitor. Provides output signal representing output current by connecting a capacitor from this pin to ground.
2	IMAX	Analog Input	Current Maximum. A resistor from this pin to ground programs IMAX.
3	VBOOT1	Analog Input	Boot-Up Voltage 1. A resistor from this pin to ground programs boot voltage
4	VBOOT2	Analog Input	Boot-Up Voltage 2. A resistor from this pin to ground programs boot voltage.
5	SS	Analog Input	Soft-Start Slew Rate. A resistor from this pin to ground programs soft-start slew rate.
6	FSET	Analog Input	Frequency Selection. A resistor from this pin to ground programs switching frequency per phase.
7	CONFIG	Analog Input	Configuration. A resistor from this pin to ground programs configuration of power stages.
8	MODE1	Analog Input	Mode Programming 1. A resistor from this pin to ground programs configuration of operation functions.
9	MODE2	Analog Input	Mode Programming 2. A resistor from this pin to ground programs configuration of operation functions.
10	ADDR	Analog Input	Address. A resistor from this pin to ground programs address of I^2C interface.
11	SDA	Logic Bidirectional	Serial Data I/O Port. Data port of I^2C interface.
12	ALERT#	Logic Output	ALERT. Open-drain output. Provides a logic low valid alert signal.
13	SCL	Logic Input	Serial Clock. Clock input of I^2C interface.
14	PGOOD	Logic Output	Power GOOD. Open-drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.
15	DRVON	Analog Input	Driver On. High input voltage means power supply of DrMOS's driver is ready.
16	EN	Analog Input	Enable. Logic high enables controller while logic low disables controller. Input supply UVLO can be programmed at this pin.
17	VIN	Power Input	Power Supply Input. Power supply input pin of the device, which is connected to the integrated 5.35 V LDO and 3.3 V LDO. 4.7 μF or more ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to this pin.
18	VCC5V	Analog Power	Voltage Supply of Controller. Output of integrated 5.35 V LDO and power input pin of analog circuits. A 4.7 μF ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
19	VCC3V	Analog Power	3.3 V Voltage Supply. Output of integrated 3.3 V LDO. A 4.7 μF ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
20	PVCC	Analog Power	Voltage Supply of PWM Drivers. Power supply input pin of internal PWM drivers and digital circuits, which is connected to VCC5 V via a 4.7 Ω resistor. A 1 μF or larger ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to this pin.
21	PWM6	Analog Output	PWM 6. PWM output of phase 6.
22	PWM5	Analog Output	PWM 5. PWM output of phase 5.
23	PWM4	Analog Output	PWM 4. PWM output of phase 4.
24	PWM3	Analog Output	PWM 3. PWM output of phase 3.
25	PWM2	Analog Output	PWM 2. PWM output of phase 2.
26	PWM1	Analog Output	PWM 1. PWM output of phase 1.
27	VB_RST# / PSI	Logic Input	VBOOT Restore. Logic low restores output to boot voltage. Power Saving Interface. Logic high enables Multi-phase CCM operation, and logic low enables 1-phase CCM operation. Pin function is programmed at MODE2 pin.
28	ISP6	Analog Input	Current Sense Positive Input 6. Non-inverting input of differential current sense amplifier of phase 6.

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TABLE 1. PIN DESCRIPTION (continued)

Pin	Name	Type	Description
29	ISN6	Analog Input	Current Sense Negative Input 6. Inverting input of differential current sense amplifier of phase 6.
30	ISN5	Analog Input	Current Sense Negative Input 5. Inverting input of differential current sense amplifier of phase 5.
31	ISP5	Analog Input	Current Sense Positive Input 5. Non-inverting input of differential current sense amplifier of phase 5.
32	ISP4	Analog Input	Current Sense Positive Input 4. Non-inverting input of differential current sense amplifier of phase 4.
33	ISN4	Analog Input	Current Sense Negative Input 4. Inverting input of differential current sense amplifier of phase 4.
34	ISN3	Analog Input	Current Sense Negative Input 3. Inverting input of differential current sense amplifier of phase 3.
35	ISP3	Analog Input	Current Sense Positive Input 3. Non-inverting input of differential current sense amplifier of phase 3.
36	ISP2	Analog Input	Current Sense Positive Input 2. Non-inverting input of differential current sense amplifier of phase 2.
37	ISN2	Analog Input	Current Sense Negative Input 2. Inverting input of differential current sense amplifier of phase 2.
38	ISN1	Analog Input	Current Sense Negative Input 1. Inverting input of differential current sense amplifier of phase 1.
39	ISP1	Analog Input	Current Sense Positive Input 1. Non-inverting input of differential current sense amplifier of phase 1.
40	ILMT	Analog Input	Limit of Current. Voltage at this pin sets over-current threshold.
41	OTP	Analog Input	Over Temperature Protection. Voltage at this pin sets over-temperature threshold.
42	VREF	Analog Output	Output of Reference. Output of 0.6 V reference. A 10 nF ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
43	CSSUM	Analog Output	Current Sense SUM. Output of current sum amplifier.
44	VDFB	Analog Output	Droop Amplifier Feedback. Inverting input of droop amplifier
45	VDRP	Analog Output	Droop Amplifier Output. Output of droop amplifier.
46	NC	No Connection	
47	COMP	Analog Output	Compensation. Output pin of error amplifier.
48	FB	Analog Input	Feedback. Inverting input of internal error amplifier.
49	DIFFOUT	Analog Output	Differential Amplifier Output. Output pin of differential voltage sense amplifier.
50	VSP	Analog Input	Voltage Sense Positive Input. Non-inverting input of differential voltage sense amplifier.
51	VSN	Analog Input	Voltage Sense Negative Input. Inverting input of differential voltage sense amplifier.
52	REFIN	Analog Input	Reference Voltage Input. External reference voltage input.
53	THERM/GND	Analog Ground	Thermal Pad and Analog Ground. Ground of internal control circuits. Must be connected to the system ground.

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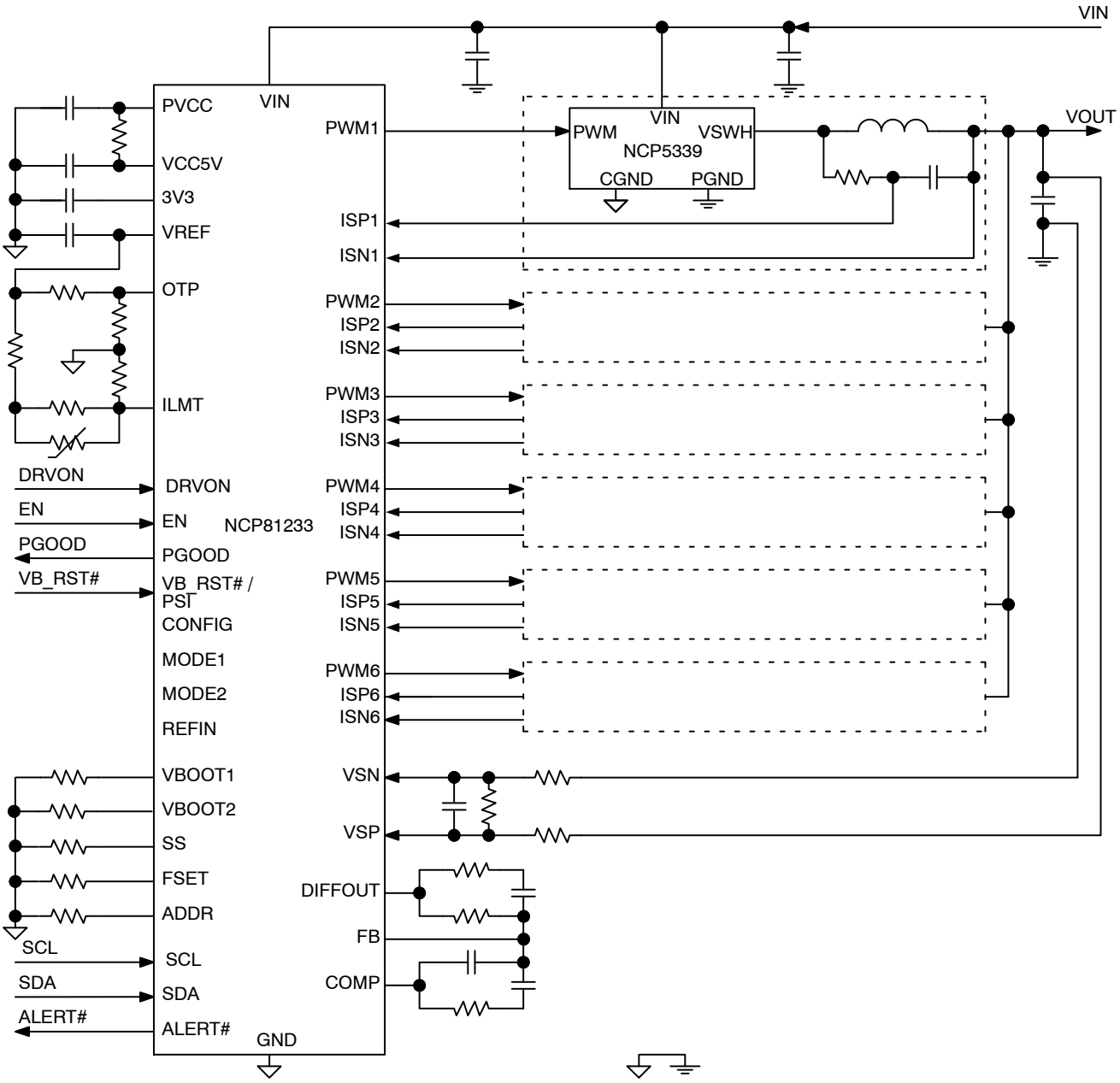

Figure 2. Typical Application Circuit with Programmed Boot Voltage

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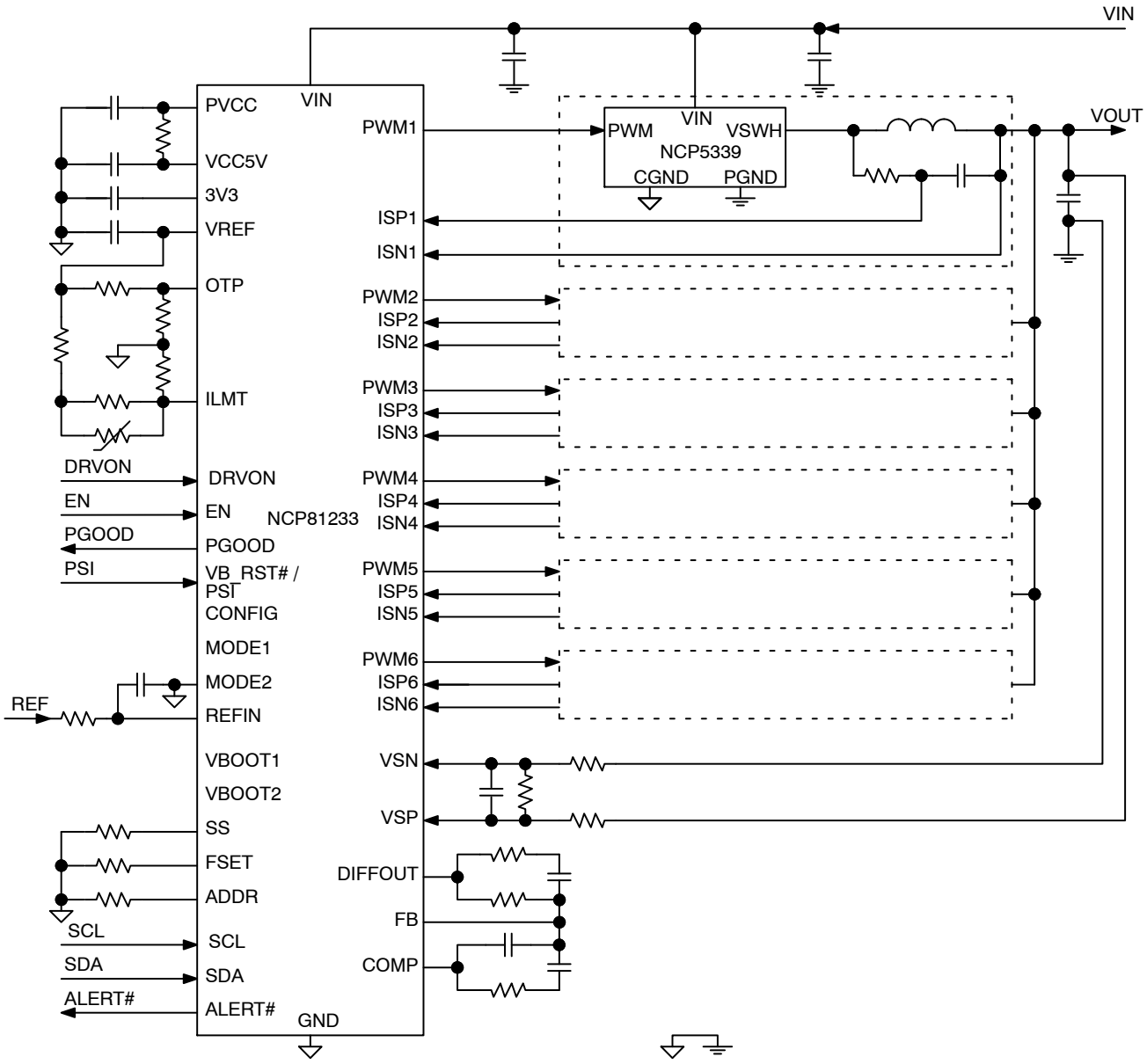

Figure 3. Typical Application Circuit with External Reference Input

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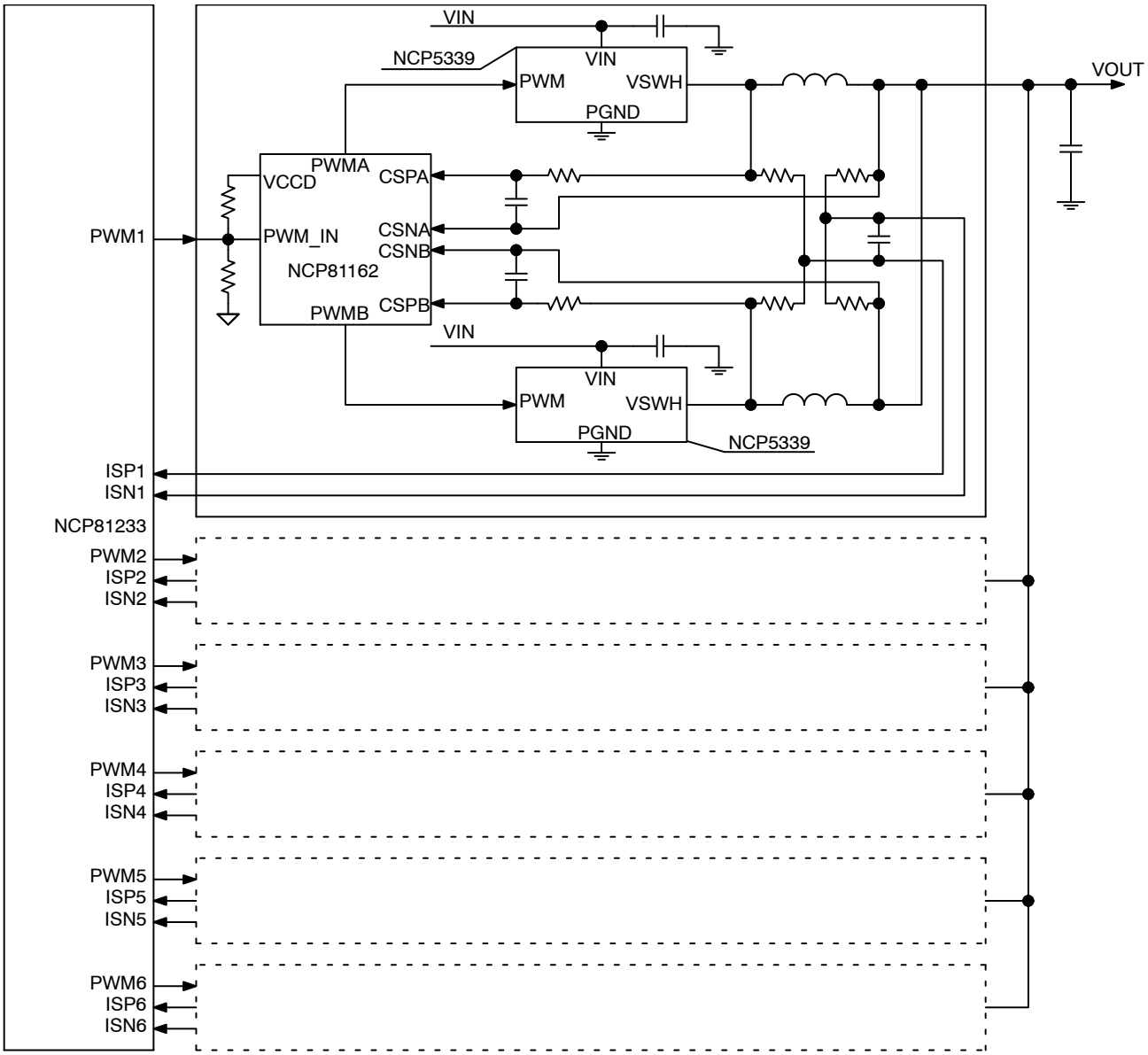

Figure 4. Application Circuit with Phase Doublers

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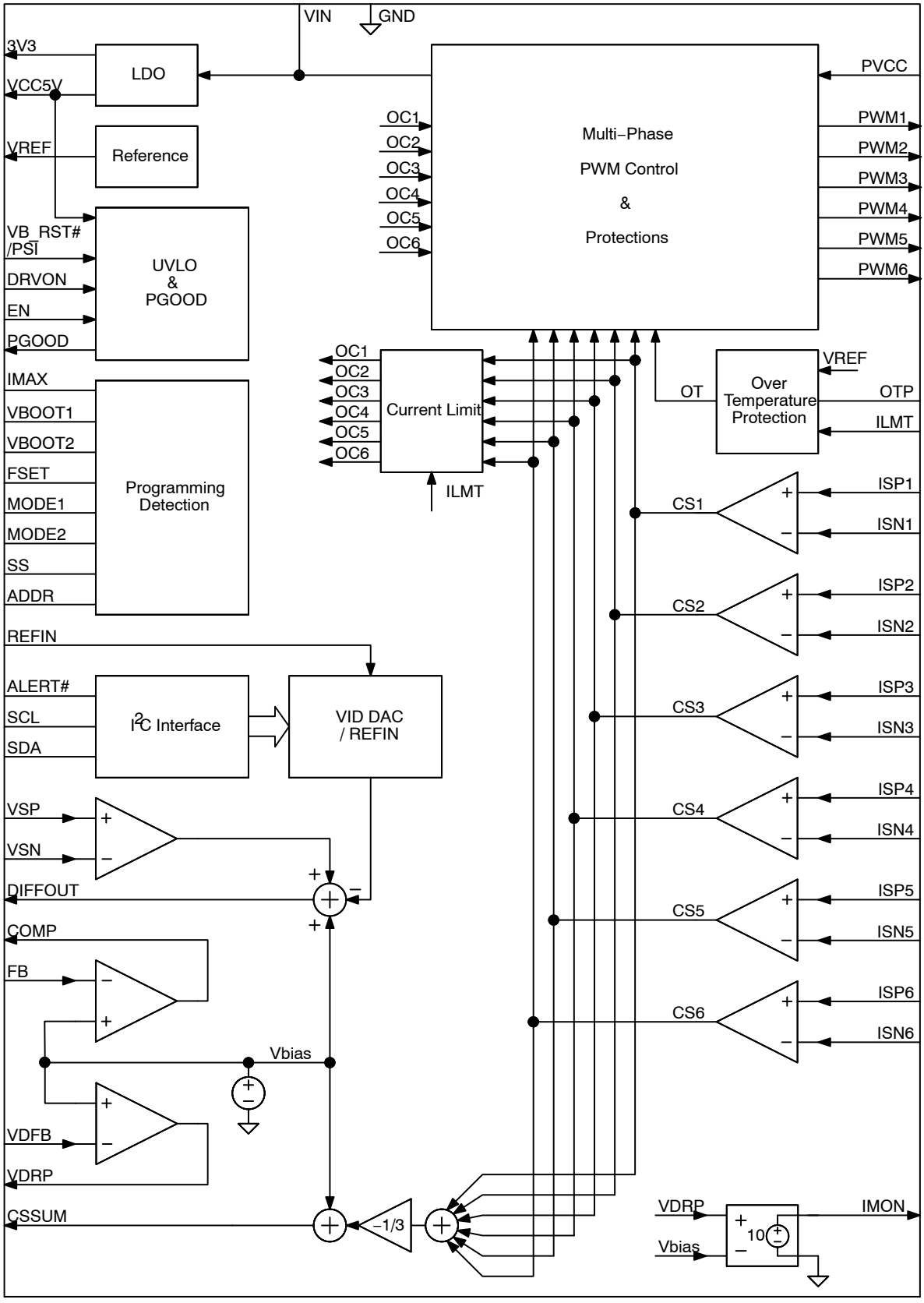

Figure 5. Functional Block Diagram

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TABLE 2. MAXIMUM RATINGS

Symbol	Rating	Value		Unit
		MIN	MAX	
V_{VIN}	Power Supply Voltage to PGND		30	V
V_{VCC5V}	Supply Voltage VCC5V to GND	−0.3	6.5	V
V_{VSN}	VSNx to GND	−0.2	0.2	V
	Other Pins to GND	−0.3	VCC5 V+0.3	V
ESD HBM	Human Body Model (HBM) ESD Rating are (Note 1)		2500	V
ESD CDM	Charge Device Model (CDM) ESD Rating are (Note 1)		2000	V
I_{LU}	Latch up Current: (Note 2)	−100	100	mA
T_J	Operating Junction Temperature Range (Note 3)	−40	125	°C
T_A	Operating Ambient Temperature Range	−40	100	°C
T_{STG}	Storage Temperature Range	−55	150	°C
$R_{\Psi JC}$	Thermal Resistance Junction to Top Case(Note 4)	1.65		°C/W
$R_{\Psi JB}$	Thermal Resistance Junction to Board (Note 4)	3.2		°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 4)	67.4		°C/W
P_D	Power Dissipation (Note 5)	1.48		W
MSL	Moisture Sensitivity Level (Note 6)	1		–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device is ESD sensitive. Handling precautions are needed to avoid damage or performance degradation.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
4. JEDEC standard JESD 51−7 (1S2P Direct-Attach Method) with 0 LFM. It is for checking junction temperature using external measurement.
5. The maximum power dissipation (PD) is dependent on input voltage, maximum output current and external components selected. Tambient = 25°C, Tjunc_max = 125°C, PD = (Tjunc_max−T_amb)/Theta JA
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

TABLE 3. ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J = −40°C to 100°C. unless other noted.)

Symbol	Characteristics	Test Conditions	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
V_{IN}	VIN Supply Voltage Range	(Note 7)	4.5	12	20	V
V_{CCUV-}	VCC5V Under-Voltage (UVLO) Threshold	VCC5V falling	3.7			V
V_{CCOK}	VCC5V OK Threshold	VCC5V rising			4.3	V
V_{CCHYS}	VCC5V UVLO Hysteresis			270		mV
V_{CC3UV-}	VCC3V Under−Voltage (UVLO) Threshold	VCC3V falling	2.6			V
V_{CC3OK}	VCC3V OK Threshold	VCC3V rising			2.9	V
V_{CC3HYS}	VCC3V UVLO Hysteresis			135		mV
VCC5V REGULATOR						
V_{CC}	Output Voltage	6V < VIN < 20V, IVCC5V = 15mA (External),EN = Low	5.2	5.35	5.5	V
	Load Regulation	IVCC5V = 5mA to 25mA (External), EN = Low	−2.0	0.2	2.0	%
V_{DO_VCC}	Dropout Voltage	VIN = 5V, IVCC5V = 25mA (External), EN = Low			200	mV

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TABLE 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = −40°C to 100°C. unless other noted.)

Symbol	Characteristics	Test Conditions		MIN	TYP	MAX	UNITS
VCC3V REGULATOR							
V_{3V3}	Output Voltage	IVCC3V = 5 mA (External), EN = Low		3.1	3.3	3.5	V
	Load Regulation	IVCC3V = 0.5 mA to 10 mA (External), EN = Low		−3.0		3.0	%
SUPPLY CURRENT							
I_{QVIN}	VIN Quiescent Current	EN high, 1−phase only EN high, 6−phase		− −	11 17	20 28	mA mA
I_{sdVIN}	VIN Shutdown Current	EN low		−	5	9	mA
VREF							
V_{VREF}	VREF Output Voltage	IVREF = 500 μA		594	600	606	mV
	Load Regulation	IVREF = 0 mA to 2 mA		−1.0		1.0	%
REFIN							
	Maximum REFIN Voltage	(Note 7)				1.53	V
I_{REFIN}	REFIN Bias Current	V_{REFIN} = 1.0 V		−100		100	nA
SYSTEM VOLTAGE ACCURACY							
	System Voltage Accuracy ($V = V_{DAC}$ or V_{REFIN})	1.0 V < V ≤ 1.52 V	−40°C to 85°C	−7		7	mV
			−40°C to 125°C	−10		10	
		0.7 V ≤ V ≤ 1.0 V	−40°C to 85°C	−0.5		0.5	%
			−40°C to 125°C	−1.0		1.0	
		0.5 V ≤ V < 0.7 V	−40°C to 85°C	−7		7	mV
			−40°C to 125°C	−10		10	
		0.25 V ≤ V < 0.5 V	−40°C to 85°C	−8		8	mV
			−40°C to 125°C	−12		12	
DIFFERENTIAL VOLTAGE-SENSE AMPLIFIER							
	VSP Input Voltage Range	(Note 7)		−0.2		1.72	V
	VSN Input Voltage Range	(Note 7)		−0.2		0.2	V
GAIN_DVA	DC Gain	VSP−VSN = 0 V to 1.52 V			1.0		V/V
BW_DVA	−3dB Gain Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND (Note 7)			10		MHz
I_{VS}	Input Bias Current	VSP = 1.72, VSN = −0.2 V		−400		400	nA
VOLTAGE ERROR AMPLIFIER							
$GAIN_{EA}$	Open-Loop DC Gain	(Note 7)			80		dB
GBW_{EA}	Unity Gain Bandwidth	(Note 7)			20		MHz
SR_{COMP}	Slew Rate	(Note 7)			20		V/μs
$V_{maxCOMP}$	COMP Voltage Swing	I_{COMP}(source) = 2 mA		3.2	3.4	−	V
$V_{minCOMP}$		I_{COMP}(sink) = 2 mA	TRBST is Enabled			0.3	V
			TRBST is Disabled	−	1.1		
I_{FB}	FB Bias Current	V_{FB} = 1.3V		−400		400	nA
DIFFERENTIAL CURRENT-SENSE AMPLIFIER							
$GAIN_{CA}$	DC Gain				6		V/V

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TABLE 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = −40°C to 100°C. unless other noted.)

Symbol	Characteristics	Test Conditions	MIN	TYP	MAX	UNITS
DIFFERENTIAL CURRENT-SENSE AMPLIFIER						
BW_{CA}	−3dB Gain Bandwidth	(Note 7)		10		MHz
	Input Common Mode Voltage Range	(Note 7)	−0.2		Vcc+0.1	V
	Differential Input Voltage Range	(Note 7)	−60	–	60	mV
I_{CS}	Input Bias Current	ISP, ISN = 1.0 V	−100		100	nA
CURRENT SUMMING AMPLIFIER						
$GAIN_{CSSUM}$	DC Gain	From (ISPn − ISNn) to (CSSUM − Vbias)		−2		V/V
BW_{CSSUM}	−3dB Gain Bandwidth	CL = 10 pF to GND, RL = 10 kΩ to GND (Note 7)		5		MHz
$V_{osCSSUM}$	CSSUM Output Offset	All (ISPn − ISNn) = 0 V (Note 7)	−7	0	7	mV
	Maximum CSSUM Output Voltage	I_{CSSUM}(source) = 1 mA (Note 7)		2.02		V
	Minimum CSSUM Output Voltage	I_{CSSUM}(sink) = 1 mA (Note 7)		0.56		V
DROOP AMPLIFIER						
$GAIN_{DA}$	Open-Loop DC Gain	(Note 7)		80		dB
GBW_{DA}	Unity Gain Bandwidth	(Note 7)		10		MHz
V_{osDA}	Input Offset Voltage	(Note 7)	−2.5		2.5	mV
I_{DFB}	Input Bias Current	V_{DFB} = 1.3V	−200		200	nA
	Maximum VDRP Output Voltage	I_{VDRP}(source) = 2 mA (Note 7)		3.0		V
	Minimum VDRP Output Voltage	I_{VDRP}(sink) = 2 mA (Note 7)		1.0		V
IMON AMPLIFIER						
$GAIN_{IMON}$	DC Gain			10		V/V
BW_{IMON}	−3dB Gain Bandwidth	(Note 7)		2		MHz
V_{osIMON}	Input Offset Voltage	(Note 7)	−2		2	mV
R_{IMON}	Output Impedance	(Note 7)		20		kΩ
IMAX						
	SourceCurrent	V_{IMAX} = 1V	47.5	50	52.5	μA
I^2C INTERFACE ADDRESS						
–	Address	Float Short to GND 2.7k 5.1k 8.2k 13k 20k 33k	–	1110000 1110001 1110010 1110011 1110100 1110101 1110110 1110111	–	–

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TABLE 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = −40°C to 100°C. unless other noted.)

Characteristics	Test Conditions	Symbol	MIN	TYP	MAX	UNITS
VBOOT CODE						
VBOOT1	Float Short to GND 2.7 k 5.1 k 8.2 k 13 k 20 k 33 k	–	–	000XXX 001XXX 010XXX 011XXX 100XXX 101XXX 110XXX 111XXX	–	–
VBOOT2	Float Short to GND 2.7 k 5.1 k 8.2 k 13 k 20 k 33 k	–	–	XXX000 XXX001 XXX010 XXX011 XXX100 XXX101 XXX110 XXX111	–	–
Source Current		I_{VBT}	45	50	55	μA
SWITCHING FREQUENCY						
Switching Frequency	2.7 k 5.1 k Float 8.2 k Short to GND 13 k 20 k 33 k	F_{SW}	180 270 360 450 540 720 900 1080	200 300 400 500 600 800 1000 1200	220 330 440 550 660 880 1100 1320	kHz
Source Current		I_{FS}	45	50	55	μA
SYSTEM RESET TIME						
System Reset Time	Measured from EN to start of soft start.	T_{RST}		2.0		ms
SOFT START						
Soft−Start Slew Rate	Float	SSSR		0.125		mV/us
	33 k			0.25		
	20 k			0.5		
	13 k			1.0		
	8.2 k			2.0		
	5.1 k			4.0		
	2.7 k			8.0		
	Short to GND			16		
Source Current		I_{SS}	45	50	55	μA
DVID						
DVID Slew Rate	000	SR		0.125		mV/us
	001			0.25		
	010			0.5		
	011			1.0		
	100			2.0		
	101			4.0		
	110			8.0		
	111			16		
I²C INTERFACE						
Logic High Input Voltage		$V_{IH(SDA, SCL)}$	1.5			V

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TABLE 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12 V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J = −40°C to 100°C. unless other noted.)

Characteristics	Test Conditions	Symbol	MIN	TYP	MAX	UNITS
I²C INTERFACE						
Logic Low Input Voltage		$V_{IL(SDA, SCL)}$			0.7	V
Hysteresis				350		mV
SDA Output Low Voltage	I_{SDA} = −4 mA	V_{OL}			0.3	V
Input Current		I_{IH}; I_{IL}	−1.0		1.0	μA
Input Capacitance	(Note 7)	$C_{SCL, SDA}$		5.0		pF
Clock Frequency	(Note 7)	f_{SCL}			400	kHz
SCL Falling Edge to SDA Valid Time	(Note 7)				1.0	μs
ALERT# Low Voltage	I_{ALERT}= −4 mA	V_{LALERT}			0.3	V
ALERT# Leakage Current	ALERT# = 5 V	$I_{lkgALERT}$			1.0	μA
PGOOD						
PGOOD Startup Delay	Measured from end of Soft Start to PGOOD assertion (Note 7)	T_{d_PGOOD}		100		μs
PGOOD Shutdown Delay	Measured from EN to PGOOD de-assertion			250		ns
PGOOD Low Voltage	I_{PGOOD}= −4 mA	V_{IPGOOD}			0.3	V
PGOOD Leakage Current	PGOOD = 5 V	$I_{lkgPGOOD}$			1.0	μA
PROTECTIONS						
Current Limit Threshold	Measured from ILIMT to GND, ISP−ISN = 50 mV	V_{OCTH}	285	300	315	mV
	Measured from ILIMT to GND, ISP−ISN = 2 0 mV		110	120	130	
Over Current Protection (OCP) Debounce Time	(Note 7)			8 Cycles		us
Under Voltage Threshold Below DAC	VSP falling	V_{UVTH}	250	300	350	mV
Under Voltage Protection (UVP) Hysteresis		V_{UVHYS}		25		mV
Under-voltage Debounce Time	(Note 7)			5		μs
Shutdown Time in Hiccup Mode	UVP (Note 7) OCP (Note 7) OTP (Note 7)			30 40 20		ms
Absolute Over Voltage Threshold During Soft-Start	VSP-GND		2.0	2.1	2.2	V
Absolute Over Voltage Threshold Hysteresis				−25		mV
Over Voltage Threshold Above DAC	VSP rising	V_{OVTH}	175	200	225	mV
Over Voltage Protection Hysteresis	VSP falling	V_{OVHYS}		−25		mV
Over Voltage Debounce Time	VSP rising to GH low			1.0		us
Offset Voltage of OTP Comparator	VILMT = 200 mV	V_{OS_OTP}	−2		2	mV
OTP Source Current		I_{OTP}	9	10	11	μA
OTP Debounce Time	(Note 7)			140		ns
Thermal Shutdown (TSD) Threshold	(Note 7)	T_{sd}	140	150		°C
Recovery Temperature Threshold	(Note 7)	T_{rec}		125		°C
Thermal Shutdown (TSD) Debounce Time	(Note 7)			120		ns

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TABLE 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = −40°C to 100°C. unless other noted.)

Characteristics	Test Conditions	Symbol	MIN	TYP	MAX	UNITS
ENABLE						
EN Operation Voltage Range			0		3.5	V
EN ON Threshold		V_{EN_TH}	0.7	0.8	0.85	V
Hysteresis Source Current	VCC5V is OK	I_{EN_HYS}	25	30	35	μA
DRVON						
DRVON Operation Voltage Range			0		2.0	V
DRVON ON Threshold		V_{DRVON_TH}	0.75	0.8	0.85	V
Hysteresis Source Current	VCC5V is OK	I_{DRVON_HYS}	25	30	35	μA
VB_RST# and PSI						
High Threshold		$V_{highRST}$	1.5	–	–	V
Low Threshold		V_{lowRST}	–	–	0.7	V
Hysteresis		V_{hysRST}		350		mV
Input Bias Current	External 1 K pull−up to 3.3 V	$I_{biasRST}$	–	–	1.0	μA
PWM MODULATION						
Minimum On Time	(Note 7)	T_{on_min}			50	ns
Minimum Off Time	(Note 7)	T_{off_min}	160			ns
0% Duty Cycle	COMP voltage when the PWM outputs remain Lo (Note 7)			1.3		V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI, Vin = 12.0 V (Note 7)			2.5		V
Ramp Feed−forward Voltage Range	(Note 7)		4.5		20	V
PWM OUTPUT						
PWM Output High Voltage	Isource = 0.5 mA	V_{PWM_H}	V_{CC} −0.2			V
PWM Output Low Voltage	Isink = 0.5 mA	V_{PWM_L}			0.2	V
Rise and Fall Times	CL (PCB) = 50 pF, measured between 10% & 90% of VCC (Note 7)			10		ns
Leakage Current in Hi-Z Stage		I_{LK_PWM}	−1.0		1.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design, not tested in production.

Table 4. RESISTOR OPTIONS FOR FUNCTION PROGRAMMING

Resistance Range (kΩ)			Resistor Options (kΩ)				
MIN	TYP	MAX	±5%	±1%			
2.565	2.7	2.835	2.7	2.61	2.67	2.74	2.80
4.845	5.1	5.355	5.1	4.87	4.99	5.11	5.23
7.79	8.2	8.61	8.2	7.87	8.06	8.25	8.45
12.35	13	13.65	13	12.4	12.7	13	13.3
19	20	21	20	19.1	19.6	20	20.5
31.35	33	34.65	33	31.6	32.4	33.2	34

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TABLE 5. VBOOT CODES

VBOOT1			VBOOT2			Voltage(V)	HEX		VBOOT1			VBOOT2			Voltage(V)	HEX
0	0	0	0	0	0	0.6	00		1	0	0	0	0	0	0.92	20
0	0	0	0	0	1	0.61	01		1	0	0	0	0	1	0.93	21
0	0	0	0	1	0	0.62	02		1	0	0	0	1	0	0.94	22
0	0	0	0	1	1	0.63	03		1	0	0	0	1	1	0.95	23
0	0	0	1	0	0	0.64	04		1	0	0	1	0	0	0.96	24
0	0	0	1	0	1	0.65	05		1	0	0	1	0	1	0.97	25
0	0	0	1	1	0	0.66	06		1	0	0	1	1	0	0.98	26
0	0	0	1	1	1	0.67	07		1	0	0	1	1	1	0.99	27
0	0	1	0	0	0	0.68	08		1	0	1	0	0	0	1	28
0	0	1	0	0	1	0.69	09		1	0	1	0	0	1	1.01	29
0	0	1	0	1	0	0.7	0A		1	0	1	0	1	0	1.02	2A
0	0	1	0	1	1	0.71	0B		1	0	1	0	1	1	1.03	2B
0	0	1	1	0	0	0.72	0C		1	0	1	1	0	0	1.04	2C
0	0	1	1	0	1	0.73	0D		1	0	1	1	0	1	1.05	2D
0	0	1	1	1	0	0.74	0E		1	0	1	1	1	0	1.06	2E
0	0	1	1	1	1	0.75	0F		1	0	1	1	1	1	1.07	2F
0	1	0	0	0	0	0.76	10		1	1	0	0	0	0	1.08	30
0	1	0	0	0	1	0.77	11		1	1	0	0	0	1	1.09	31
0	1	0	0	1	0	0.78	12		1	1	0	0	1	0	1.1	32
0	1	0	0	1	1	0.79	13		1	1	0	0	1	1	1.11	33
0	1	0	1	0	0	0.8	14		1	1	0	1	0	0	1.12	34
0	1	0	1	0	1	0.81	15		1	1	0	1	0	1	1.13	35
0	1	0	1	1	0	0.82	16		1	1	0	1	1	0	1.14	36
0	1	0	1	1	1	0.83	17		1	1	0	1	1	1	1.15	37
0	1	1	0	0	0	0.84	18		1	1	1	0	0	0	1.16	38
0	1	1	0	0	1	0.85	19		1	1	1	0	0	1	1.17	39
0	1	1	0	1	0	0.86	1A		1	1	1	0	1	0	1.18	3A
0	1	1	0	1	1	0.87	1B		1	1	1	0	1	1	1.19	3B
0	1	1	1	0	0	0.88	1C		1	1	1	1	0	0	1.2	3C
0	1	1	1	0	1	0.89	1D		1	1	1	1	0	1	1.21	3D
0	1	1	1	1	0	0.9	1E		1	1	1	1	1	0	1.22	3E
0	1	1	1	1	1	0.91	1F		1	1	1	1	1	1	1.23	3F

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TABLE 6. VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	OFF	00
0	0	0	0	0	0	0	1	0.25000	01
0	0	0	0	0	0	1	0	0.25500	02
0	0	0	0	0	0	1	1	0.26000	03
0	0	0	0	0	1	0	0	0.26500	04
0	0	0	0	0	1	0	1	0.27000	05
0	0	0	0	0	1	1	0	0.27500	06
0	0	0	0	0	1	1	1	0.28000	07
0	0	0	0	1	0	0	0	0.28500	08
0	0	0	0	1	0	0	1	0.29000	09
0	0	0	0	1	0	1	0	0.29500	0A
0	0	0	0	1	0	1	1	0.30000	0B
0	0	0	0	1	1	0	0	0.30500	0C
0	0	0	0	1	1	0	1	0.31000	0D
0	0	0	0	1	1	1	0	0.31500	0E
0	0	0	0	1	1	1	1	0.32000	0F
0	0	0	1	0	0	0	0	0.32500	10
0	0	0	1	0	0	0	1	0.33000	11
0	0	0	1	0	0	1	0	0.33500	12
0	0	0	1	0	0	1	1	0.34000	13
0	0	0	1	0	1	0	0	0.34500	14
0	0	0	1	0	1	0	1	0.35000	15
0	0	0	1	0	1	1	0	0.35500	16
0	0	0	1	0	1	1	1	0.36000	17
0	0	0	1	1	0	0	0	0.36500	18
0	0	0	1	1	0	0	1	0.37000	19
0	0	0	1	1	0	1	0	0.37500	1A
0	0	0	1	1	0	1	1	0.38000	1B
0	0	0	1	1	1	0	0	0.38500	1C
0	0	0	1	1	1	0	1	0.39000	1D
0	0	0	1	1	1	1	0	0.39500	1E
0	0	0	1	1	1	1	1	0.40000	1F
0	0	1	0	0	0	0	0	0.40500	20
0	0	1	0	0	0	0	1	0.41000	21

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TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	1	0	0	0	1	0	0.41500	22
0	0	1	0	0	0	1	1	0.42000	23
0	0	1	0	0	1	0	0	0.42500	24
0	0	1	0	0	1	0	1	0.43000	25
0	0	1	0	0	1	1	0	0.43500	26
0	0	1	0	0	1	1	1	0.44000	27
0	0	1	0	1	0	0	0	0.44500	28
0	0	1	0	1	0	0	1	0.45000	29
0	0	1	0	1	0	1	0	0.45500	2A
0	0	1	0	1	0	1	1	0.46000	2B
0	0	1	0	1	1	0	0	0.46500	2C
0	0	1	0	1	1	0	1	0.47000	2D
0	0	1	0	1	1	1	0	0.47500	2E
0	0	1	0	1	1	1	1	0.48000	2F
0	0	1	1	0	0	0	0	0.48500	30
0	0	1	1	0	0	0	1	0.49000	31
0	0	1	1	0	0	1	0	0.49500	32
0	0	1	1	0	0	1	1	0.50000	33
0	0	1	1	0	1	0	0	0.50500	34
0	0	1	1	0	1	0	1	0.51000	35
0	0	1	1	0	1	1	0	0.51500	36
0	0	1	1	0	1	1	1	0.52000	37
0	0	1	1	1	0	0	0	0.52500	38
0	0	1	1	1	0	0	1	0.53000	39
0	0	1	1	1	0	1	0	0.53500	3A
0	0	1	1	1	0	1	1	0.54000	3B
0	0	1	1	1	1	0	0	0.54500	3C
0	0	1	1	1	1	0	1	0.55000	3D
0	0	1	1	1	1	1	0	0.55500	3E
0	0	1	1	1	1	1	1	0.56000	3F
0	1	0	0	0	0	0	0	0.56500	40
0	1	0	0	0	0	0	1	0.57000	41
0	1	0	0	0	0	1	0	0.57500	42
0	1	0	0	0	0	1	1	0.58000	43

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TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	0	0	0	1	0	0	0.58500	44
0	1	0	0	0	1	0	1	0.59000	45
0	1	0	0	0	1	1	0	0.59500	46
0	1	0	0	0	1	1	1	0.60000	47
0	1	0	0	1	0	0	0	0.60500	48
0	1	0	0	1	0	0	1	0.61000	49
0	1	0	0	1	0	1	0	0.61500	4A
0	1	0	0	1	0	1	1	0.62000	4B
0	1	0	0	1	1	0	0	0.62500	4C
0	1	0	0	1	1	0	1	0.63000	4D
0	1	0	0	1	1	1	0	0.63500	4E
0	1	0	0	1	1	1	1	0.64000	4F
0	1	0	1	0	0	0	0	0.64500	50
0	1	0	1	0	0	0	1	0.65000	51
0	1	0	1	0	0	1	0	0.65500	52
0	1	0	1	0	0	1	1	0.66000	53
0	1	0	1	0	1	0	0	0.66500	54
0	1	0	1	0	1	0	1	0.67000	55
0	1	0	1	0	1	1	0	0.67500	56
0	1	0	1	0	1	1	1	0.68000	57
0	1	0	1	1	0	0	0	0.68500	58
0	1	0	1	1	0	0	1	0.69000	59
0	1	0	1	1	0	1	0	0.69500	5A
0	1	0	1	1	0	1	1	0.70000	5B
0	1	0	1	1	1	0	0	0.70500	5C
0	1	0	1	1	1	0	1	0.71000	5D
0	1	0	1	1	1	1	0	0.71500	5E
0	1	0	1	1	1	1	1	0.72000	5F
0	1	1	0	0	0	0	0	0.72500	60
0	1	1	0	0	0	0	1	0.73000	61
0	1	1	0	0	0	1	0	0.73500	62
0	1	1	0	0	0	1	1	0.74000	63
0	1	1	0	0	1	0	0	0.74500	64
0	1	1	0	0	1	0	1	0.75000	65

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TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	1	0	0	1	1	0	0.75500	66
0	1	1	0	0	1	1	1	0.76000	67
0	1	1	0	1	0	0	0	0.76500	68
0	1	1	0	1	0	0	1	0.77000	69
0	1	1	0	1	0	1	0	0.77500	6A
0	1	1	0	1	0	1	1	0.78000	6B
0	1	1	0	1	1	0	0	0.78500	6C
0	1	1	0	1	1	0	1	0.79000	6D
0	1	1	0	1	1	1	0	0.79500	6E
0	1	1	0	1	1	1	1	0.80000	6F
0	1	1	1	0	0	0	0	0.80500	70
0	1	1	1	0	0	0	1	0.81000	71
0	1	1	1	0	0	1	0	0.81500	72
0	1	1	1	0	0	1	1	0.82000	73
0	1	1	1	0	1	0	0	0.82500	74
0	1	1	1	0	1	0	1	0.83000	75
0	1	1	1	0	1	1	0	0.83500	76
0	1	1	1	0	1	1	1	0.84000	77
0	1	1	1	1	0	0	0	0.84500	78
0	1	1	1	1	0	0	1	0.85000	79
0	1	1	1	1	0	1	0	0.85500	7A
0	1	1	1	1	0	1	1	0.86000	7B
0	1	1	1	1	1	0	0	0.86500	7C
0	1	1	1	1	1	0	1	0.87000	7D
0	1	1	1	1	1	1	0	0.87500	7E
0	1	1	1	1	1	1	1	0.88000	7F
1	0	0	0	0	0	0	0	0.88500	80
1	0	0	0	0	0	0	1	0.89000	81
1	0	0	0	0	0	1	0	0.89500	82
1	0	0	0	0	0	1	1	0.90000	83
1	0	0	0	0	1	0	0	0.90500	84
1	0	0	0	0	1	0	1	0.91000	85
1	0	0	0	0	1	1	0	0.91500	86
1	0	0	0	0	1	1	1	0.92000	87

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TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	0	0	1	0	0	0	0.92500	88
1	0	0	0	1	0	0	1	0.93000	89
1	0	0	0	1	0	1	0	0.93500	8A
1	0	0	0	1	0	1	1	0.94000	8B
1	0	0	0	1	1	0	0	0.94500	8C
1	0	0	0	1	1	0	1	0.95000	8D
1	0	0	0	1	1	1	0	0.95500	8E
1	0	0	0	1	1	1	1	0.96000	8F
1	0	0	1	0	0	0	0	0.96500	90
1	0	0	1	0	0	0	1	0.97000	91
1	0	0	1	0	0	1	0	0.97500	92
1	0	0	1	0	0	1	1	0.98000	93
1	0	0	1	0	1	0	0	0.98500	94
1	0	0	1	0	1	0	1	0.99000	95
1	0	0	1	0	1	1	0	0.99500	96
1	0	0	1	0	1	1	1	1.00000	97
1	0	0	1	1	0	0	0	1.00500	98
1	0	0	1	1	0	0	1	1.01000	99
1	0	0	1	1	0	1	0	1.01500	9A
1	0	0	1	1	0	1	1	1.02000	9B
1	0	0	1	1	1	0	0	1.02500	9C
1	0	0	1	1	1	0	1	1.03000	9D
1	0	0	1	1	1	1	0	1.03500	9E
1	0	0	1	1	1	1	1	1.04000	9F
1	0	1	0	0	0	0	0	1.04500	A0
1	0	1	0	0	0	0	1	1.05000	A1
1	0	1	0	0	0	1	0	1.05500	A2
1	0	1	0	0	0	1	1	1.06000	A3
1	0	1	0	0	1	0	0	1.06500	A4
1	0	1	0	0	1	0	1	1.07000	A5
1	0	1	0	0	1	1	0	1.07500	A6
1	0	1	0	0	1	1	1	1.08000	A7
1	0	1	0	1	0	0	0	1.08500	A8
1	0	1	0	1	0	0	1	1.09000	A9

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TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	1	0	1	0	1	0	1.09500	AA
1	0	1	0	1	0	1	1	1.10000	AB
1	0	1	0	1	1	0	0	1.10500	AC
1	0	1	0	1	1	0	1	1.11000	AD
1	0	1	0	1	1	1	0	1.11500	AE
1	0	1	0	1	1	1	1	1.12000	AF
1	0	1	1	0	0	0	0	1.12500	B0
1	0	1	1	0	0	0	1	1.13000	B1
1	0	1	1	0	0	1	0	1.13500	B2
1	0	1	1	0	0	1	1	1.14000	B3
1	0	1	1	0	1	0	0	1.14500	B4
1	0	1	1	0	1	0	1	1.15000	B5
1	0	1	1	0	1	1	0	1.15500	B6
1	0	1	1	0	1	1	1	1.16000	B7
1	0	1	1	1	0	0	0	1.16500	B8
1	0	1	1	1	0	0	1	1.17000	B9
1	0	1	1	1	0	1	0	1.17500	BA
1	0	1	1	1	0	1	1	1.18000	BB
1	0	1	1	1	1	0	0	1.18500	BC
1	0	1	1	1	1	0	1	1.19000	BD
1	0	1	1	1	1	1	0	1.19500	BE
1	0	1	1	1	1	1	1	1.20000	BF
1	1	0	0	0	0	0	0	1.20500	C0
1	1	0	0	0	0	0	1	1.21000	C1
1	1	0	0	0	0	1	0	1.21500	C2
1	1	0	0	0	0	1	1	1.22000	C3
1	1	0	0	0	1	0	0	1.22500	C4
1	1	0	0	0	1	0	1	1.23000	C5
1	1	0	0	0	1	1	0	1.23500	C6
1	1	0	0	0	1	1	1	1.24000	C7
1	1	0	0	1	0	0	0	1.24500	C8
1	1	0	0	1	0	0	1	1.25000	C9
1	1	0	0	1	0	1	0	1.25500	CA
1	1	0	0	1	0	1	1	1.26000	CB

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TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	0	0	1	1	0	0	1.26500	CC
1	1	0	0	1	1	0	1	1.27000	CD
1	1	0	0	1	1	1	0	1.27500	CE
1	1	0	0	1	1	1	1	1.28000	CF
1	1	0	1	0	0	0	0	1.28500	D0
1	1	0	1	0	0	0	1	1.29000	D1
1	1	0	1	0	0	1	0	1.29500	D2
1	1	0	1	0	0	1	1	1.30000	D3
1	1	0	1	0	1	0	0	1.30500	D4
1	1	0	1	0	1	0	1	1.31000	D5
1	1	0	1	0	1	1	0	1.31500	D6
1	1	0	1	0	1	1	1	1.32000	D7
1	1	0	1	1	0	0	0	1.32500	D8
1	1	0	1	1	0	0	1	1.33000	D9
1	1	0	1	1	0	1	0	1.33500	DA
1	1	0	1	1	0	1	1	1.34000	DB
1	1	0	1	1	1	0	0	1.34500	DC
1	1	0	1	1	1	0	1	1.35000	DD
1	1	0	1	1	1	1	0	1.35500	DE
1	1	0	1	1	1	1	1	1.36000	DF
1	1	1	0	0	0	0	0	1.36500	E0
1	1	1	0	0	0	0	1	1.37000	E1
1	1	1	0	0	0	1	0	1.37500	E2
1	1	1	0	0	0	1	1	1.38000	E3
1	1	1	0	0	1	0	0	1.38500	E4
1	1	1	0	0	1	0	1	1.39000	E5
1	1	1	0	0	1	1	0	1.39500	E6
1	1	1	0	0	1	1	1	1.40000	E7
1	1	1	0	1	0	0	0	1.40500	E8
1	1	1	0	1	0	0	1	1.41000	E9
1	1	1	0	1	0	1	0	1.41500	EA
1	1	1	0	1	0	1	1	1.42000	EB
1	1	1	0	1	1	0	0	1.42500	EC
1	1	1	0	1	1	0	1	1.43000	ED

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TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	1	0	1	1	1	0	1.43500	EE
1	1	1	0	1	1	1	1	1.44000	EF
1	1	1	1	0	0	0	0	1.44500	F0
1	1	1	1	0	0	0	1	1.45000	F1
1	1	1	1	0	0	1	0	1.45500	F2
1	1	1	1	0	0	1	1	1.46000	F3
1	1	1	1	0	1	0	0	1.46500	F4
1	1	1	1	0	1	0	1	1.47000	F5
1	1	1	1	0	1	1	0	1.47500	F6
1	1	1	1	0	1	1	1	1.48000	F7
1	1	1	1	1	0	0	0	1.48500	F8
1	1	1	1	1	0	0	1	1.49000	F9
1	1	1	1	1	0	1	0	1.49500	FA
1	1	1	1	1	0	1	1	1.50000	FB
1	1	1	1	1	1	0	0	1.50500	FC
1	1	1	1	1	1	0	1	1.51000	FD
1	1	1	1	1	1	1	0	1.51500	FE
1	1	1	1	1	1	1	1	1.52000	FF

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TABLE 7. STANDARD COMMAND CODES (PART 1)

Command Code	R/W	Default	Description	# Bytes	Comment
0x01	R/W	0x80	Operation	1	Operation command turns the device on or off in conjunction with EN signal.
					Bit / **Default** / **R/W** / **Comment**
					7 / 1 / R/W / 0: Immediate Off; 1: On (slew rate set by soft-start) Default
					6 / 0 / R / (Reserved for future use.)
					5:2 / 0000 / R / Margin Operation. (Reserved for future use.)
					1:0 / 00 / R / (Reserved for future use.)
0x02	R/W	0x17	ON_OFF_Config	1	Configures how the controller is turned on and off.
					Bit / **Default** / **R/W** / **Comment**
					7:5 / 000 / R / (Reserved for future use.)
					4 / 1 / R / Switching starts when commanded by the EN Pin and the Operation Command, as set in Bits 3:0
					3 / 0 / R/W / 0: Unit ignores OPERATION commands over the I^2C Interface 1: Unit responds to OPERATION command, power up may also depend upon EN input, as described in Bit 2
					2 / 1 / R / 0: Unit ignores EN pin 1: Unit responds EN pin, power up may also depend upon the Operation Register, as described for Bit 3
					1 / 1 / R / EN Pin polarity 0 = Active Low 1 = Active High
					0 / 1 / R / 1: When the controller is disabled it will immediately turn off (as set in the Operation Command)
0x03	W	NA	Clear_Faults	0	Writing any value to this command code will clear all Status Bits immediately. The ALERT# is deasserted on this command. If the fault is still present the fault bit shall immediately be asserted again. This command is write only. There is no data byte for this command.
0x19	R	0xB0	Capability	1	This command allows the host to get some information on the I^2C device.
					Bit / **Default** / **R/W** / **Comment**
					7 / 1 / R / PEC (Packet Error Checking is supported)
					6:5 / 01 / R / Supported maximum bus speed is 400 kHz
					4 / 1 / R / NCP81233 has an ALERT# pin and Alert Response Address (ARA) protocol is supported
					3:0 / 0000 / R / (Reserved for future use.)

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TABLE 7. STANDARD COMMAND CODES (PART 1) (continued)

Command Code	R/W	Default	Description	# Bytes	Comment
0x20	R	0x20	Vout_Mode	1	The NCP81233 supports VID mode for programming the output voltage.
0x21	R/W	0x0000	Vout_Command	2	Sets the output voltage using VID in low byte.
0x24	R/W	0x00FF	Vout_Max	2	Sets maximum output voltage (VID data format). (Reserved for future use.)
0xA4	R/W	0x0000	Vout_Min	2	Sets minimum output voltage (VID data format). (Reserved for future use.)
0x60	R/W	0x0000	TON_DELAY	2	Sets the delay time, in ms, from the end of system reset until the output voltage starts to rise. The lowest 4 bits of the high byte is valid, i.e. 0x0000 = 0ms 0x0100 = 1ms 0x0200 = 2ms … 0x0F00 = 15ms
0x78	R	0x00	STATUS BYTE	1	**Bit** / **Name** / **Description**
					7 / BUSY / A fault was declared because the NCP81233 was busy and unable to respond
					6 / OFF / This bit is set whenever the NCP81233 is not switching
					5 / VOUT_OV / This bit gets set whenever the NCP81233 goes into OVP (Abs OVP and/or Normal OVP) mode.
					4 / IOUT_OC / This bit gets set whenever the NCP81233 turns off due to an over current event.
					3 / VIN_UV / Not supported.
					2 / OT / This bit gets set whenever the NCP81233 turns off due to an over temperature event.
					1 / CML / This bit gets set whenever a communications or logic fault has occurred.
					0 / None of the Above / A fault has occurred which is not one of the above.

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TABLE 7. STANDARD COMMAND CODES (PART 1) (continued)

Command Code	R/W	Default	Description	# Bytes	Comment			
0x79	R	0x0000	STATUS WORD	2	**Byte**	**Bit**	**Name**	**Description**
					Low	7	BUSY	A fault was declared because the NCP81233 was busy and unable to respond.
						6	OFF	This bit is set whenever the NCP81233 is not switching.
						5	VOUT _OV	This bit gets set whenever the NCP81233 goes into OVP mode.
						4	IOUT_ OC	This bit gets set whenever the NCP81233 turns off due to an over current event.
						3	VIN_ UV	Not supported.
						2	OT	This bit gets set whenever the NCP81233 turns off due to an over temperature event.
						1	CML	This bit gets set whenever a communications or logic fault has occurred.
						0	None of the Above	A fault has occurred which is not one of the above.
					High	7	VOUT	This bit gets set whenever the measured output voltage goes outside its power good limits or an OVP/UVP event has taken place. i.e. any bit in Status VOUT is set.
						6	Iout/ Pout	This bit gets set whenever the measured output current or power exceeds its warning limit or goes into OCP. i.e. any bit in Status IOUT is set.
						5		(Reserved for future use.)
						4		(Reserved for future use.)
						3	POWER GOOD #	The VDD_PWRGD signal is deasserted. Same as Power-Good in General Status.
						2		(Reserved for future use.)

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Table 8. STANDARD COMMAND CODES (PART 2)

Command Code	R/W	Default	Description	# Bytes	Comment		
0x7A	R	0x00	STATUS VOUT	1	**Bit**	**Name**	**Description**
					7	VOUT_OVER VOLTAGE FAULT	This bit gets set whenever an OVP event takes place.
					6	VOUT_OVER VOLTAGE WARNING	This bit gets set whenever the measured output voltage goes above its power-good limit. (Reserved for future use.)
					5	VOUT_ UNDER VOLTAGE WARNING	This bit gets set whenever the measured output voltage goes below its power – good limit. (Reserved for future use.)
					4	VOUT_UNDE RVOLTAGE FAULT	This bit gets set whenever an UVP event takes place.
					3		(Reserved for future use.)
					2		(Reserved for future use.)
					1		(Reserved for future use.)
					0		(Reserved for future use.)
0x7B	R	0x00	STATUS IOUT	1	**Bit**	**Name**	**Description**
					7	IOUT_OVER CURRENT FAULT	This bit gets set if the NCP81233 turns off due to an OCP Event
					6		(Reserved for future use.)
					5	IOUT_OVER CURRENT WARNING	This bit gets set if IOUT exceeds its programmed high warning limit. (Reserved for future use.)
					4		(Reserved for future use.)
					3		(Reserved for future use.)
					2		(Reserved for future use.)
					1		(Reserved for future use.)
					0		(Reserved for future use.)
0x7E	R	0x00	STATUS CML	1	**Bit**	**Name**	**Description**
					7	INVALID COMMAND	Invalid or unsupported command is received. (Reserved for future use.)
					6	INVALID DATA	Invalid or unsupported data is received. (Reserved for future use.)
					5	PEC_FAULT	PEC failed. (Reserved for future use.)
					4		(Reserved for future use.)
					3		(Reserved for future use.)
					2		(Reserved for future use.)
					1	OTHERS	A communication fault other than the ones listed has occurred. (Reserved for future use.)
					0		(Reserved for future use.)

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Table 8. STANDARD COMMAND CODES (PART 2)(continued)

Command Code	R/W	Default	Description	# Bytes	Comment		
0x80	R	0x00	STATUS_ ALERT	1	**Bit**	**Name**	**Description**
					7		(Reserved for future use.)
					6		(Reserved for future use.)
					5		(Reserved for future use.)
					4		(Reserved for future use.)
					3		(Reserved for future use.)
					2	VMON WARN	Gets asserted when VMON exceeds it programmed WARN limits. (Reserved for future use.)
					1	VMON FAULT	Gets asserted when VMON exceeds it programmed FAULT limits. (Reserved for future use.)
					0		(Reserved for future use.)
0x8B	R	0x0000	Read_VOUT	2	Readback output voltage. Voltage is read back in VID Mode.		
0x8C	R	0x0000	Read_IOUT	2	Readback output current. Current is read back in Linear Mode with unit of Amp.		
0x99	R	0x1A	MFR_ID	1			
0x9A	R	0x1233	MFR_ MODEL	2			
0x9B	R	0x00	MFR_ REVISION	1			

Table 9. MANUFACTURER SPECIFIC COMMAND CODES

Command Code	R/W	Default	Description	# Bytes	Comment		
0xD0	R/W	0x00	Lock/Reset	1	**Bit**	**Name**	**Description**
					1	Reset	Resets all registers to their POR Value. Has no effect if Lock bit is set.
					0	Lock	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read*only and cannot be modified until the NCP81233 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable).

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Table 9. MANUFACTURER SPECIFIC COMMAND CODES (continued)

Command Code	R/W	Default	Description	# Bytes	Comment		
0xD6	R/W	0x00	Vout Slew Rate	1	**Bit**	**Name**	**Description**
					7:5	DVID Slew Rate	DVID Slew Rate is automatically set to the same value as soft-start slew rate after each startup, which is programmed by SS pin. After that, it can be adjusted by I^2C interface. 000 = 0.125mV/us 001 = 0.25mV/us 010 = 0.5mV/us 011 = 1mV/us 100 = 2mV/us 101 = 4mV/us 110 = 8mV/us 111= 16mV/us
					4:2		(Reserved for future use.)
					1		(Reserved for future use.)
					0		(Reserved for future use.)
0xDD	R	0x0000	Read_IMAX	2	Maximum load current value, which is set at IMAX pin. The unit is Amp.		
0xF9	R/W	0x00	Mask ALERT	1	**Bit**	**Name**	**Description**
					7	Mask VOUT	Masks any ALERT caused by bits in Status VOUT Register.
					6	Mask IOUT	Masks any ALERT caused by bits in Status IOUT Register.
					5	Mask OV FAULT	Masks any ALERT caused by OVP (Abs OVP and Normal OVP).
					4	Mask UV FAULT	Masks any ALERT caused by UVP.
					3	Mask OC FAULT	Masks any ALERT caused by OCP.
					2	Mask OT FAULT	Masks any ALERT caused by OTP.
					1	Mask CML	Masks any ALERT caused by bits in Status CML Register.
					0	VMON	Masks any ALERT caused by VMON exceeding its high or low limit. (Reserved for future use.)

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DETAILED DESCRIPTION

General

The NCP81233, a multi-phase synchronous buck controller with an I^2C interface, provides power management solutions for applications supported by DrMOS. It supports 1-, 2-, 3-, 4-, or 6-phase operation and provides differential voltage and current sense, flexible programming, and comprehensive protections.

Operation Modes

The number of operational phases is programmed at CONFIG pin as shown in Table 10. All used phases are paralleled together in output of power stage with a common voltage-sense feedback. All input pins of current senses in unused phases can be left float.

TABLE 10. CONFIG CONFIGURATION

CONFIG		
R_{CONFIG}	Phase Number	Phase Number
Float	PWM1+PWM2+PWM3+PWM4+PWM5+PWM6	6
Short to GND	PWM1+PWM2+PWM3+PWM4	4
33k	PWM1+PWM2+PWM3	3
13k	PWM1+PWM2	2
5.1k	PWM1	1

Other control functions can be programmed at MODE1 pin and MODE2 pin as shown in Table 11 and Table 12.

TABLE 11. MODE 1 CONFIGURATION

MODE1			
R_{MODE1}	OVP & UVP	OVP Option	OCP, UVP, OTP
Float	Enabled	Recoverable	Hiccup
33 k			Latch Off
20 k		Latch Off	Hiccup
13 k			Latch Off
8.2 k	Disabled	Disabled	Latch Off
5.1 k			
2.7 k			Hiccup
Short to GND			

TABLE 12. MODE 2 CONFIGURATION

MODE2			
R_{MODE2}	Regulation Reference	PIN 27 Function	OTP Option
Float	VBOOT/VID	VB_RST#	OTP1
33 k			OTP2
20 k		PSI	OTP1
13 k			OTP2
8.2 k	REFIN	PSI	OTP2
5.1 k			
2.7 k			OTP1
Short to GND			

In applications with an external analog reference input, the device needs to be programmed at MODE2 pin to select REFIN as the regulation reference. Once REFIN is selected as the regulation reference, the command Vout_Command through I^2C interface won't be proceeded and the readback result of the command Read_VOUT is FFh.

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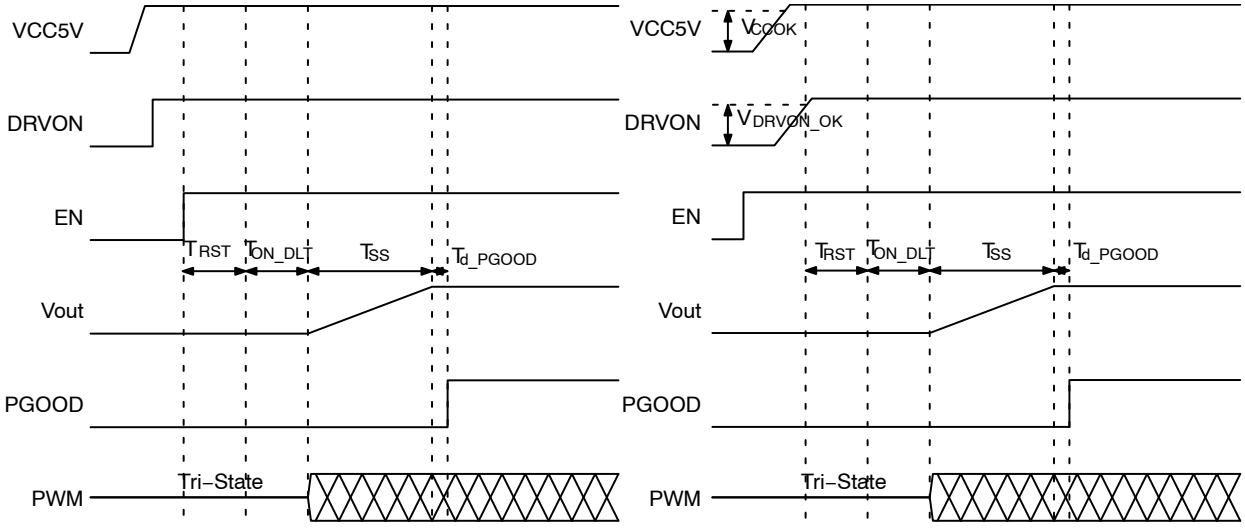
Power Sequence and Soft Start

The NCP81233 has a soft start function and the soft start slew rate is externally programmed at SS pins. The output starts to ramp up following a system reset period TRST and a programmable delay time T_{ON_DLY} after the device is enabled and VCC is ok. The system reset time is about 2 ms. The value of T_{ON_DLY} can be programmed by TON_DELAY command and the default value is zero. When the device is disabled or UVLO happens, the device shuts down immediately and all the PWM turn to Tri-State.



(1) VCC5V and DRVON Ready before EN

(2) VCC5V and DRVON Ready after EN

Figure 6. Timing Diagrams of Power Up Sequence

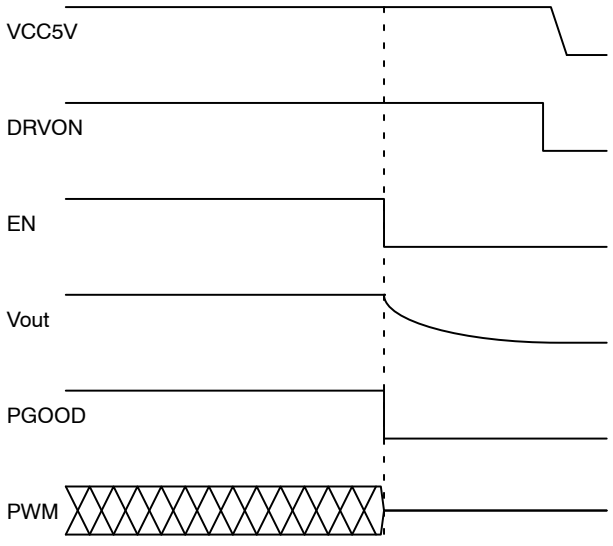


Figure 7. Timing Diagram of Power Down Sequence

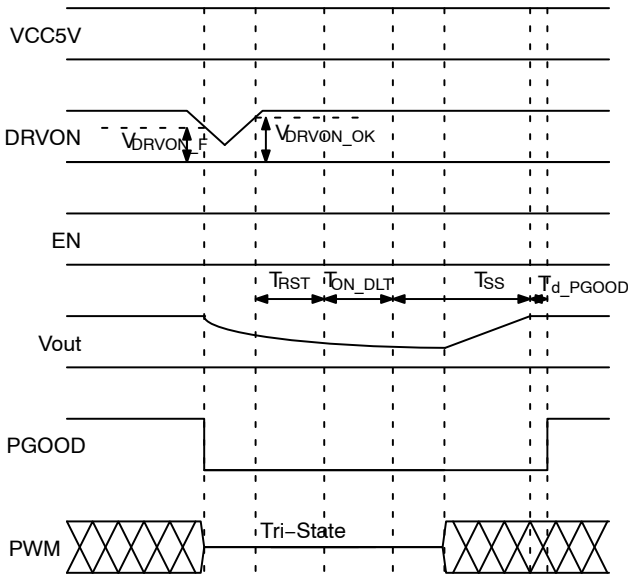


Figure 8. Timing Diagram of DRVON UVLO

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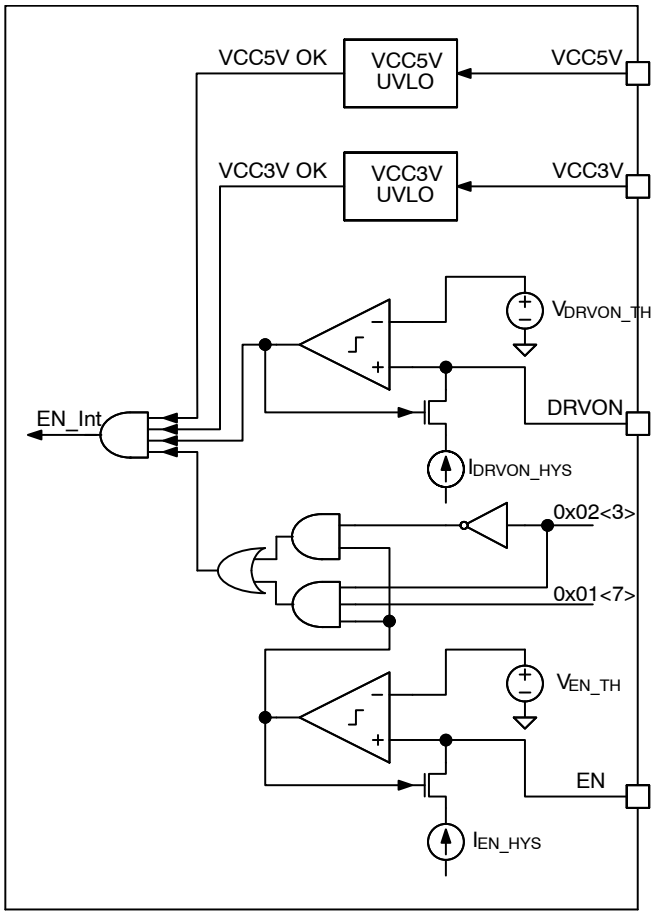

Figure 9. Enable, DRVON and UVLO

The device is able to start up smoothly under an output pre-biased condition without discharging the output before ramping up. In applications with external analog REFIN, soft start completes when the internal DAC reaches REFIN.

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Enable and Input UVLO

The NCP81233 is enabled when the voltage at EN pin is higher than an internal threshold V_{EN_TH} = 0.8 V.
A hysteresis can be programmed by an external resistor R_{EN} connected to EN pin as shown in Figure 10 The high threshold V_{EN_H} in ENABLE signal is

$$V_{EN_H} = V_{EN_TH} \quad \text{(eq. 1)}$$

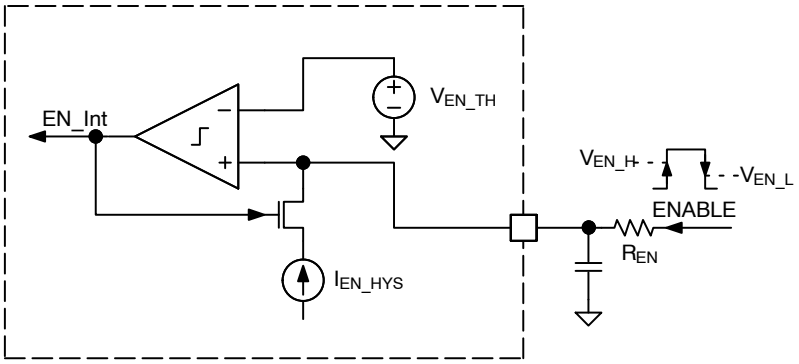

Figure 10. Enable and Hysteresis Programming

The low threshold V_{EN_L} in ENABLE signal is:

$$V_{EN_L} = V_{EN_TH} - V_{EN_HYS} \quad \text{(eq. 2)}$$

The hysteresis V_{EN_HYS} is:

$$V_{EN_HYS} = I_{EN_HYS} \times R_{EN} \quad \text{(eq. 3)}$$

A UVLO function for input power supply can be implemented at EN pin. As shown in Figure 11 the UVLO threshold can be programmed by two external resistors. The high threshold V_{IN_H} in VIN signal is:

$$V_{IN_H} = \left(\frac{R_{EN1}}{R_{EN2}} + 1\right) \times V_{EN_TH} \quad \text{(eq. 4)}$$

The low threshold V_{IN_L} in VIN signal is:

$$V_{IN_L} = V_{IN_H} - V_{IN_HYS} \quad \text{(eq. 5)}$$

The hysteresis V_{IN_HYS} is:

$$V_{IN_HYS} = I_{EN_HYS} \times R_{EN1} \quad \text{(eq. 6)}$$

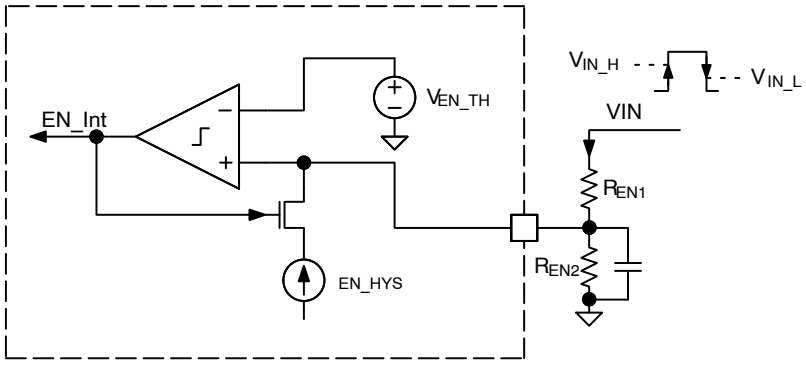

Figure 11. Enable and Input Supply UVLO Circuit

To avoid undefined operation, EN pin should not be left float in applications.

DRVON and DrMOS Power Monitor

The NCP81233 provides comprehensive power up sequence control including a DrMOS power monitor to ensure proper operation of DrMOS during power up and down.

Similar to the UVLO function for input power supply implemented at EN pin, as shown in Figure 12, the UVLO threshold for DrMOS power can be programmed by two external resistors. The high threshold V_{DRV_H} in the driver supply of DrMOS can be programmed as:

$$V_{DRV_H} = \left(\frac{R_{DRV1}}{R_{DRV2}} + 1\right) \times V_{DRVON_TH} \quad \text{(eq. 7)}$$

The low threshold V_{DRV_L} in the driver supply of DrMOS is:

$$V_{DRV_L} = V_{DRV_H} - V_{DRV_HYS} \quad \text{(eq. 8)}$$

The hysteresis V_{DRV_HYS} is

$$V_{DRV_HYS} = I_{DRVON_HYS} \times R_{DRV1} \quad \text{(eq. 9)}$$

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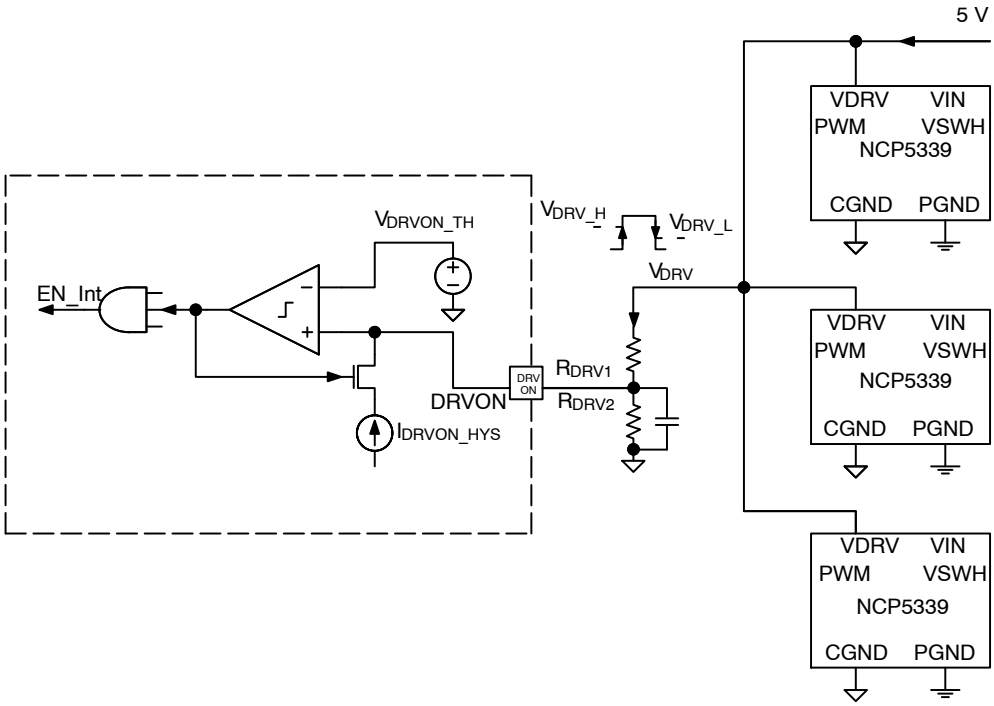

Figure 12. DRVON and DrMOS Supply UVLO Circuit

To avoid undefined operation, DRVON pin should not be left float in applications. In an application using phase doublers, DRVON pin may be used to monitor a common power supply shared by both phase doublers and DrMOSs.

VBOOT Restore

On condition that VBOOT Restore (VB_RST#) function is selected for pin 27 by function programming at MODE2 pin, the NCP81233 has a capability to restore to boot voltage once pin 27 is pulled low for more than 4ms after PGOOD is asserted. The output voltage slew rate has the same value as soft start.

Power Saving Interface (PSI)

On condition that PSI function is selected for pin 27 by function programming at MODE2 pin, the NCP81233 has 2 power operation modes responding to PSI levels as shown in Table 13. The operation modes can be changed on the fly after PGOOD is asserted. In PS0 mode, the operating phases are determined by the configuration programming at CONFIG pin. In PS1 mode, only PWM1 is active while high impedance in other PWM outputs.

TABLE 13. POWER SAVING INTERFACE (PSI) CONFIGURATIONS

PSI Level	Power Mode	Phase Configuration
High	PS0	Multi-Phase, FCCM
Low	PS1	1-Phase, FCCM

PWM Output

To be able to operate with diverse DrMOSs and phase doublers, the NCP81233 has 6 tri-level PWM outputs which may be connected to PWM inputs of these receivers. As shown in Figure 13, an internal transistor S_H in the NCP81233 pulls a PWM pin up to PVCC when outputs a high level and another internal transistor S_L pulls the PWM pin down to GND when outputs a low level. When there is a need to have a mid-level at the PWM input of a DrMOS or a phase doubler during power sequence or fault modes, both S_H and S_L are turned off and therefore the PWM output of the NCP81233 is left float. To well adapt the mid-level window of the receiver's PWM input, an external resistor divider composed of R_H and R_L is required in the connection between the NCP81233 and the receiver if no internal resistor divider in the receiver. Moreover, reduced input impedance by an external resistor also speeds up entering mid-level from either high level or low level for a receiver having an internal resistor divider.

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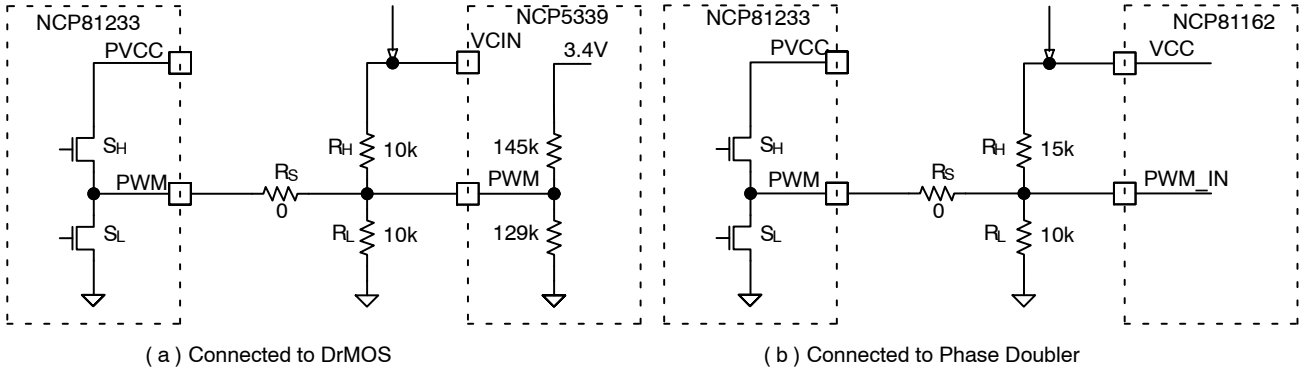

Figure 13. PWM Connections to DrMOS and Phase Doubler

The NCP81233 works with most of DrMOSs having either 5 V or 3.3 V PWM input logic. However, for some 3.3 V-logic DrMOSs having a low maximum voltage rating of PWM pins which is less than the PVCC level of the NCP81233, an additional resistor R_S may be inserted into the interconnection, as shown in Figure 13, to reduce the high voltage level. Note the insertion of R_S also raises the low voltage level at the PWM input of the receiver, so the resistance of R_S needs to be properly designed to meet the receiver's specification on both high level and low level.

Output Voltage Sensing and Regulation

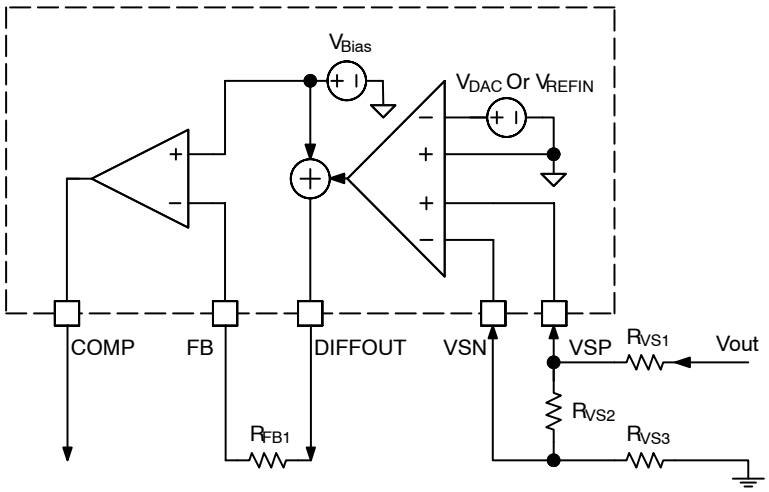

Figure 14. Output Voltage Sensing and Regulation

The NCP81233 has a differential voltage-sense amplifier. As shown in Figure 14, the remote voltage sensing points are connected to input pins VSP and VSN of the differential voltage-sense amplifier via a resistor network composed by R_{VS1}, R_{VS2}, and R_{VS3}. For applications with $V_{OUT} \le 1.52$ V, $R_{VS1} = R_{VS3} = 0\ \Omega$ or $100\ \Omega$ and R_{VS2} is left open. In steady-state, $V_{OUT} = V_{DAC}$. For applications with $V_{OUT} > 1.52$ V, the output voltage needs to be divided down by the resistor network to have VSP-VSN be within DAC range. Usually R_{VS3} is set to $0\ \Omega$ or $100\ \Omega$. Given a preset value of R_{VS2}, then the value of R_{VS1} can be obtained by

$$R_{VS1} = \frac{(V_{OUT} - V_{DAC}) \times R_{VS2}}{V_{DAC}} - R_{VS3} \quad \text{(eq. 10)}$$

A small offset voltage can also be added in output if needed. As shown in Figure 15, a resistor divider composed by R_1 and R_2 is connected from VREF to the negative remote sense point and feeds an offset voltage into VSN pin. By doing this way, the output voltage is:

$$V_{OUT} = V_{DAC} + V_{REF} \times \frac{R_1}{R_1 + R_2} \quad \text{(eq. 11)}$$

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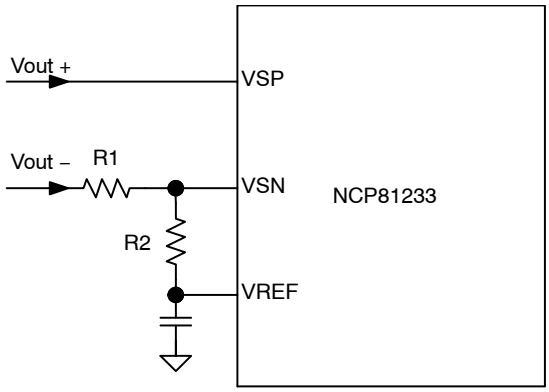

Figure 15. Adding Offset Voltage in Output

IMAX

The I²C interface conveys the platform IMAX value to the master by command Read_IMAX. A resistor R_{IMAX} from the IMAX pin to ground programs this register at the time the part is enabled. A 50 μA current is sourced out this pin to generate a voltage across the programming resistor. The maximum voltage at IMAX pin is 2 V and the maximum value in the IMAX register 0xDDh is 00FFh which is 255 in decimal. For applications with a maximum load I_{OUT_MAX} equal to or less than 255 A, the value $IMAX_{DDh}$ of the register is 1 A per LSB and directly represents I_{OUT_MAX}.

For applications with a maximum load IOUT_MAX greater than 255 A, the resistor should be equal or higher than 39.8 k, which results in 00FFh in the IMAX register.

$$IMAX_{DDh} = \begin{cases} I_{OUT_MAX} & \text{if } I_{OUT_MAX} \le 255\ A \\ 255 & \text{if } I_{OUT_MAX} > 255\ A \end{cases} \quad \text{(eq. 12)}$$

$$R_{IMAX} = \begin{cases} \dfrac{I_{OUT_MAX}}{6.4 \times 10^{-3}} & \text{if } I_{OUT_MAX} \le 255\ A \\ 39.8\ k\Omega \text{ or higher,} & \text{if } I_{OUT_MAX} > 255\ A \end{cases} \quad \text{(eq. 13)}$$

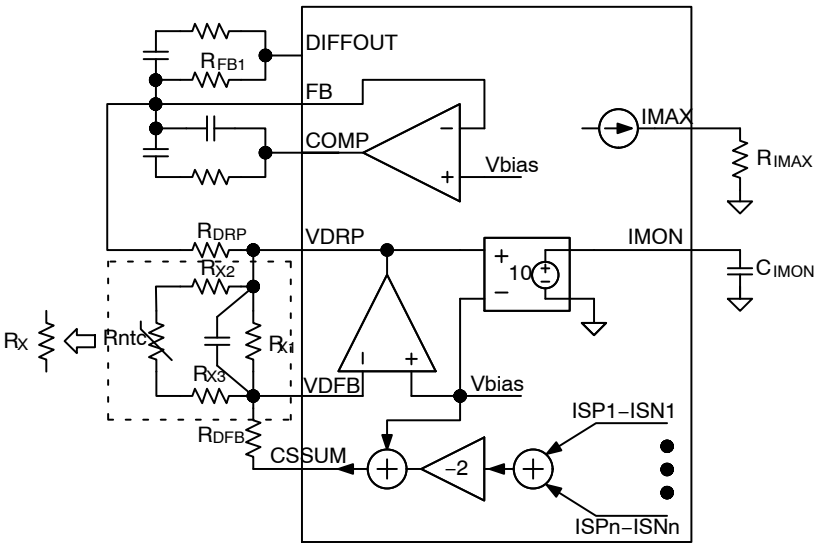

Figure 16. IMAX, IMON, and Load Line

IMON

The voltage of the IMON pin is monitored by the internal A/D converter and should be scaled with external resistors, R_X and R_{DFB}, surround the droop amplifier such that the maximum load current I_{OUT_MAX} in an application generates a 2 V signal at IMON pin. Therefore, the gain-up ratio R_X/R_{DFB} can be designed as below.

$$\frac{R_X}{R_{DFB}} = \frac{1}{10} \times \frac{1}{\sum_{n=1}^{N} (V_{ISPn} - V_{ISNn})} \quad \text{(eq. 14)}$$

R_X can be replaced by a resistor network with a NTC resistor to compensate temperature effect on the DCR of inductor. The filtered voltage at IMON pin is

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$$V_{IMON} = 20 \times \frac{R_X}{R_{DFB}} \times \Sigma_{n=1}^{N} (V_{ISPn} - V_{ISNn}) \quad \text{(eq. 15)}$$

The I^{2}C interface conveys the IOUT value to the master by command Read_IOUT. The maximum value in the IOUT register 0x8Ch is 00FFh which is 255 in decimal. For applications with a maximum load equal to or less than 255A, the value $IOUT_{8Ch}$ in the register is 1 A per LSB which directly represents the output load current value in Amperes. For applications with a maximum load greater than 255 A, the real output current value can be obtained from the reading $IOUT_{8Ch}$ in the register with a coefficient of $I_{OUT_MAX}/255$.

$$I_{OUT} = \begin{cases} IOUT_{8Ch} & \text{if } I_{OUT_MAX} \le 255\ A \\ \frac{IOUT_{8Ch}}{255} \times I_{OUT_MAX} & \text{if } I_{OUT_MAX} > 255\ A \end{cases} \quad \text{(eq. 16)}$$

Load Line Programming

In applications with a need of programmable load line, the output of the droop amplifier needs to be connected to FB pin by an external resistor RDRP as shown in Figure 16. Droop voltage VDROOP in DIFFOUT output can be obtained by:

$$V_{DROOP} = 2 \times \frac{R_{FB1}}{R_{DRP}} \times \frac{R_X}{R_{DFB}} \Sigma_{n=1}^{N} (V_{ISPn} - V_{ISNn}) \quad \text{(eq. 17)}$$

DC load line LL in output is:

$$LL = 2 \times \frac{R_{FB1}}{R_{DRP}} \times \frac{R_X}{R_{DFB}} \times \frac{R_{VS1} + R_{VS2} + R_{VS3}}{R_{VS2}} \times DCR \quad \text{(eq. 18)}$$

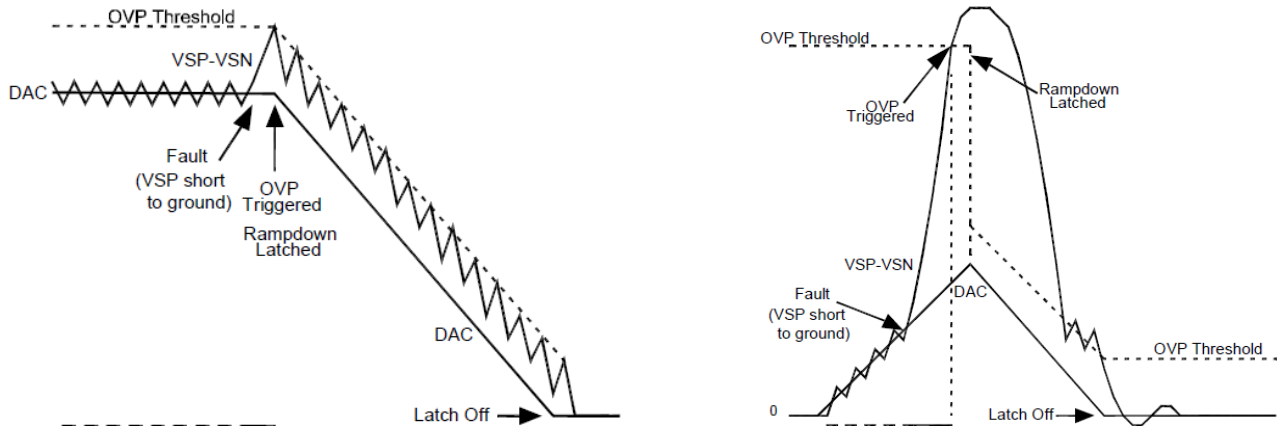
Over Voltage Protection (OVP)

By means of the configuration at MODE1 pin as shown in Table 11, the users can choose either recoverable OVP or latch-off OVP.

Recoverable OVP

During normal operation the output voltage is monitored at the differential inputs VSP and VSN. If VSP-VSN voltage exceeds the DAC+V_{OVTH} (or REFIN+V_{OVTH}) for more than 1us, over voltage protection OVP is triggered and PGOOD is pulled low. In the meanwhile, all the high-side MOSFETs are turned off and all the low-side MOSFETs are turned on. The over voltage protection can be cleared once VSP-VSN voltage drops 25mV lower than DAC+V_{OVTH} (or REFIN+V_{OVTH}), and then the system comes back to normal operation. During soft-start, the OVP threshold is set to 2.1V before PGOOD is asserted, but it changes to DAC+V_{OVTH} (or REFIN+V_{OVTH}) after OVP is triggered.

Latch-Off OVP



(a) Normal Operation Mode

(b) During Start Up

Figure 17. Function of Latch-Off Over Voltage Protection

During normal operation the output voltage is monitored at the differential inputs VSP and VSN. If VSP-VSN voltage exceeds the DAC+V_{OVTH} (or REFIN+V_{OVTH}) for more than 1us, over voltage protection OVP is triggered and PGOOD is pulled low. In the meanwhile, all the high-side MOSFETs are latched off and all the low-side MOSFETs are turned on. After the OVP trips, the DAC ramps slowly down to zero, having a slew rate of −0.5 mV/us to avoid a negative output voltage spike during shutdown. All the low-side MOSFETs toggle between on and off as the output voltage follows the DAC+V_{OVTH} (or REFIN+V_{OVTH}) down with a hysteresis of 25 mV. When the DAC gets to zero, all the high-side MOSFETs will be held off and all the low-side MOSFETs will remain on. During soft-start, the OVP threshold is set to 2.1 V, and it changes to DAC+V_{OVTH} (or REFIN+V_{OVTH}) after DAC starts to ramp down. To restart

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the device after latch-off OVP, the system needs to have either VCC5V or EN toggled state.

OVP detection starts from the beginning of soft-start time TSS and ends in shutdown, latch-off, and idle time of hiccup mode caused by other protections.

Under Voltage Protection (UVP)

The NCP81233 pulls PGOOD low and turns off both high-side MOSFETs and low-side MOSFETs with high impedance in all PWM outputs once VSP-VSN voltage drops below DAC-V_{UVTH} for more than 5μs. Under voltage protection operates in either a hiccup mode or ends in latch-off, which is programmable at MODE1 pin as shown in Table 11. A normal power up sequence happens after a hiccup interval. To restart the device after latch-off UVP, the system needs to have either VCC5V or EN toggled state.

UVP detection starts when PGOOD delay T_{d_PGOOD} is expired right after a soft start, and ends in shutdown, latch-off, and idle time of hiccup mode.

Over Current Protection (OCP)

The NCP81233 senses phase current by a differential current-sense amplifier and provides a cycle-by-cycle over current protection for each phase. If OCP happens in all the phases and lasts for more than 8 times of the switching cycle, the NCP81233 turns off both high-side MOSFETs and low-side MOSFETs with all PWM outputs in high impedance and enters into a hiccup mode or ends in latch-off, which is programmable at MODE1 pin as shown in Table 11. A normal power up sequence happens after a hiccup interval. To restart the device after latch-off OCP, the system needs to have either VCC5V or EN toggled state. The part may enter into hiccup mode or latch-off sooner due to the under voltage protection in a case if the output voltage drops down very fast.

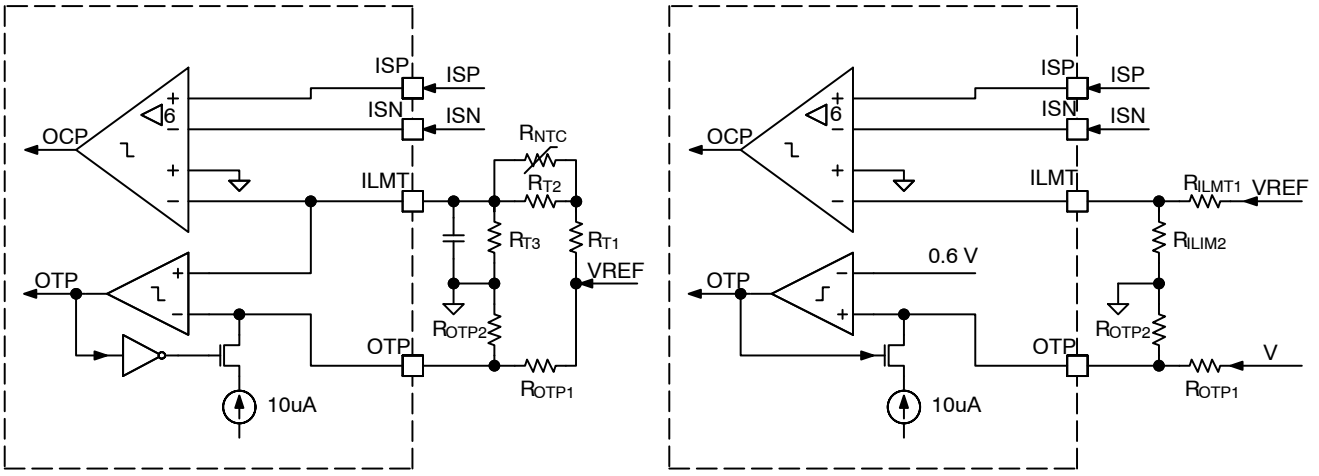

Figure 18. Over−Current Protection and Over−Temperature Protection

The over-current threshold can be externally programmed at the ILIM pin. As shown in Figure 18 (1), a NTC resistor R_{NTC} can be employed for temperature compensated over current protection. The peak current limit per phase can be calculated by

$$V_{ISP} - V_{ISN} = \frac{1}{6} \times \frac{R_{T3}}{R_{T1} + \frac{R_{T2} \times R_{NTC}}{R_{T2} + R_{NTC}} + R_{T3}} \times V_{REF} \quad \text{(eq. 19)}$$

If no temperature compensation is needed, as shown in Figure 18 (2), the peak current limit per phase can be simply set by

$$V_{ISP} - V_{ISN} = \frac{1}{6} \times \frac{R_{ILIM2}}{R_{ILIM1} + R_{ILIM2}} \times V_{REF} \quad \text{(eq. 20)}$$

OCP detection starts from the beginning of soft-start time TSS, and ends in shutdown and idle time of hiccup mode.

Over Temperature Protection (OTP)

The NCP81233 provides over temperature protection. To serve different types of DrMOS, one of two internal configurations of OTP detection can be selected at MODE2 pin as shown in Table 12.

With OTP Configuration 1, as shown in Figure 18 (1), the NTC resistor RNTC senses the hot-spot temperature and changes the voltage at ILMT pin. Both over-temperature threshold and hysteresis are externally programmed at OTP pin by a resistor divider. Once the voltage at ILMT pin is higher than the voltage at OTP pin, the NCP81233 turns off both high-side MOSFETs and low-side MOSFETs with all PWM outputs in high impedance and operates in either a hiccup mode or ends in latch-off, which is programmable at MODE1 pin as shown in Table 11. The controller will have

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a normal start up after a hiccup interval in condition that the temperature drops below the OTP reset threshold. To restart the device after latch-off OTP, the system needs to have either VCC5V or EN toggled state. The OTP assertion threshold VOTP and reset threshold VOTP_RST can be calculated by:

$$V_{OTP} = \frac{V_{REF} + I_{OTP_HYS} \times R_{OTP1}}{1 + \frac{R_{OTP1}}{R_{OTP2}}} \quad \text{(eq. 21)}$$

$$V_{OTP_RST} = \frac{V_{REF} \times R_{OTP2}}{R_{OTP1} + R_{OTP2}} \quad \text{(eq. 22)}$$

The corresponding OTP temperature TOTP and reset temperature T_{OTP_RST} can be calculated by

$$T_{OTP} = \frac{1}{\frac{\ln\left(R_{NTC_OTP}/R_{TNC}\right)}{B} + \frac{1}{25+273.15}} - 273.15 \quad \text{(eq. 23)}$$

$$T_{OTP_RST} = \frac{1}{\frac{\ln\left(R_{NTC_OTPRST}/R_{TNC}\right)}{B} + \frac{1}{25+273.15}} - 273.15 \quad \text{(eq. 24)}$$

Where:

$$R_{NTC_OTP} = \frac{1}{\frac{1}{R_{T_OTP} - R_{T1}} - \frac{1}{R_{T2}}} \quad \text{(eq. 25)}$$

$$R_{NTC_OTPRST} = \frac{1}{\frac{1}{R_{T_OTPRST} - R_{T1}} - \frac{1}{R_{T2}}} \quad \text{(eq. 26)}$$

$$R_{T_OTP} = \left(\frac{V_{REF}}{V_{OTP}} - 1\right) \times R_{T3} \quad \text{(eq. 27)}$$

$$R_{T_OTPRST} = \left(\frac{V_{REF}}{V_{OTP_RST}} - 1\right) \times R_{T3} \quad \text{(eq. 28)}$$

With OTP Configuration 2, as shown in Figure 18 (2), the NCP81233 receives an external signal VT linearly representing temperature and compares to an internal 0.6 V reference voltage. If the voltage is over the threshold OTP happens. The OTP assertion threshold V_{OTP} and reset threshold V_{OTP_RST} in this configuration can be obtained by

$$V_{T_OTP} = \left(1 + \frac{R_{OTP1}}{R_{OTP2}}\right) \times 0.6 \quad \text{(eq. 29)}$$

$$V_{T_OTP_RST} = \left(\frac{0.6}{R_{OTP2}} - I_{OTP_HYS}\right) \times R_{OTP1} + 0.6 \quad \text{(eq. 30)}$$

OTP detection starts from the beginning of soft-start time T_{SS}, and ends in shutdown, latch-off, and idle time of hiccup mode.

Thermal Shutdown (TSD)

The NCP81233 has an internal thermal shutdown protection to protect the device from overheating in an extreme case that the die temperature exceeds 150°C. TSD detection is activated when VCC5V, EN, and DRVON are valid. Once the thermal protection is triggered, the whole chip shuts down and all PWM signals are in high impedance. If the temperature drops below 125°C, the system automatically recovers and a normal power sequence follows.

I²C Interface

Control of the NCP81233 is carried out using the I²C Interface. The NCP81233 is connected to this bus as a slave device, under the control of a master controller. The master controller can start to access the NCP81233 via I²C after VCC5V is ready for more than 2 ms.

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as No Acknowledge. The master takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the NCP81233, write operations contain one, two or three bytes, and read operations contain one or two bytes. The command code or register address determines the number of bytes to be read or written, See the register map for more information.

To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed (i.e. command code), and then data can be written to that register or read from it. The first byte of a read or write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

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This write byte operation is shown in Figure 20. The device address is sent over the bus, and then R/W is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

- The read byte operation is shown in Figure 21. First the command code needs to be written to the NCP81233 so that the required data is sent back. This is done by performing a write to the NCP81233 as before, but only the data byte containing the register address is sent, because no data is written to the register. A repeated start is then issued and a read operation is then performed consisting of the serial bus address; R/W bit set to 1, followed by the data byte read from the data register.
- It is not possible to read or write a data byte from a data register without first writing to the address pointer register, even if the address pointer register is already at the correct value.
- In addition to supporting the send byte, the NCP81233 also supports the read byte, write byte, read word and write word protocols.

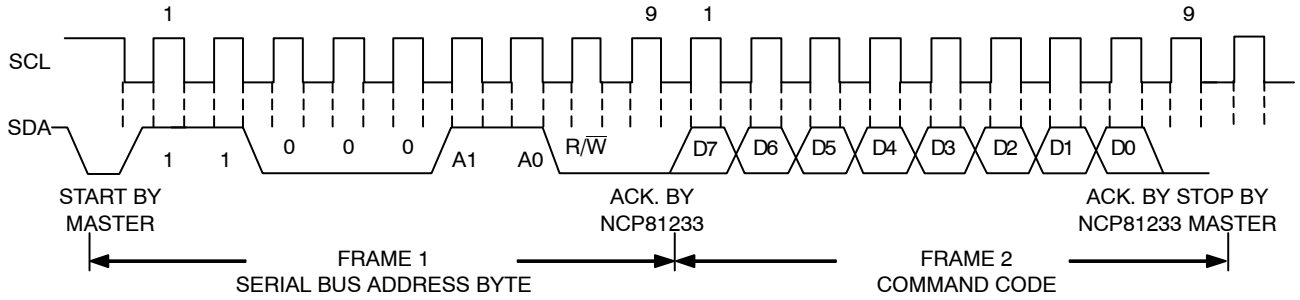

Figure 19. Send Byte

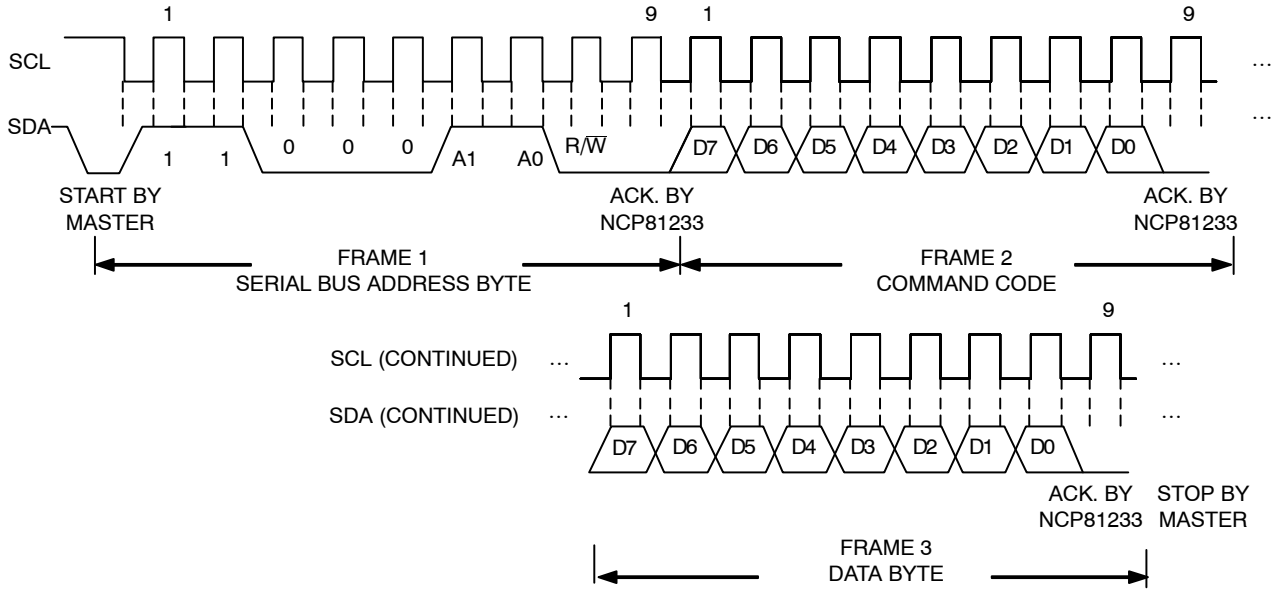

Figure 20. Write Byte

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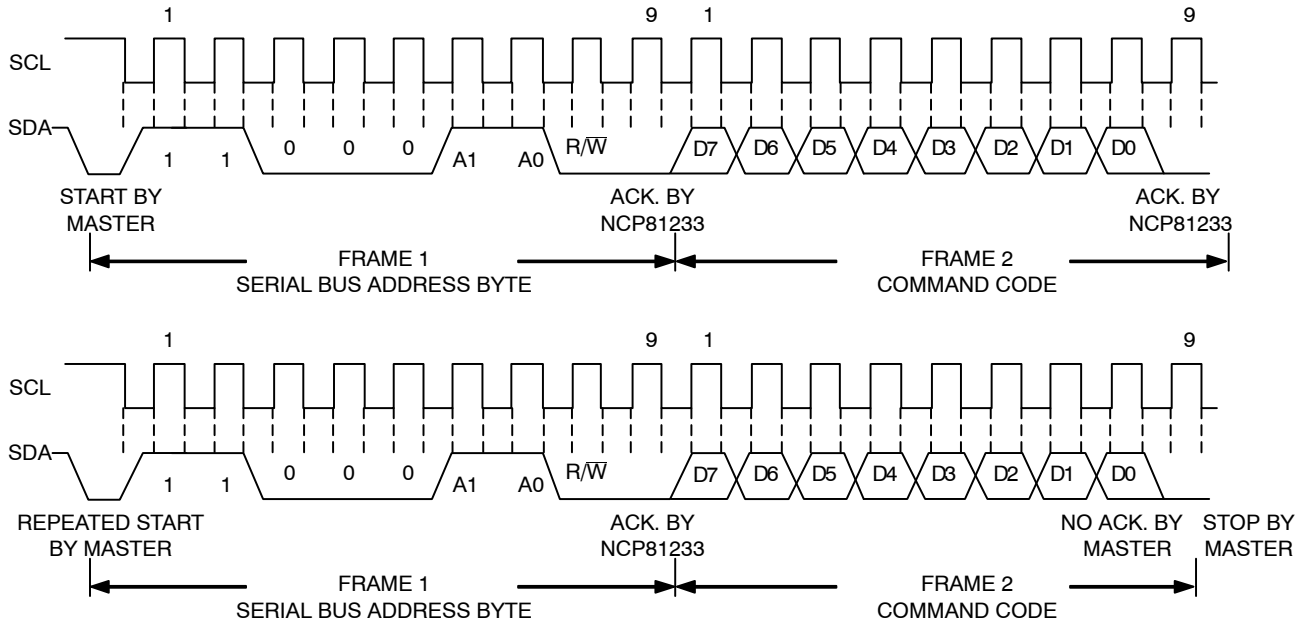

Figure 21. Read Byte

Write Operations

The I²C specification defines several protocols for different types of read and writes operations. The ones used in the NCP81233 are discussed in this section. The following abbreviations are used in the diagrams:

S—START
P—STOP
R—READ
W—WRITE
A—ACKNOWLEDGE
$\overline{A}$—NO ACKNOWLEDGE

The NCP81233 uses the following I²C write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the NCP81233, the send byte protocol is used to clear faults. This operation is shown in Figure 22.

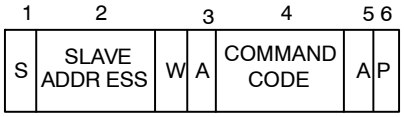

Figure 22. Send Byte Command

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA and the transaction ends.

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The byte write operation is shown in Figure 23

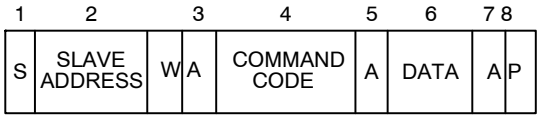

Figure 23. Single Byte Write to a Register

Write Word

In this operation, the master device sends a command byte and two data bytes to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the first data byte.
7. The slave asserts ACK on SDA.
8. The master sends the second data byte.
9. The slave asserts ACK on SDA.
10. The master asserts a stop condition on SDA and the transaction ends.

The word write operation is shown in Figure 24.

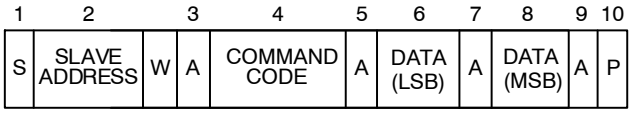

Figure 24. Single Word Write to a Register

Block Write

In this operation, the master device sends a command byte and a byte count followed by the stated number of data bytes to the slave device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the byte count N.
7. The slave asserts ACK on SDA.
8. The master sends the first data byte.
9. The slave asserts ACK on SDA.
10. The master sends the second data byte.
11. The slave asserts ACK on SDA.
12. The master sends the remainder of the data byes.
13. The slave asserts an ACK on SDA after each data byte.
14. After the last data byte the master asserts a STOP condition on SDA.

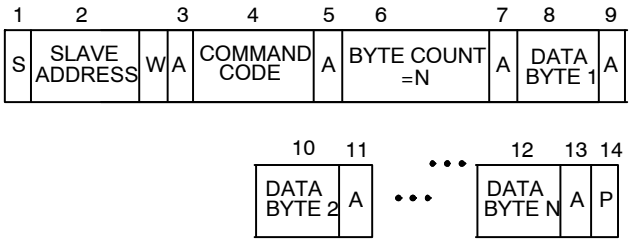

Figure 25. Block Write to a Register

Read Operations

The NCP81233 uses the following I^2C read protocols.

Read Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the Data Byte.
10. The master asserts NO ACK on SDA.
11. The master asserts a stop condition on SDA and the transaction ends.

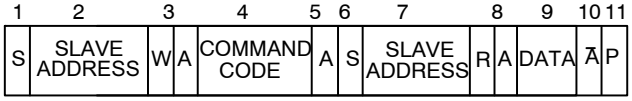

Figure 26. Single Byte Read to a Register

Read Word

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In this operation, the master device receives two data bytes from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. he master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the first Data Byte (low Data Byte).
10. The master asserts ACK on SDA.
11. The slave sends the second Data Byte (high Data Byte).
12. The master asserts a No ACK on SDA.
13. The master asserts a stop condition on SDA and the transaction ends.

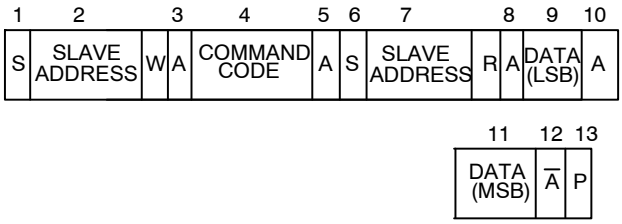

Figure 27. Single Word Read to a Register

Block Read

In this operation, the master device sends a command byte, the slave sends a byte count followed by the stated number of data bytes to the master device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a REPEATED START condition on SDA
5. The master sends the 7-bit slave address followed by the read bit (high).
6. The slave asserts ACK on SDA.
7. The slave sends the byte count N.
8. The master asserts ACK on SDA.
9. The slave sends the first data byte.
10. The master asserts ACK on SDA.
11. The slave sends the remainder of the data byes, the master asserts an ACK on SDA after each data byte.
12. After the last data byte the master asserts a No ACK on SDA.
13. The master asserts a STOP condition on SDA.

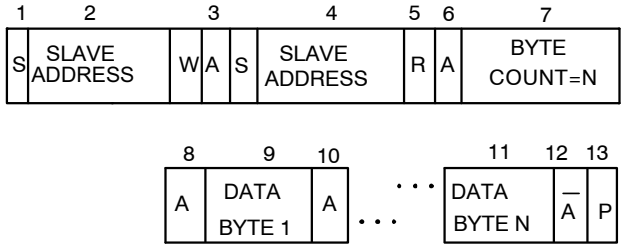

Figure 28. Block Write to a Command Coder

ALERT# Signal

The NCP81233 has an ALERT# output to notify the host of fault or warning conditions and also supports the Alert Response Address (ARA) protocol. ALERT# pin is an open-drain output. It is pulled low whenever at least one bit in the status registers is asserted with the following exception, on condition that the corresponding alert is not masked in the Mask Alert register. Bit 6 in Status Byte and Bit 3 in the high byte of Status Word have no impact on ALERT#.

A broadcast address used by the system host as part of the Alert Response Protocol initiated when a device asserts the ALERT# signal. The Alert Response Address (0001 100b) can be a substitute for device master capability. The host processes the interrupt and simultaneously accesses all ALERT# devices through the Alert Response Address. Only the device(s) which pulled ALERT# low will acknowledge the Alert Response Address. The host performs a modified Receive Byte operation. The 7 bit device address provided by the slave transmit device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

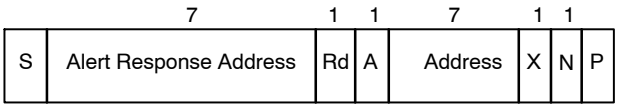

Figure 29. Alert Response Address Command

If more than one device pulls ALERT# low, the highest priority (lowest address) device will win communication rights via standard arbitration during the slave address transfer. A host which does not implement the ALERT# signal may periodically access the ARA.

Timeout

The NCP81233 includes a timeout feature. If there is no activity for 35 ms, the NCP81233 assumes that the bus is locked and releases the bus. This prevents the device from

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locking or holding the expecting data. Some controllers cannot handle the timeout feature, so it can be disabled.

Configuration Register 1 (0xD1)

Bit 3 BUS_TO_EN = 1; timeout enabled.

Bit 3 TODIS = 0; timeout disabled (default).

Virus Protection

To prevent rogue programs or viruses from accessing critical NCP81233 register settings, the lock bit can be set. Setting Bit 0 of the Lock/Reset sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the NCP81233 is powered down and powered up again. For more information on which registers are locked see the register map.

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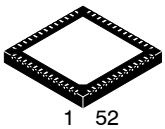
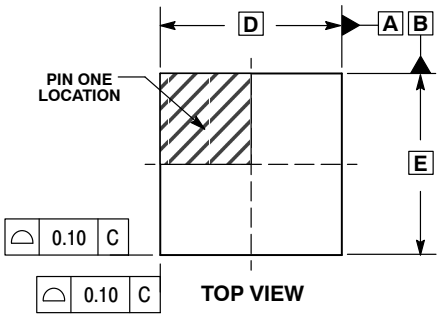
QFN52 6x6, 0.4P
CASE 485BE
ISSUE B

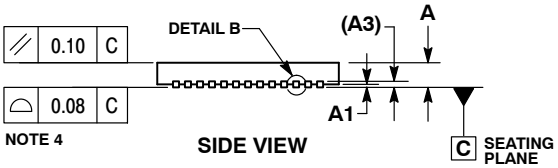
DATE 23 JUN 2010



SCALE 2:1

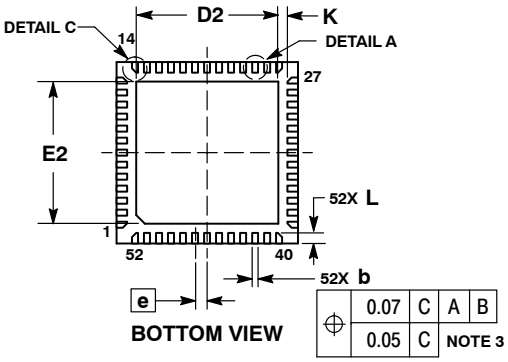


TOP VIEW



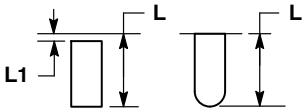
NOTE 4

SIDE VIEW

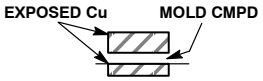


NOTE 3

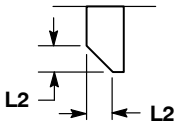
BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



DETAIL C
8 PLACES

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

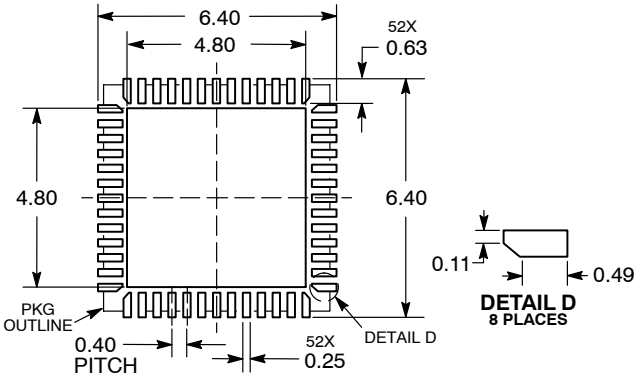
GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DETAIL D
8 PLACES

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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