MOSFET – Power, Single N-Channel

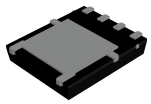
40 V, 4.2 mΩ, 120 A

NVMFS5832NL

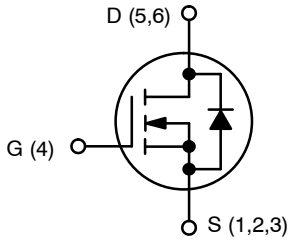
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	4.2 mΩ @ 10 V	120 A
	6.5 mΩ @ 4.5 V	

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5832NLWF - Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant



DFNW5
CASE 507BA



N-CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			40	V
V_{GS}	Gate-to-Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\Psi J\text{-}mb}$ (Notes 1, 2, 3, 4)	Steady State	T_{mb} = 25 °C	120	A
			T_{mb} = 100 °C	84	
P_D	Power Dissipation $R_{\Psi J\text{-}mb}$ (Notes 1, 2, 3)		T_{mb} = 25 °C	127	W
			T_{mb} = 100 °C	64	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State	T_A = 25 °C	21	A
			T_A = 100 °C	15	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)		T_A = 25 °C	3.7	W
			T_A = 100 °C	1.9	
I_{DM}	Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		557	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to +175	°C
I_S	Source Current (Body Diode)			120	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy (T_J = 25 °C, V_{GS} = 10 V, $I_{L(pk)}$ = 52 A, L = 0.1 mH, R_G = 25 Ω)			134	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

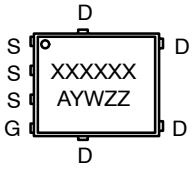
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\Psi J\text{-}mb}$	Junction-to-Mounting Board (top) - Steady State (Notes 2, 3)	1.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Note 3)	40	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		40	–	–	V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			–	34.2	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C	–	–	1	μA
			T_J = 125 °C	–	–	100	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS (Note 5)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.4	–	2.4	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient			–	6.4	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 10 V	I_D = 20 A	–	3.1	4.2	mΩ
		V_{GS} = 4.5 V	I_D = 20 A	–	5.0	6.5	
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 20 A		–	21	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V		–	2700	–	pF
C_{OSS}	Output Capacitance			–	360	–	
C_{RSS}	Reverse Transfer Capacitance			–	250	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 20 A		–	25	–	nC
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 20 A		–	51	–	
$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 20 A		–	2.0	–	
Q_{GS}	Gate-to-Source Charge			–	8.0	–	
Q_{GD}	Gate-to-Drain Charge			–	12.7	–	
V_{GP}	Plateau Voltage			–	3.2	–	V
SWITCHING CHARACTERISTICS (Note 6)							
$t_{d(ON)}$	Turn-On Delay Time	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 10 A, R_G = 1.0 Ω		–	13	–	ns
t_r	Rise Time			–	24	–	
$t_{d(OFF)}$	Turn-Off Delay Time			–	27	–	
t_f	Fall Time			–	8.0	–	
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 5 A	T_J = 25 °C	–	0.73	1.2	V
			T_J = 125 °C	–	0.57	–	
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 10 A		–	28.6	–	ns
t_a	Charge Time			–	14	–	
t_b	Discharge Time			–	14.5	–	
Q_{RR}	Reverse Recovery Charge			–	23.4	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Test: pulse width ≤ 300 μs, duty cycle ≤ 2%..
6. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

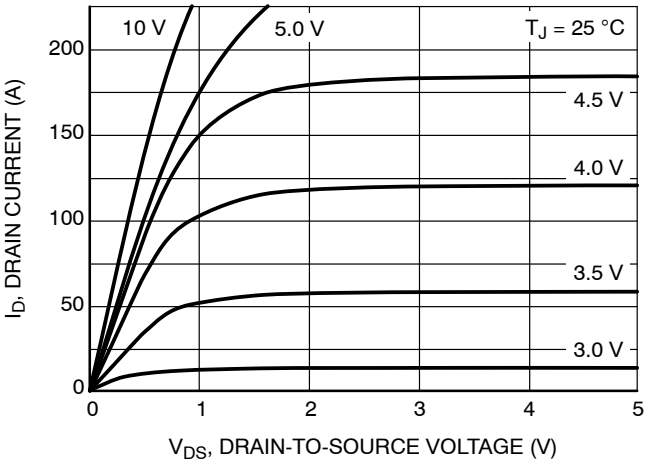


Figure 1. On-Region Characteristics

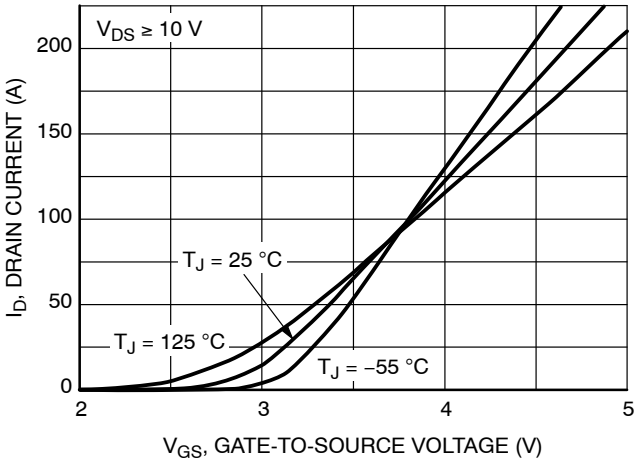


Figure 2. Transfer Characteristics

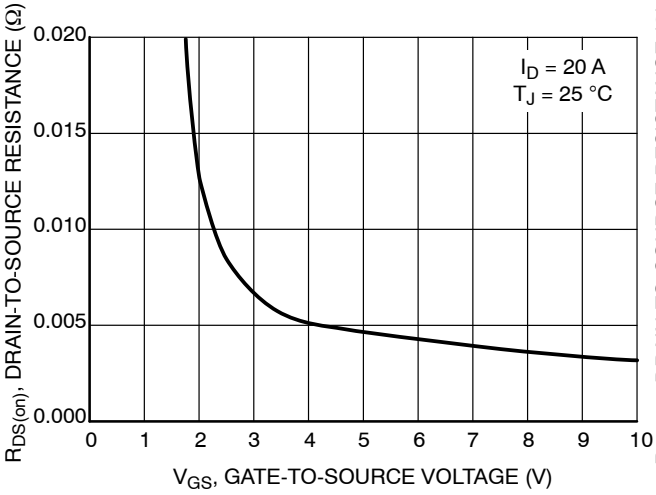


Figure 3. On-Resistance vs. Gate-to-Source Voltage

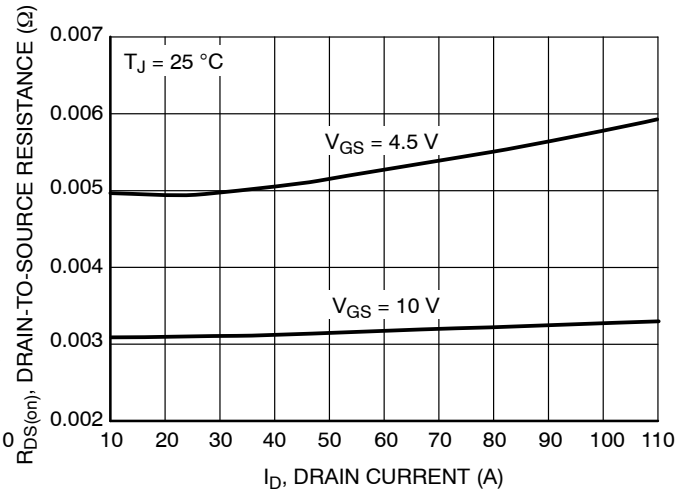


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

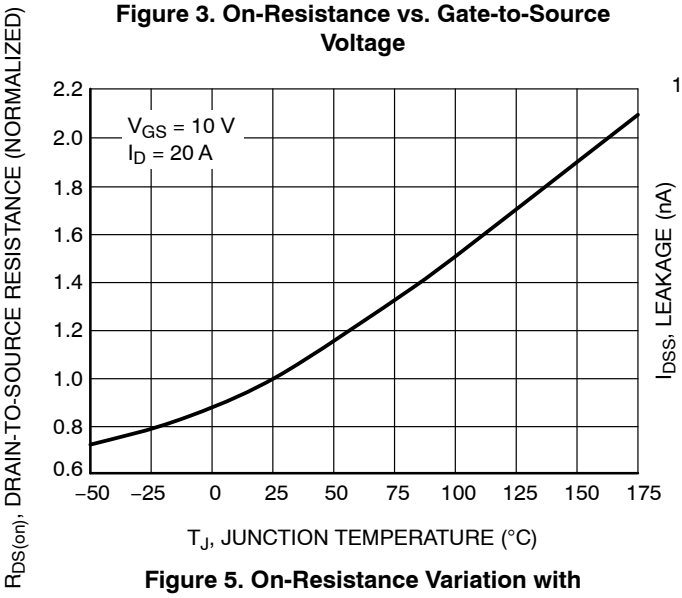


Figure 5. On-Resistance Variation with Temperature

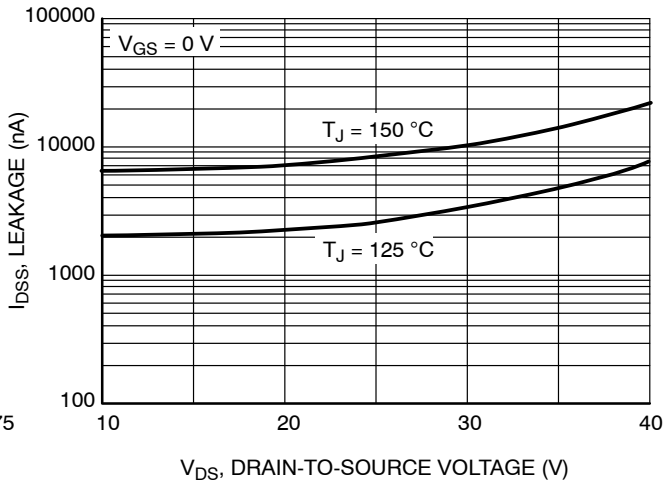


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

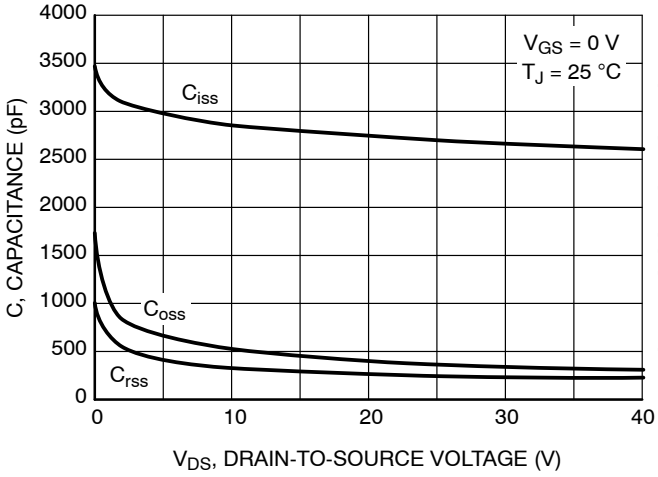


Figure 7. Capacitance Variation

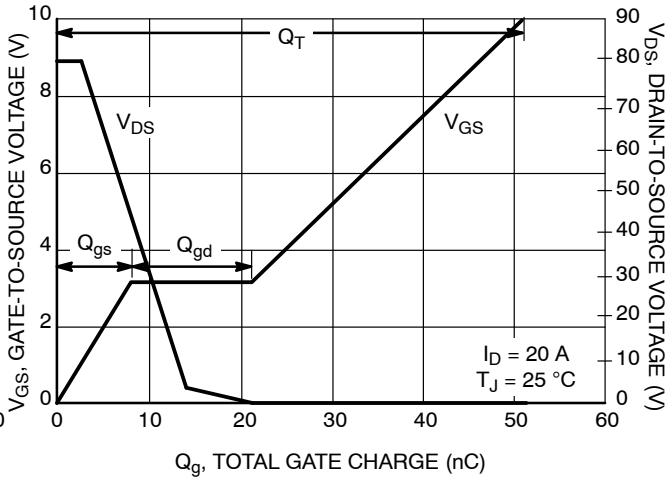


Figure 8. Gate-to-Source Voltage vs. Total Charge

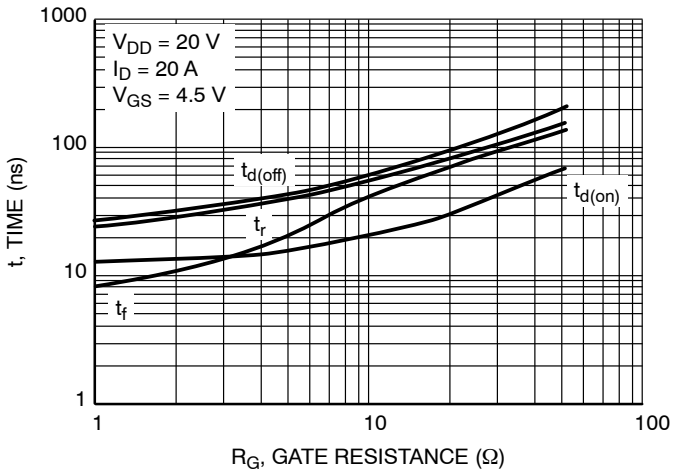


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

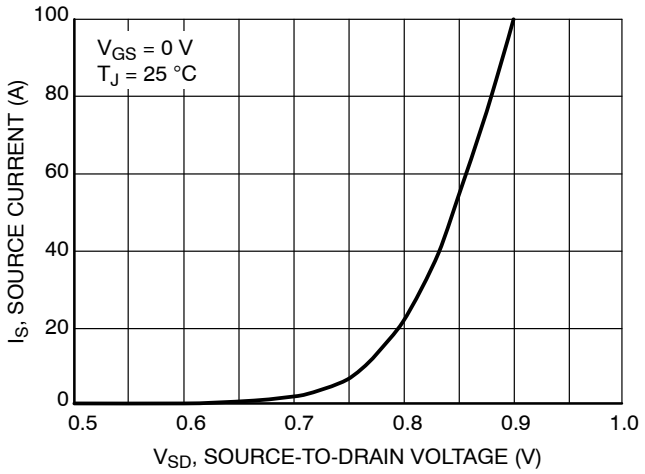


Figure 10. Diode Forward Voltage vs. Current

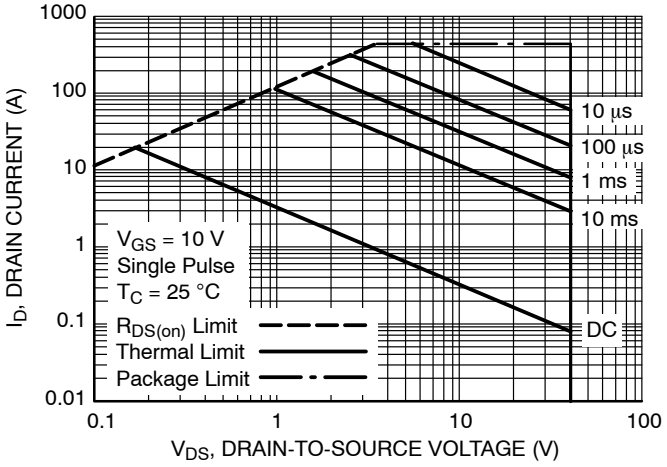


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS (continued)

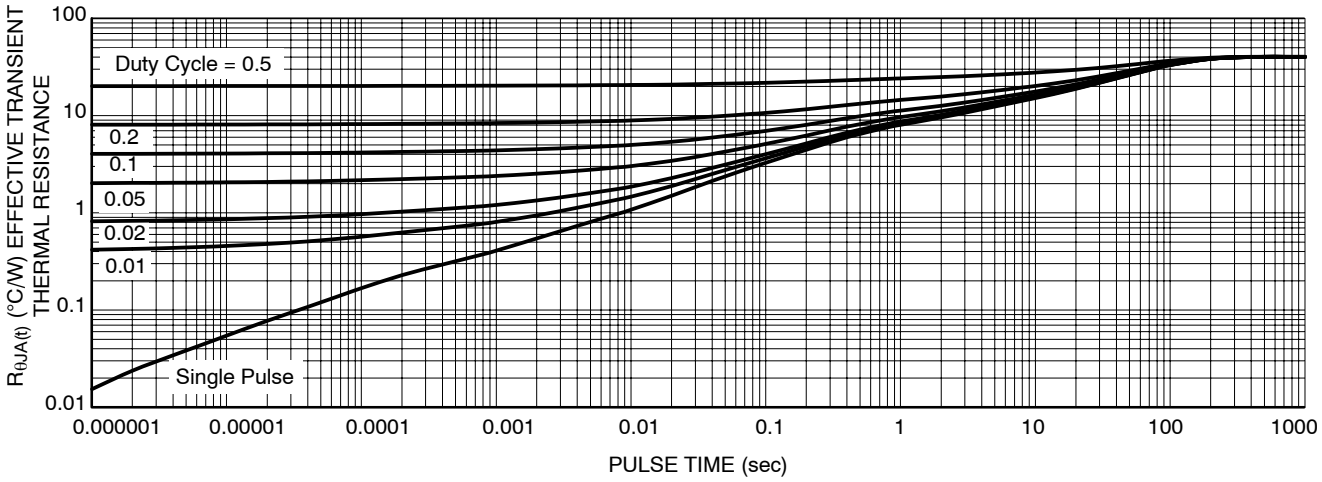


Figure 12. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS5832NLWFT1G-UM	5832LW	DFNW5 (Pb-Free)	1,500 / Tape & Reel

DISCONTINUED (Note 7)

NVMFS5832NLT1G	V5832L	DFN5 (Pb-Free)	1,500 / Tape & Reel
NVMFS5832NLWFT1G	5832LW	DFN5 (Pb-Free)	1,500 / Tape & Reel
NVMFS5832NLT3G	V5832L	DFN5 (Pb-Free)	5,000 / Tape & Reel
NVMFS5832NLWFT3G	5832LW	DFN5 (Pb-Free)	5,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

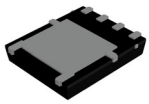
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REVISION HISTORY

Revision	Description of Changes	Date
5	Datasheet reactivated due to active NVMFS5832NLWFT1G-UM part and rebranded to **onsemi**.	11/13/2025

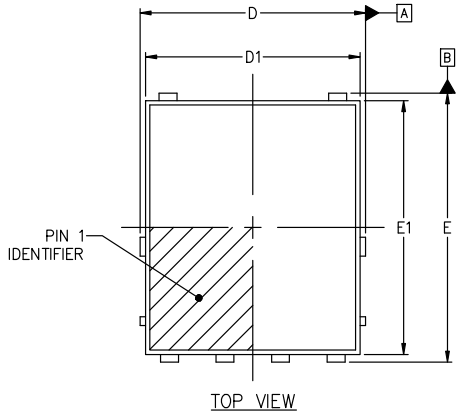
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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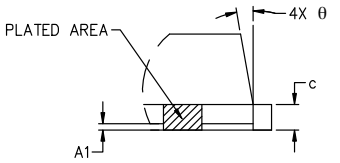
DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

DATE 19 SEP 2024

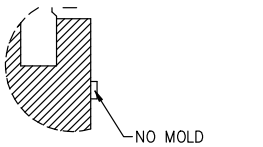


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

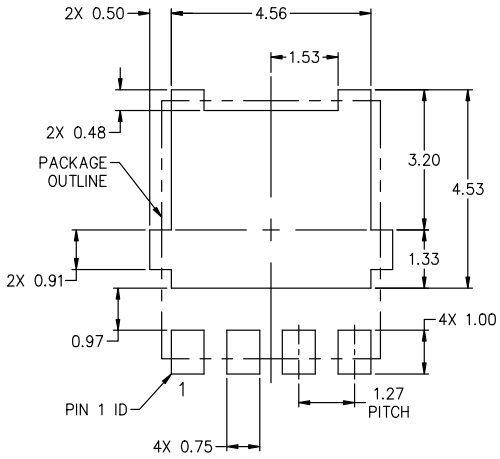


DETAIL "A"
SCALE 2:1



DETAIL "B"
SCALE 2:1

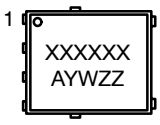
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW5 4.90x5.90x1.00, 1.27P**	**PAGE 1 OF 1**

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