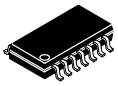
# Quad 2-Input “NAND” Schmitt Trigger

# MC14093B



SOIC-14
D SUFFIX
CASE 751A



SOEIAJ-14
F SUFFIX
CASE 965



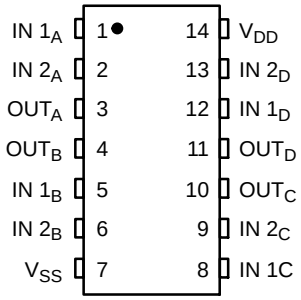
TSSOP-14
DT SUFFIX
CASE 948G

The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to “square up” slowly changing waveforms.

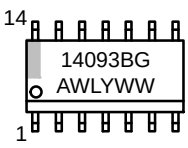
### Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B
- Independent Schmitt-Trigger at each Input
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

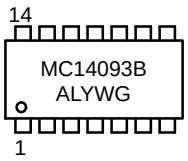
### PIN ASSIGNMENT



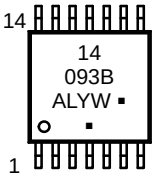

### MARKING DIAGRAMS




SOIC-14




SOEIAJ-14




TSSOP-14

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8-Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C From 65 °C To 125 °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

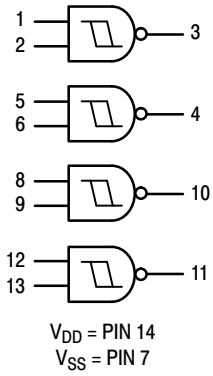
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

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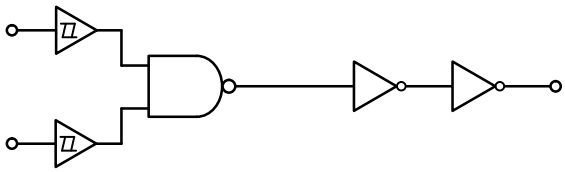
## LOGIC DIAGRAM




$V_{DD}$ = PIN 14
$V_{SS}$ = PIN 7

## EQUIVALENT CIRCUIT SCHEMATIC

(1/4 OF CIRCUIT SHOWN)



## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC14093BDG | SOIC-14<br>(Pb-Free) | 55 Units / Rail |
| MC14093BDR2G | SOIC-14<br>(Pb-Free) | 2500 Units / Tape & Reel |
| NLV14093BDR2G* | SOIC-14<br>(Pb-Free) | 2500 Units / Tape & Reel |
| MC14093BDTR2G | TSSOP-14<br>(Pb-Free) | 2500 Units / Tape & Reel |
| NLV14093BDTR2G* | TSSOP-14<br>(Pb-Free) | 2500 Units / Tape & Reel |

**DISCONTINUED** (Note 2)

| | | |
|---|---|---|
| NLV14093BDG* | SOIC-14<br>(Pb-Free) | 55 Units / Rail |
| MC14093BFELG | SOEIAJ-14<br>(Pb-Free) | 2000 Units / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

2. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



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**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | −55 °C Min | −55 °C Max | 25 °C Min | 25 °C Typ (Note 3) | 25 °C Max | 125 °C Min | 125 °C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0<br>0<br>0 | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | Vdc |
| “1” Level<br>$V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0<br>10<br>15 | 4.95<br>9.95<br>14.95 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | 5.0<br>10<br>15 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | –<br>–<br>– | Vdc |
| Output Drive Current | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | –3.0 | – | –2.4 | –4.2 | – | –1.7 | – | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | –0.64 | – | –0.51 | –0.88 | – | –0.36 | – | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | –1.6 | – | –1.3 | –2.25 | – | –0.9 | – | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | –4.2 | – | –3.4 | –8.8 | – | –2.4 | – | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0<br>10<br>15 | –<br>–<br>– | 0.25<br>0.5<br>1.0 | –<br>–<br>– | 0.0005<br>0.0010<br>0.0015 | 0.25<br>0.5<br>1.0 | –<br>–<br>– | 7.5<br>15<br>30 | μAdc |
| Total Supply Current (Notes 4 & 5) (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0<br>10<br>15 | $I_T$ = (1.2 μA/kHz) f + $I_{DD}$<br>$I_T$ = (2.4 μA/kHz) f + $I_{DD}$<br>$I_T$ = (3.6 μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |
| Hysteresis Voltage | $V_H$† | 5.0<br>10<br>15 | 0.3<br>1.2<br>1.6 | 2.0<br>3.4<br>5.0 | 0.3<br>1.2<br>1.6 | 1.1<br>1.7<br>2.1 | 2.0<br>3.4<br>5.0 | 0.3<br>1.2<br>1.6 | 2.0<br>3.4<br>5.0 | Vdc |
| Threshold Voltage | | | | | | | | | | Vdc |
| Positive-Going | $V_{T+}$ | 5.0<br>10<br>15 | 2.2<br>4.6<br>6.8 | 3.6<br>7.1<br>10.8 | 2.2<br>4.6<br>6.8 | 2.9<br>5.9<br>8.8 | 3.6<br>7.1<br>10.8 | 2.2<br>4.6<br>6.8 | 3.6<br>7.1<br>10.8 | |
| Negative-Going | $V_{T-}$ | 5.0<br>10<br>15 | 0.9<br>2.5<br>4.0 | 2.8<br>5.2<br>7.4 | 0.9<br>2.5<br>4.0 | 1.9<br>3.9<br>5.8 | 2.8<br>5.2<br>7.4 | 0.9<br>2.5<br>4.0 | 2.8<br>5.2<br>7.4 | Vdc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25 °C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in μA (per package), $C_L$ in pF, V = ($V_{DD}$ − $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.004.



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**SWITCHING CHARACTERISTICS** ($C_L$ = 50 pF, $T_A$ = 25 °C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | 5.0<br>10<br>15 | –<br>–<br>– | 100<br>50<br>40 | 200<br>100<br>80 | ns |
| Output Fall Time | $t_{THL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 100<br>50<br>40 | 200<br>100<br>80 | ns |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 125<br>50<br>40 | 250<br>100<br>80 | ns |

6. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

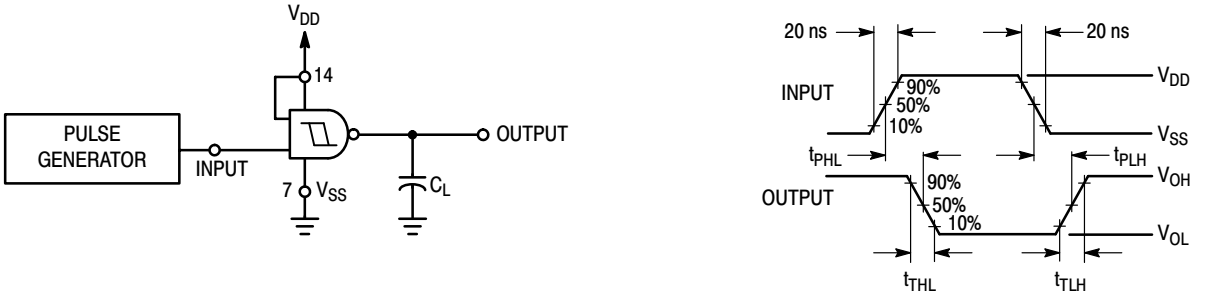
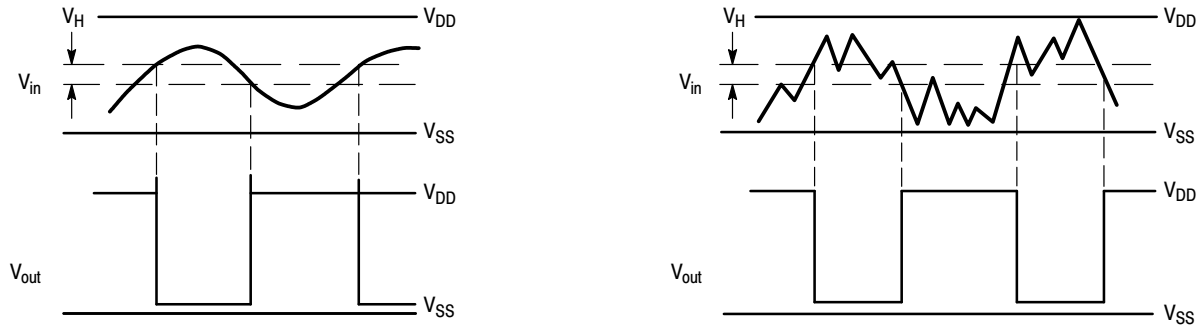



**Figure 1. Switching Time Test Circuit and Waveforms**




**(a) Schmitt Triggers will square up inputs with slow rise and fall times.**

**(b) A Schmitt trigger offers maximum noise immunity in gate applications.**

**Figure 2. Typical Schmitt Trigger Applications**



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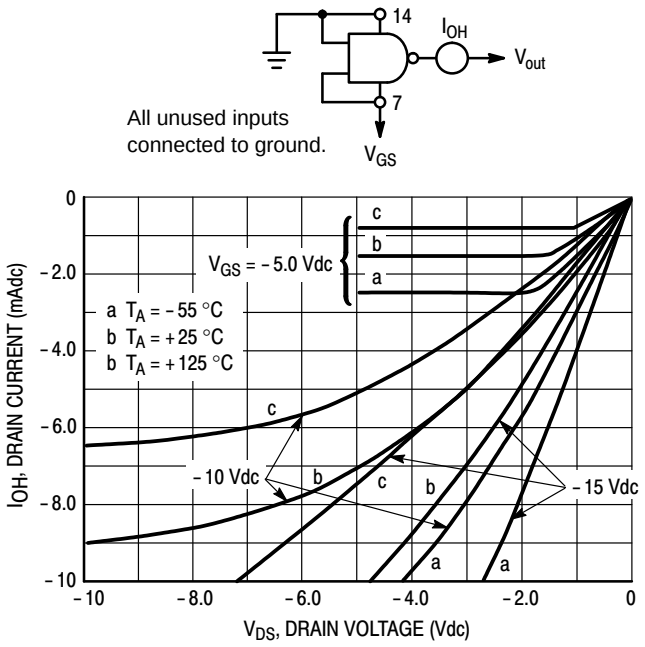



**Figure 3. Typical Output Source Characteristics Test Circuit**

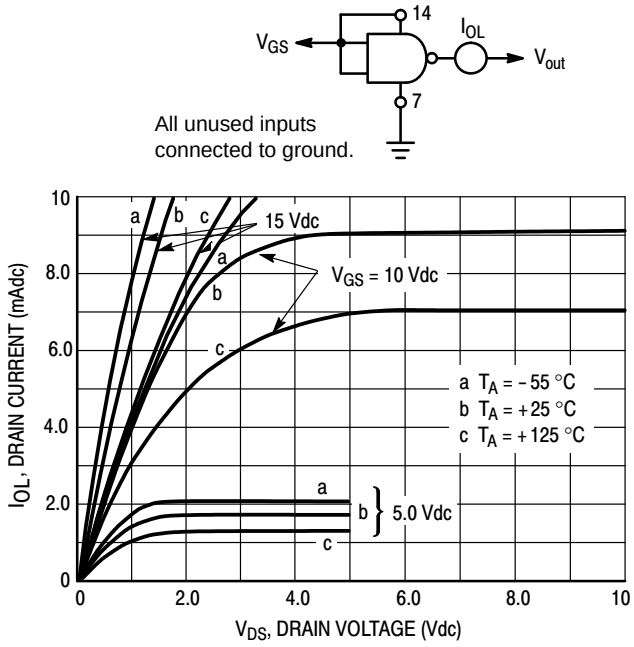



**Figure 4. Typical Output Sink Characteristics Test Circuit**

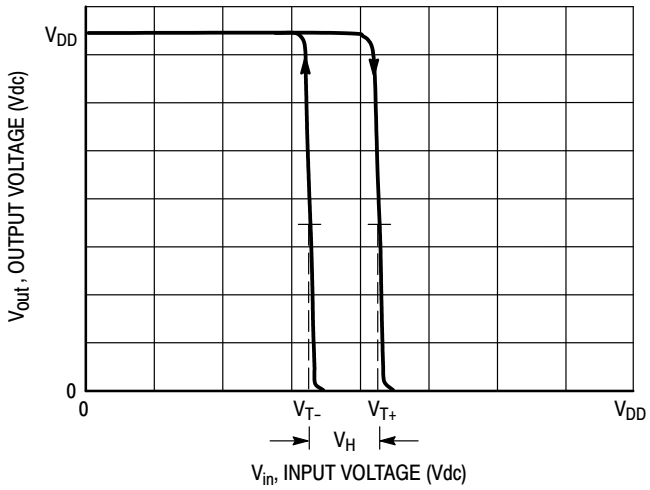



**Figure 5. Typical Transfer Characteristics**



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## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 11 | Rebranded the Data Sheet to **onsemi** format.<br>NLV14093BDG and MC14093BFELG OPNs Marked as Discontinued. | 8/27/2025 |

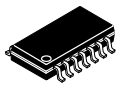
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



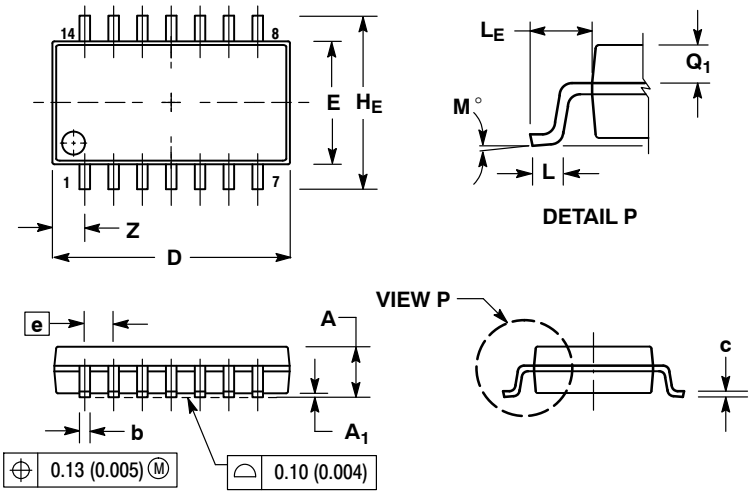
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**SOEIAJ−14**
CASE 965−01
ISSUE B

DATE 29 FEB 2008



**SCALE 1:1**



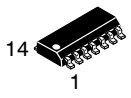

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.004 | 0.008 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |

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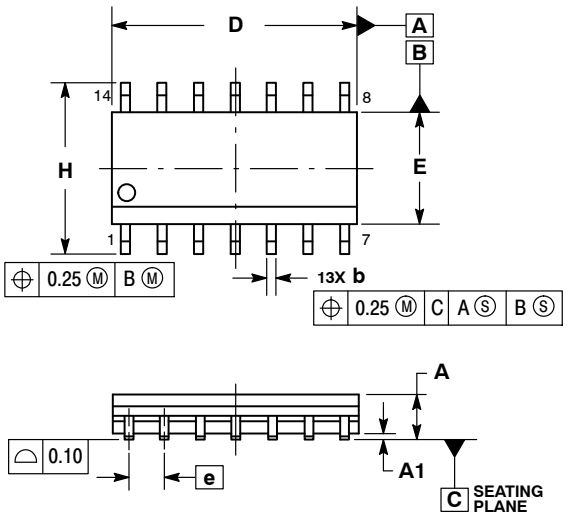
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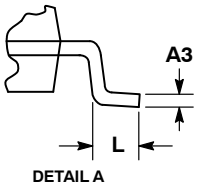


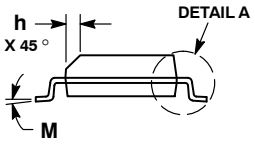

SCALE 1:1

**SOIC−14 NB**
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



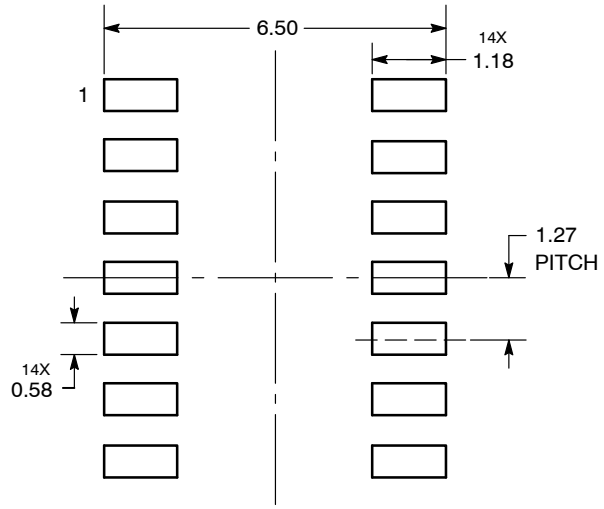




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |

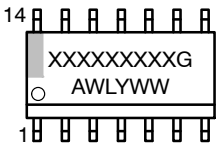
## SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

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| **DESCRIPTION:** | **SOIC−14 NB** | | **PAGE 1 OF 2** |

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**SOIC−14**
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

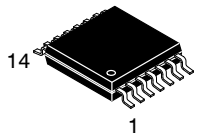
STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE




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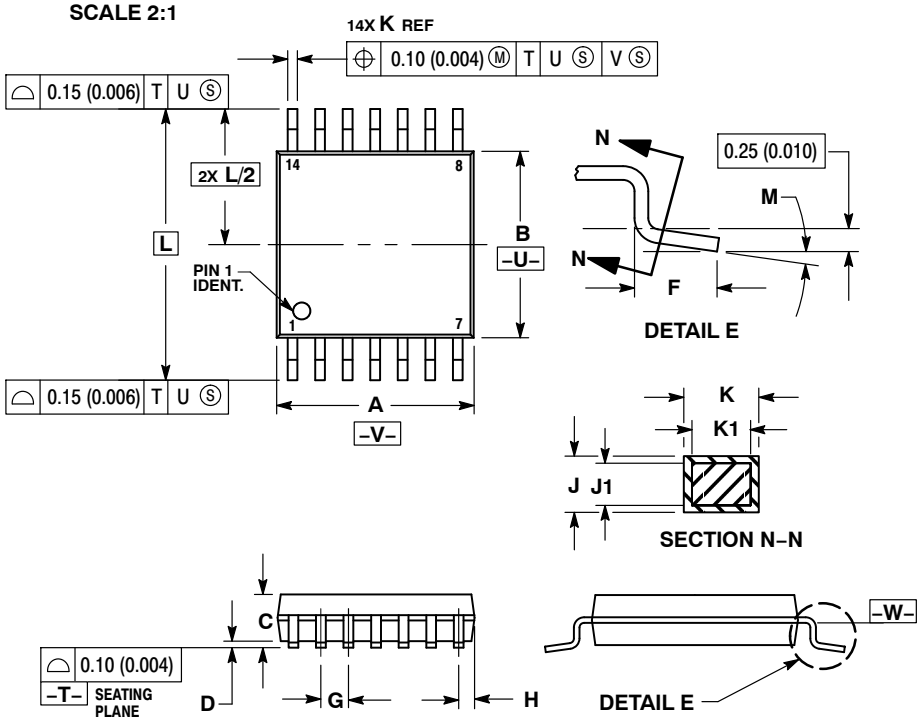
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SCALE 2:1

**TSSOP−14 WB**
CASE 948G
ISSUE C

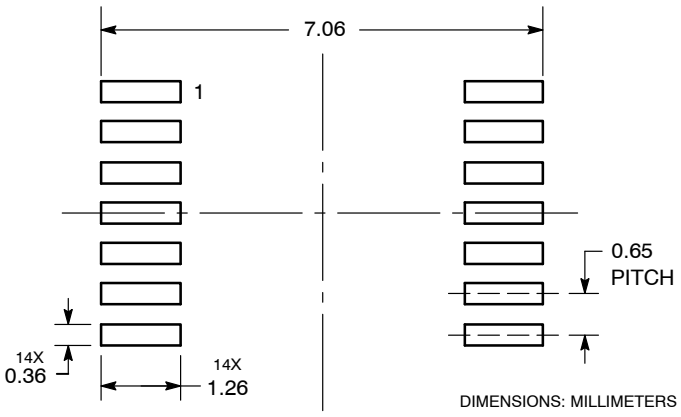
DATE 17 FEB 2016




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

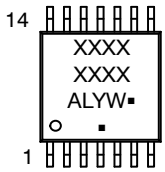
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

## RECOMMENDED SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TSSOP−14 WB** | **PAGE 1 OF 1** |

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