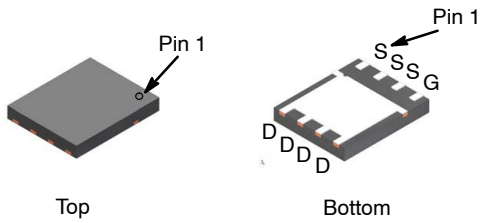
MOSFET – N-Channel, POWERTRENCH®

80 V, 130 A, 2.4 mΩ

FDMS86350



PQFN8 5X6, 1.27P
CASE 483AG

Description

This N−Channel MOSFET is produced using **onsemi** advanced POWERTRENCH® process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

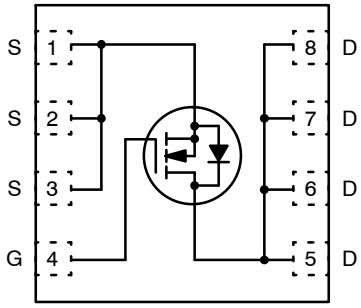
Features

- Max $R_{DS(on)}$ = 2.4 mΩ at V_{GS} = 10 V, I_D = 25 A
- Max $R_{DS(on)}$ = 3.2 mΩ at V_{GS} = 8 V, I_D = 22 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant
- These Device is Halogen Free

Applications

- Primary MOSFET
- Synchronous Rectifier
- Load Switch
- Motor Control Switch

ELECTRICAL CONNECTION



MARKING DIAGRAM



$Y	= Logo
&Z	= Assembly Location
&3	= Date Code (Year and Week)
&K	= Lot Run Traceability Code
FDMS	= Specific Device Code
86350	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous T_C = 25°C – Continuous T_A = 25°C (Note 1a) – Pulsed (Note 4)	 130 25 680	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	864	mJ
P_D	Power Dissipation, T_C = 25°C	156	W
	Power Dissipation, T_A = 25°C (Note 1a)	2.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

ELECTRICAL CHARACTERISTICS T_J = 25°C unless otherwise noted

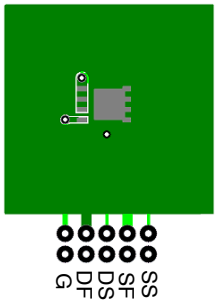
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		–	45	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V		–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.5	3.8	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		–	−12	–	mV/°C
$R_{DS(ON)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 25 A		–	2.0	2.4	mΩ
		V_{GS} = 8 V, I_D = 22 A		–	2.5	3.2	
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C		–	3.1	3.8	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 25 A		–	70	–	S
DYNAMIC CHARACTERISTICS							
C_{ISS}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		–	8030	10680	pF
C_{OOS}	Output Capacitance			–	1370	1825	pF
Crss	Reverse Transfer Capacitance			–	31	50	pF
R_g	Gate Resistance			0.1	1.1	3	Ω
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 40 V, I_D = 25 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	50	80	ns
t_r	Rise Time			–	34	55	ns
$t_{d(off)}$	Turn−Off Delay Time			–	40	65	ns
t_f	Fall Time			–	11	20	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	V_{DD} = 40 V, I_D = 25 A	–	110	155	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 8 V		–	90	127	nC
Qgs	Gate to Source Charge			–	46	–	nC
Qgd	Gate to Drain “Miller” Charge			–	23	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS							
I_S	Diode Continuous Forward Current	T_C = 25°C		–	–	130	A
$I_{S,\ pulse}$	Diode Pulse Current	T_C = 25°C		–	–	300	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		–	0.71	1.2	V
		V_{GS} = 0 V, I_S = 25 A (Note 2)		–	0.79	1.3	
t_{rr}	Reverse Recovery Time	I_F = 25 A, di/dt = 100 A/μs		–	63	101	ns
Q_{rr}	Reverse Recovery Charge			–	62	100	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

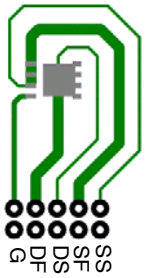
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NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 45°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 115°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 864 mJ is based on starting T_J = 25°C; L = 3 mH, I_{AS} = 24 A, V_{DD} = 80 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 74 A.
4. Pulse Id limited by junction temperature, td <= 100 μs, please refer to SOA curve for more details.

PACKAGE MARKING AND ORDERING INFOMRATION

ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping†
FDMS86350	FDMS86350	PQFN8 (Power 56) (Halogen Free)	13”	12 mm	3000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

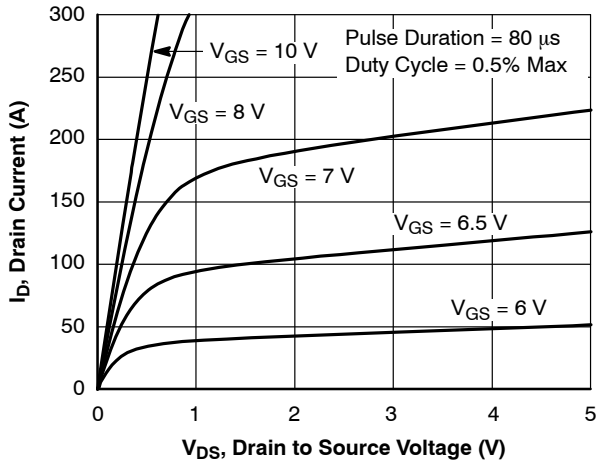


Figure 1. On−Region Characteristics

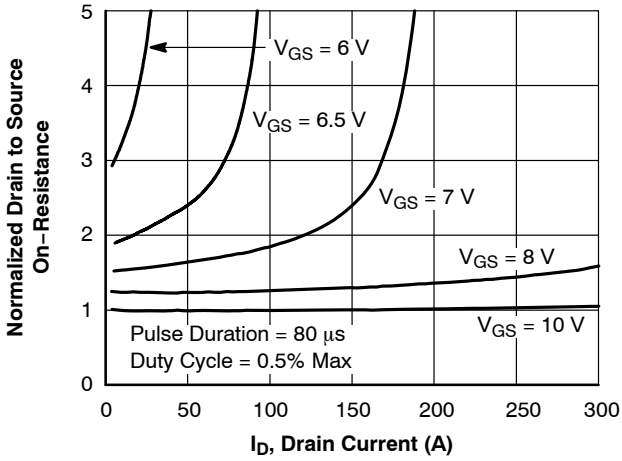


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

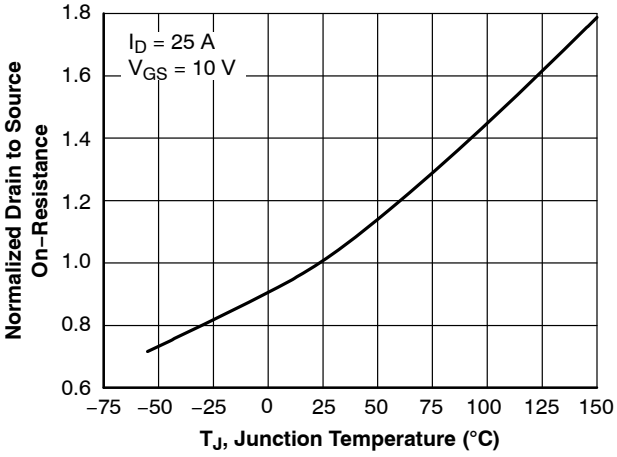


Figure 3. Normalized On−Resistance vs. Junction Temperature

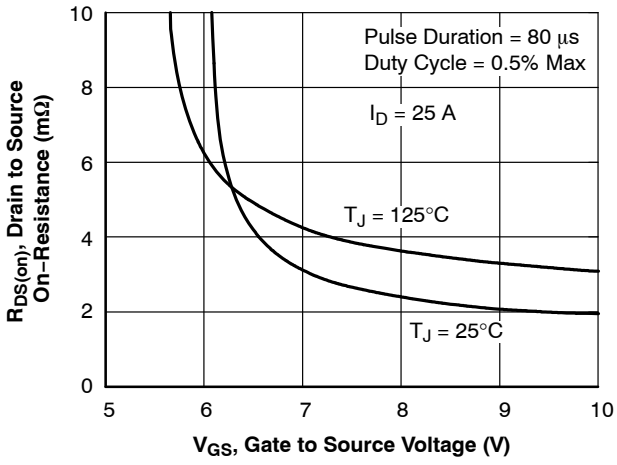


Figure 4. On−Resistance vs. Gate to Source Voltage

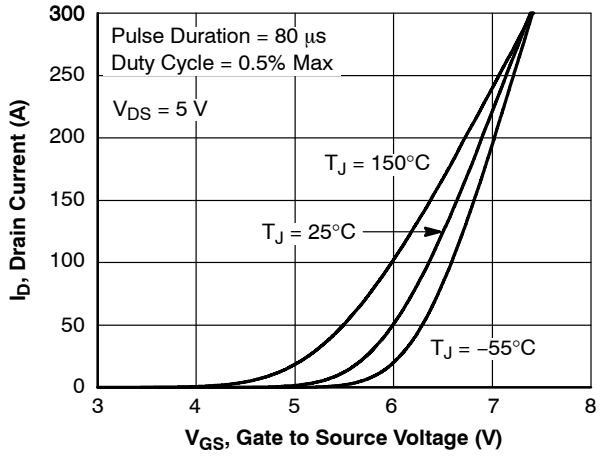


Figure 5. Transfer Characteristics

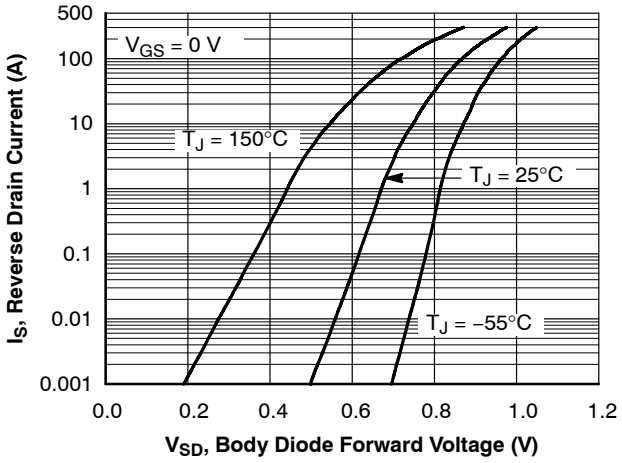


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

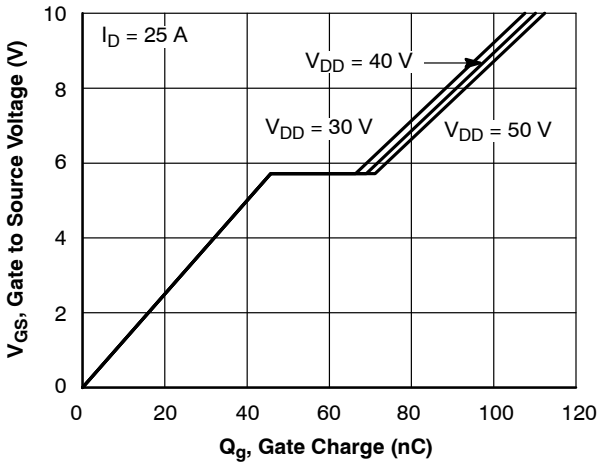


Figure 7. Gate Charge Characteristics

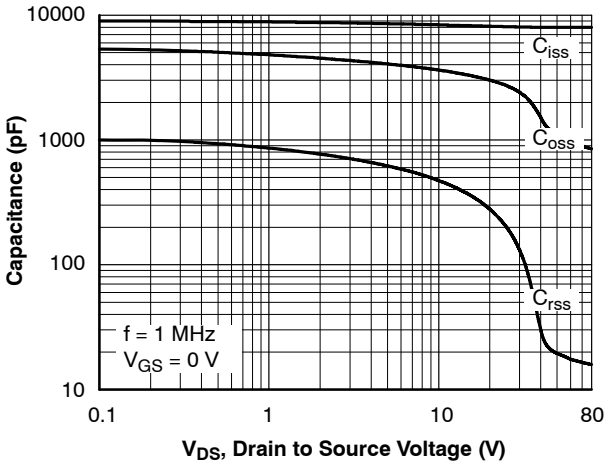


Figure 8. Capacitance vs. Drain to Source Voltage

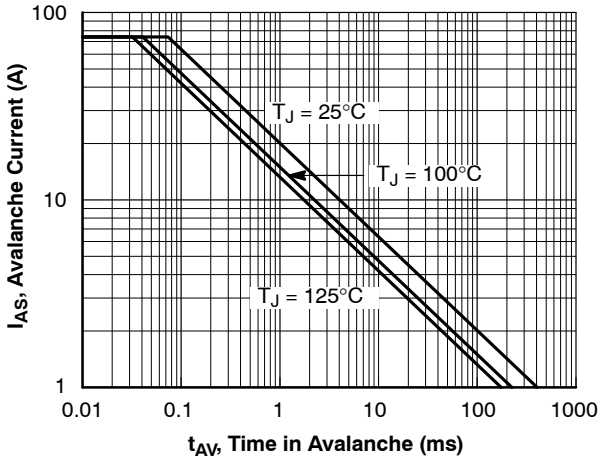


Figure 9. Unclamped Inductive Switching Capability

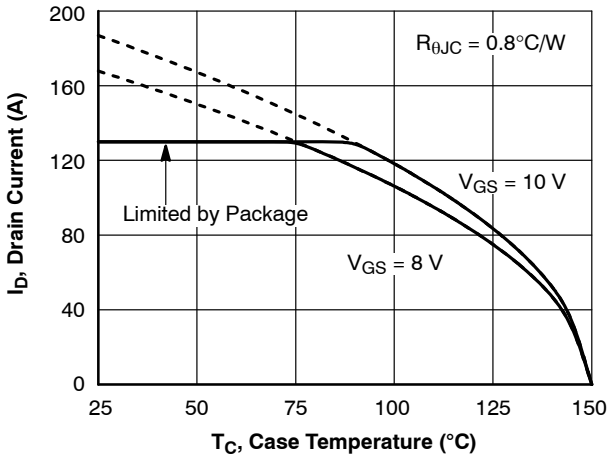


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

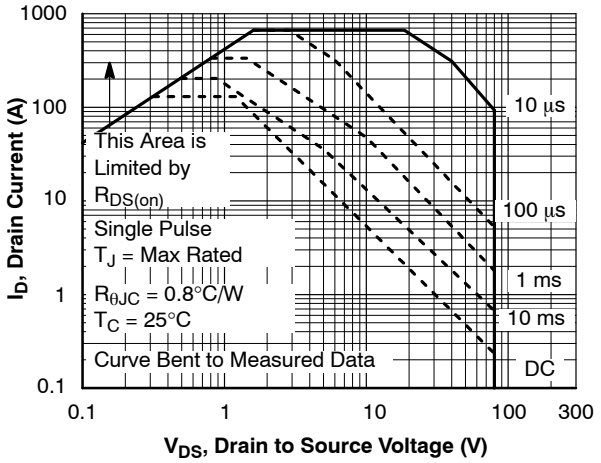


Figure 11. Forward Bias Safe Operating Area

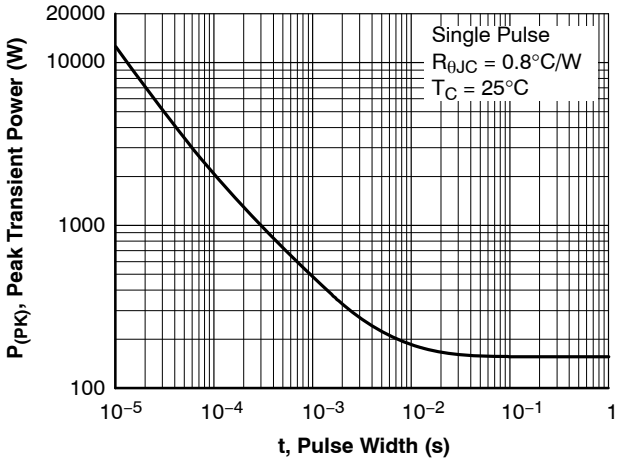


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

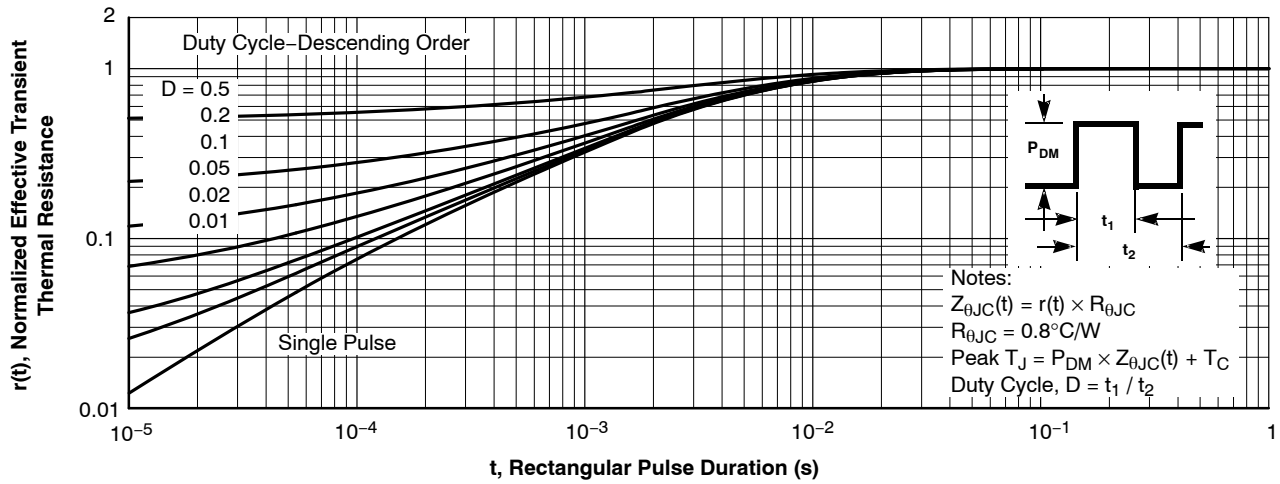
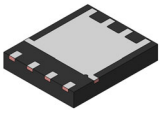


Figure 13. Junction−to−Case Transient Thermal Response Curve

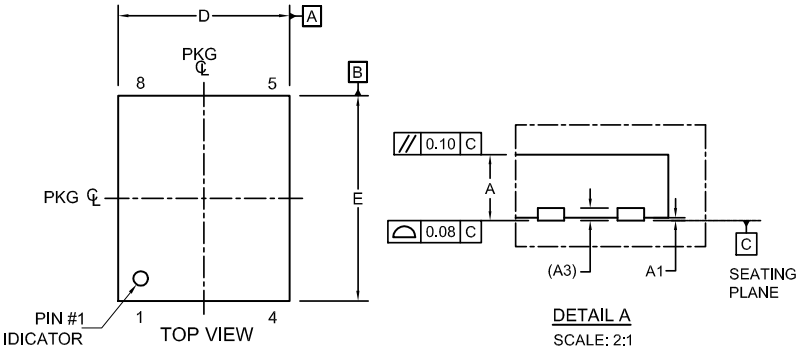
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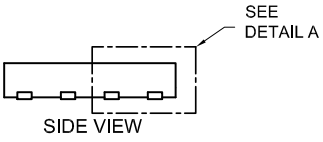
PQFN8 5X6, 1.27P
CASE 483AG
ISSUE A

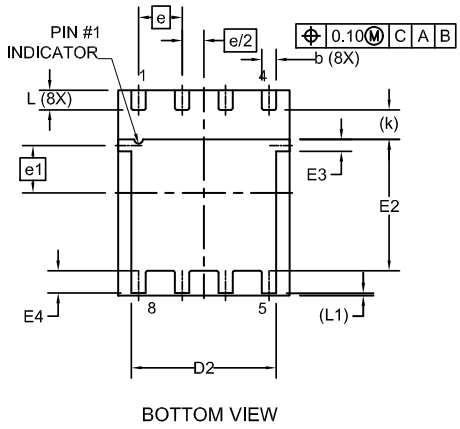
DATE 25 JUN 2021

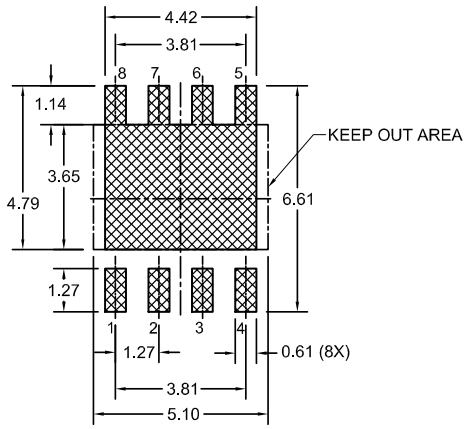


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.







LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3		0.20 REF	
b	0.37	0.42	0.47
D	4.90	5.00	5.10
D2	4.13	4.23	4.33
E	5.90	6.00	6.10
E2	3.74	3.84	3.94
E3	0.25	0.35	0.45
E4	0.60	0.70	0.80
e		1.27 BSC	
e/2		0.635 BSC	
e1		1.31 BSC	
k		0.86 REF	
L	0.47	0.57	0.67
L1		0.08REF	

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