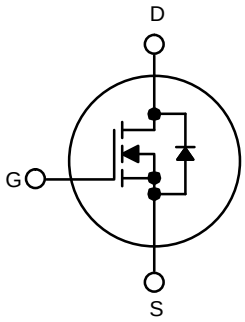
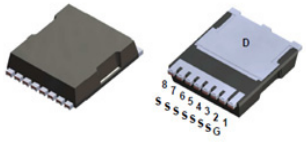
MOSFET – N-Channel, POWERTRENCH®

80 V, 220 A, 3.0 mΩ

FDBL86366-F085



N-Channel



H-PSOF8L
CASE 100CU

Features

- Typical $R_{DS(on)}$ = 2.4 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 86 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

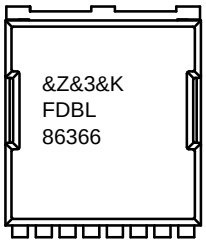
MOSFET MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current − Continuous (V_{GS} = 10), T_C = 25 °C (Note 1)	220	A
	Pulsed Drain Current, T_C = 25 °C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	205	mJ
P_D	Power Dissipation	300	W
	Derate Above 25 °C	2.0	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting T_J = 25 °C, L = 0.1 mH, I_{AS} = 64 A, V_{DD} = 80 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86366	= Specific Device Code

ORDERING INFORMATION

Device	Top Mark	Package	Shipping†
FDBL86366-F085	FDBL86366	H-PSOF8L	2000 Units/ Tape&Reel

* For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain-to-Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		80	–	–	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS} = 80 V, V_{GS} = 0 V	T_J = 25 °C	–	–	1	μA
			T_J = 175 °C (Note 4)	–	–	1	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source on Resistance	I_D = 80 A, V_{GS} = 10 V	T_J = 25 °C	–	2.4	3.0	mΩ
			T_J = 175 °C (Note 4)	–	4.9	6.1	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		–	6320	–	pF
C_{oss}	Output Capacitance			–	1030	–	pF
C_{rss}	Reverse Transfer Capacitance			–	32	–	pF
R_g	Gate Resistance	f = 1 MHz		–	2.1	–	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10 V	V_{GS} = 0 to 10 V	V_{DD} = 64 V, I_D = 80 A	–	86	112	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V		–	12	18	nC
Q_{gs}	Gate-to-Source Gate Charge	V_{DD} = 64 V, I_D = 80 A		–	30	–	nC
Q_{gd}	Gate-to-Drain “Miller” Charge			–	18	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn-On Time	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	–	98	ns
$t_{d(on)}$	Turn-On Delay			–	30	–	ns
t_r	Rise Time			–	34	–	ns
$t_{d(off)}$	Turn-Off Delay			–	40	–	ns
t_f	Fall Time			–	17	–	ns
t_{off}	Turn-Off Time			–	–	86	ns
DRAIN-SOURCE DIODE CHARACTERISTIC							
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} = 80 A, V_{GS} = 0 V		–	–	1.25	V
		I_{SD} = 40 A, V_{GS} = 0 V		–	–	1.2	V
t_{rr}	Reverse-Recovery Time	I_F = 80 A, dI_{SD}/dt = 100 A/μs, V_{DD} = 64 V		–	80	120	ns
Q_{rr}	Reverse-Recovery Charge			–	95	140	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175 °C. Product is not tested to this condition in production.

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TYPICAL CHARACTERISTICS

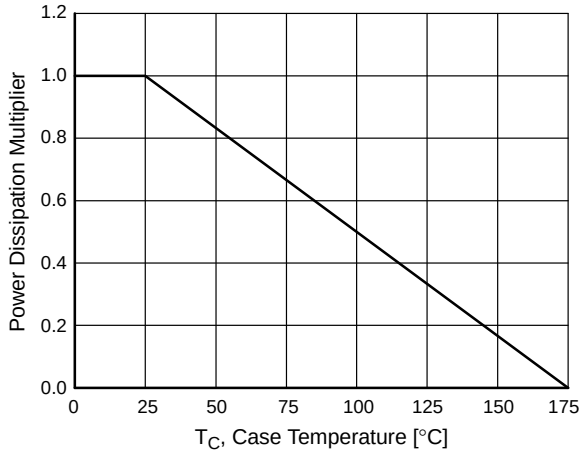


Figure 1. Normalized Power Dissipation vs. Case Temperature

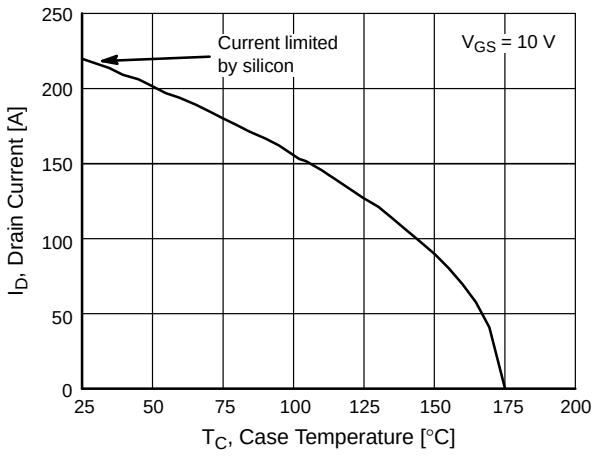


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

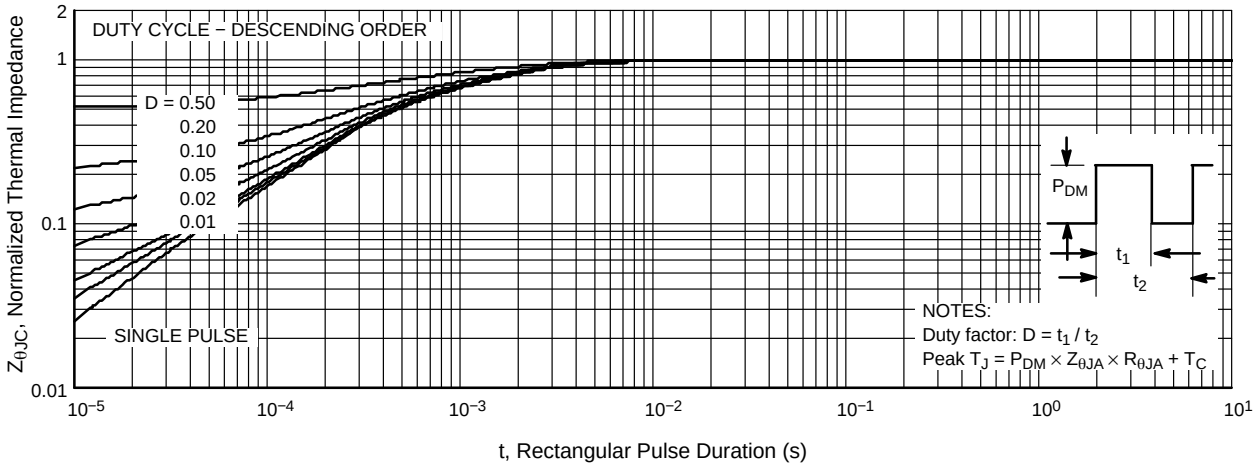


Figure 3. Normalized Maximum Transient Thermal Impedance

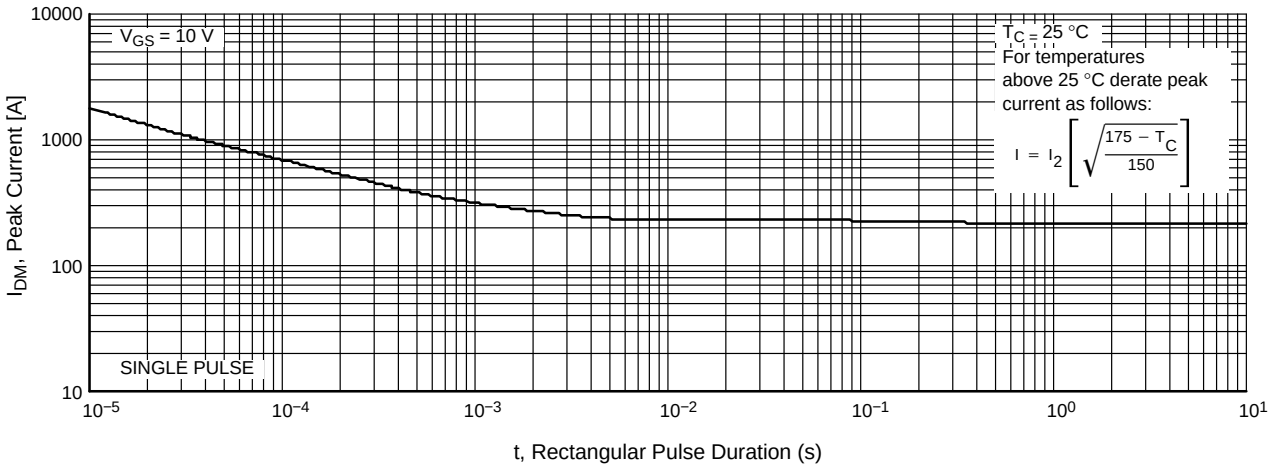


Figure 4. Peak Current Capability

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TYPICAL CHARACTERISTICS (CONTINUED)

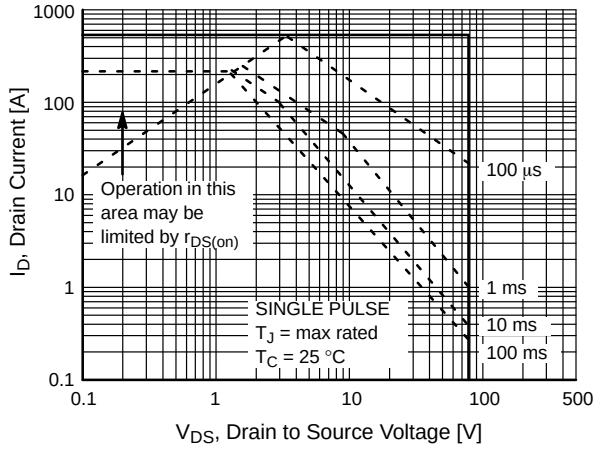
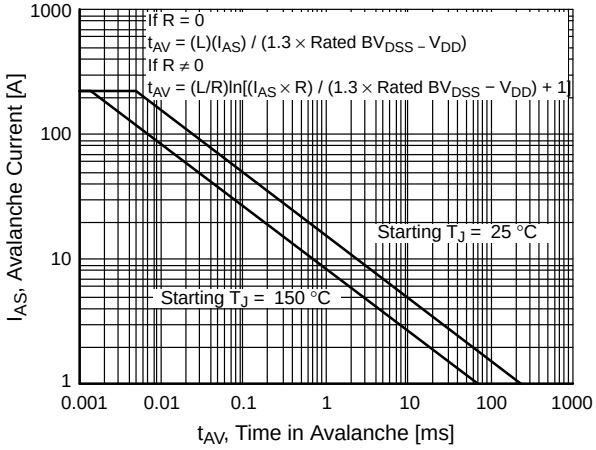


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to **onsemi** Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

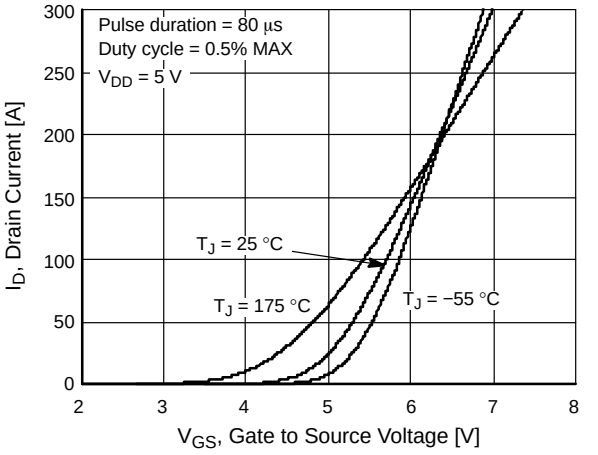


Figure 7. Transfer Characteristics

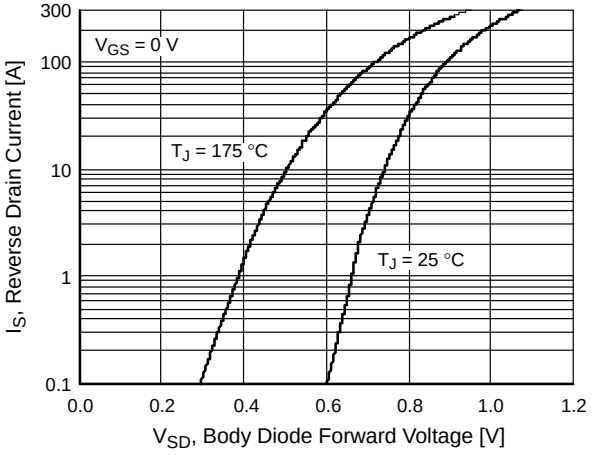


Figure 8. Forward Diode Characteristics

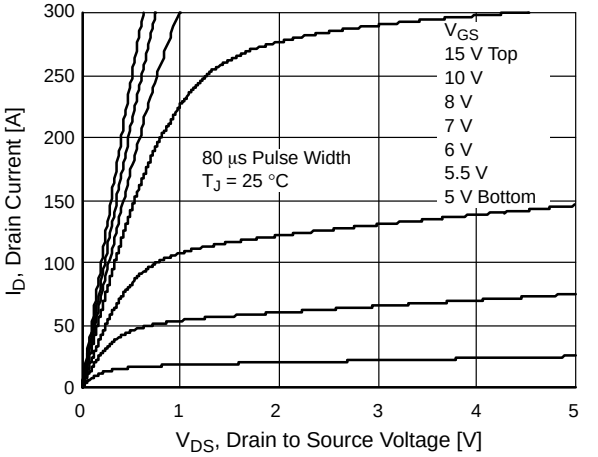


Figure 9. Saturation Characteristics

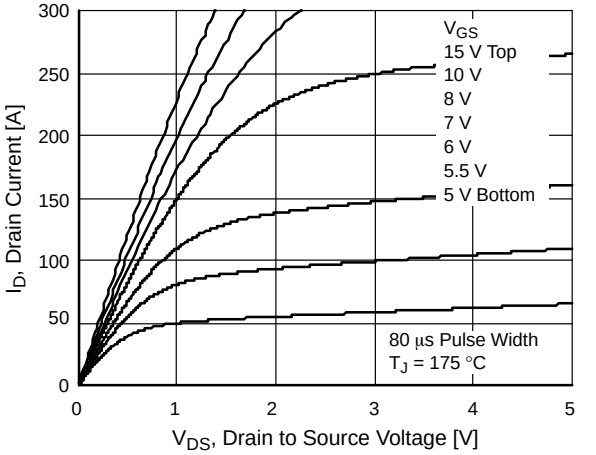


Figure 10. Saturation Characteristics

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TYPICAL CHARACTERISTICS (CONTINUED)

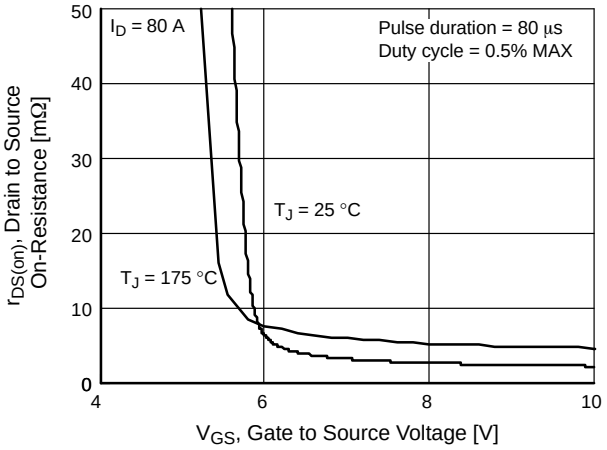


Figure 11. R_{DSON} vs. Gate Voltage

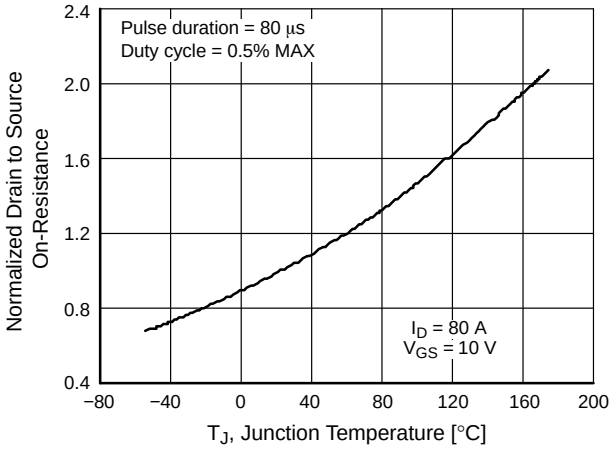


Figure 12. Normalized R_{DSON} vs. Junction Temperature

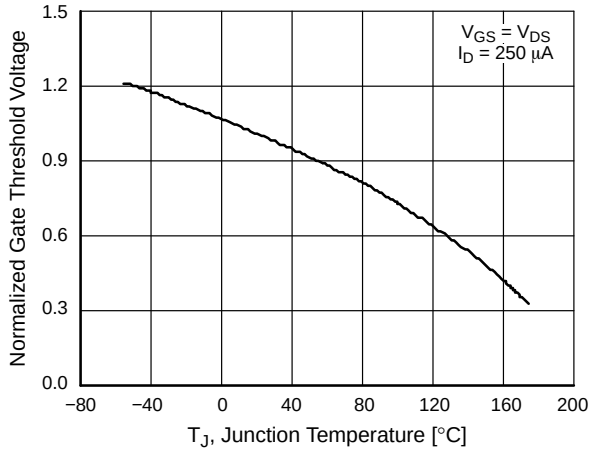


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

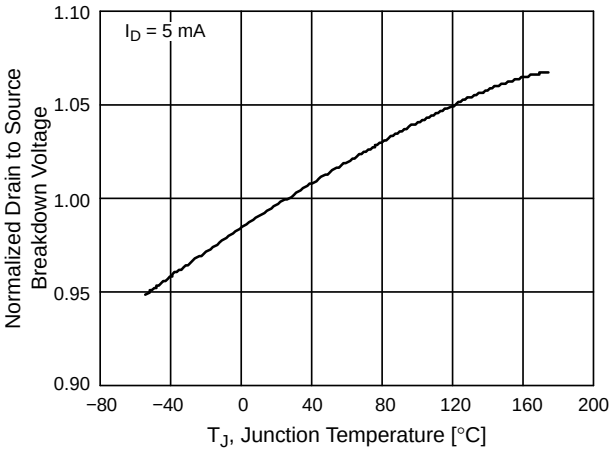


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

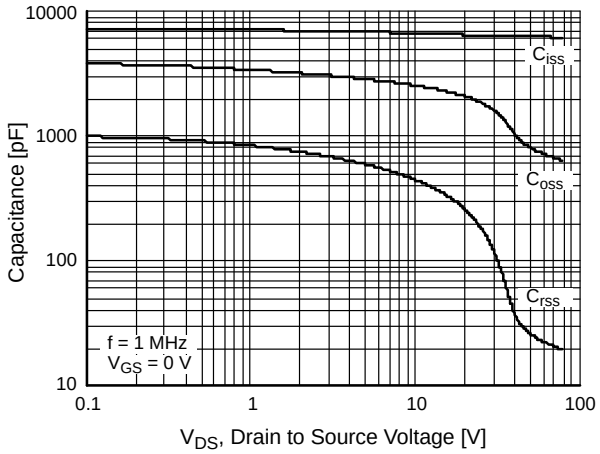


Figure 15. Capacitance vs. Drain to Source Voltage

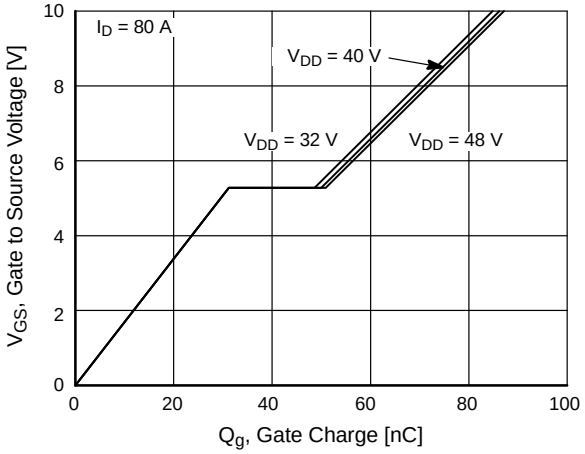


Figure 16. Gate Charge vs. Gate to Source Voltage

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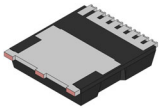
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REVISION HISTORY

Revision	Description of Changes	Date
4	Rebranded the document to **onsemi** format.	3/27/2026

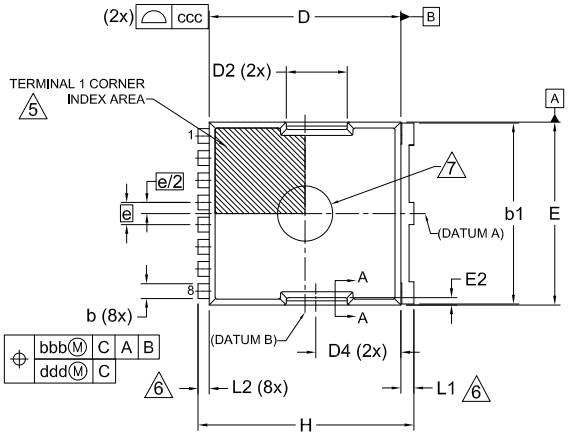
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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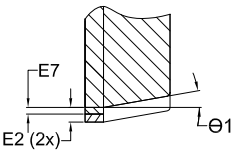


H−PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

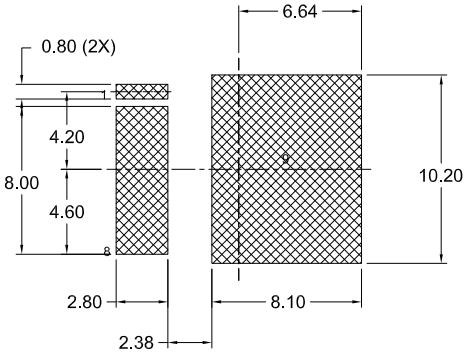
DATE 30 JUL 2024



TOP VIEW

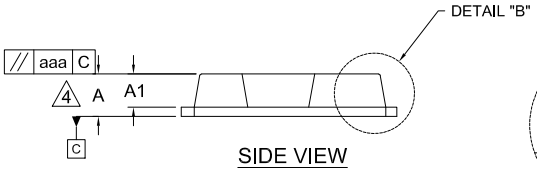


SECTION "A-A"
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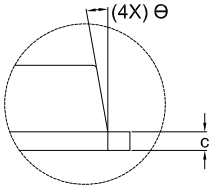


LAND PATTERN RECOMMENDATION

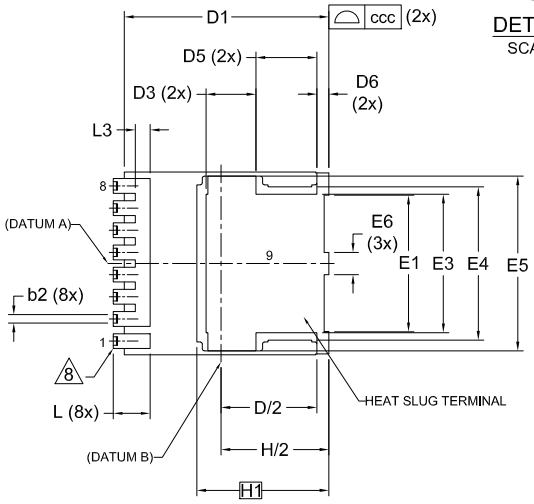
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SIDE VIEW



DETAIL "B"
SCALE: 2X



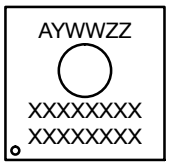
BOTTOM VIEW

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g.,EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**H−PSOF8L 11.68x9.80x2.30, 1.20P**	**PAGE 1 OF 1**

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