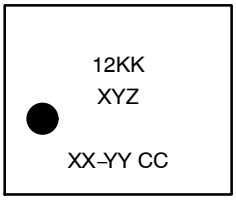
5 A, 2.4 MHz, Digitally Programmable TinyBuck Regulator

FAN53555



WLCSP20
CASE 567QK, 567SH, 567SK

MARKING DIAGRAM



Line 1:
12 = Device Marking Code
(See Ordering Information for specific device code)
KK = Lot Run Code

Line 2:
XY = Date Code
Z = Assembly Plant Code

Line 3: **onsemi** internal use only

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

Description

The FAN53555 is a step−down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5 V to 5.5 V. The output voltage is programmed through an I^2C interface capable of operating up to 3.4 MHz.

Using a proprietary architecture with synchronous rectification, the FAN53555 is capable of delivering 5 A continuous at over 80% efficiency, while maintaining over 80% efficiency at load currents as low as 10 mA. Pulse currents as high as 6.5 A can be supported by the 05 option. The regulator operates at a nominal fixed frequency of 2.4 MHz, which reduces the value of the external components to 330 nH for the output induction and as low as 20 μF for the output capacitor. Additional output capacitance can be added to improve regulation during load transients without affecting stability. Inductance up to 1.2 μH may be used with additional output capacitance.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in Power−Save Mode with a typical quiescent current of 60 μA. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed−frequency control, operating at 2.4 MHz. In Shutdown Mode, the supply current drops below 1 μA, reducing power consumption. PFM Mode can be disabled if constant frequency is desired. The FAN53555 is available in a 20−bump, 1.6 × 2 mm, WLCSP.

Features

- Fixed−Frequency Operation: 2.4 MHz
- Best−in−Class Load Transient
- Continuous Output Current Capability: 5 A
- Pulse Current Capability: 6.5 A (05 Option)
- 2.5 V to 5.5 V Input Voltage Range
- Digitally Programmable Output Voltage:
  - 00/01/03/05/08/18 Options: 0.6−1.23 V in 10 mV Steps
  - 04/042/09/ Options: 0.603−1.411 V in 12.826 mV Steps
  - 23, 79 Option: 0.60−1.3875 V in 12.5 mV Steps
  - 24 Option: 0.603−1.420 V in 12.967 mV Steps
  - 13 Option: 0.8−1.43 V in 10 mV Steps
- Programmable Slew Rate for Voltage Transitions
- I^2C−Compatible Interface Up to 3.4 Mbps
- PFM Mode for High Efficiency in Light Load
- Quiescent Current in PFM Mode: 60 μA (Typical)

Features (continued)

- Internal Soft−Start
- Input Under−Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 20−Bump Wafer−Level Chip Scale Package (WLCSP)

Applications

- Application, Graphic, and DSP Processors Arm®, Krait, OMAP™, NovaThor™, ARMADA
- Hard Disk Drives
- Tablets, Netbooks, Ultra−Mobile Pcs
- Smart Phones
- Gaming Devices

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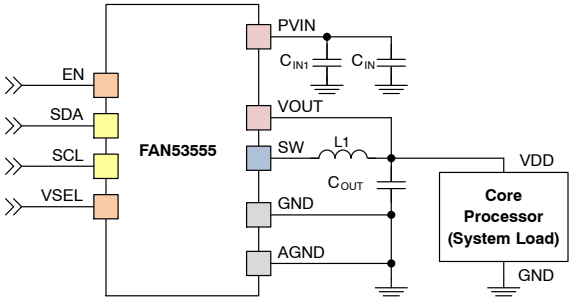


Figure 1. Typical Application

Table 1. ORDERING INFORMATION

Part Number	Device Code	Power−Up Defaults		I^2C Slave Address	A1 PIN Function	Max. RMS Current	Programmable Output Voltage	EN Pin Low
		VSEL0	VSEL1					
FAN53555UC04X	BP	1.10	1.20	C0	VSEL	5 A	0.603−1.411 V in 12.826 mV	Registers reset
DISCONTINUED (Note 4)								
FAN53555UC00X	BK	1.05	1.20	C0	VSEL	5 A	0.6−1.23 V in 10 mV	Registers not reset
FAN53555UC01X	BL	0.90	OFF		VSEL	5 A		
FAN53555UC03X	BN	0.90	N/A		PGOOD	5 A		
FAN53555UC05X	BU	0.90	OFF		VSEL	5 A		
FAN53555BUC05X (Note 1)	BU	0.90	OFF		VSEL	5 A		
FAN53555UC08X	BW	1.02	1.15		VSEL	4 A		
FAN53555BUC08X (Note 1)	BJ	1.02	1.15		VSEL	4 A		
FAN53555BUC09X (Note 1)	CP	1.10	1.10		VSEL	3 A	0.603−1.411 V in 12.826 mV	
FAN53555UC09X	CP	1.10	1.10		VSEL	3 A		
FAN53555UC13X	CT	1.15	1.15		VSEL	5 A	0.8−1.43 V in 10 mV	
FAN53555BUC13X (Note 1)	CT	1.15	1.15		VSEL	5 A		
FAN53555UC18X	CU	1.02	1.15		VSEL	5 A	0.6−1.23 V in 10 mV	
FAN53555BUC18X (Note 1)	CU	1.02	1.15		VSEL	5 A		
FAN53555BUC79X	FU	0.85	N/A		PGOOD	5 A		Registers reset
FAN53555BUC23X (Note 1)	CW	1.15	1.15		VSEL	5 A	0.6−1.3875 V in 12.5 mV	Registers not reset
FAN53555UC24X	CR	1.225	1.212		VSEL	4 A	0.603−1.42 V in 12.967 mV	Registers reset
FAN53555BUC24X (Note 1)	CR	1.225	1.212		VSEL	4 A		
FAN53555UC042X (Note 2)	BX	1.10	1.20	C4	VSEL	5 A	0.603−1.411 V in 12.826 mV	

1. The FAN53555BUC05X, FAN53555BUC08X, FAN53555BUC09X, FAN53555BUC13X, FAN53555BUC18X, FAN53555BUC23X, and FAN53555BUC24X, include backside lamination.
2. The 042 option is the same as the 04 option, except the I^2C slave addresses.
3. Temperature Range −40 to 85 °C, Package WLCSP−20, Packing Method Tape & Reel
4. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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RECOMMENDED EXTERNAL COMPONENTS

Table 2. RECOMMENDED EXTERNAL COMPONENTS FOR 5 A MAXIMUM LOAD CURRENT

Component	Description	Vendor	Parameter	Typ.	Unit
L1	330 nH Nominal	*See Table 3*	L	0.33	μH
			DCR	13	mΩ
C_{OUT}	2 Pieces; 22 μF, 6.3 V, X5R, 0805	GRM21BR60J226M (Murata) C2012X5R0J226M (TDK)	C	44	μF
C_{IN}	1 Piece; 10 μF, 10 V, X5R, 0805	LMK212BJ106KG−T (Taiyo Yuden) C2012X5R1A106M (TDK)	C	10	
	2 Pieces; 10 μF, 6.3 V, X5R, 0805	GRM21BR60J106M (Murata) C2012X5R0J106M (TDK)	C	20	
C_{IN1}	10 nF, 25 V, X7R, 0402	GRM155R71E103K (Murata) C1005X7R1E103K (TDK)	C	10	nF

Table 3. RECOMMENDED INDUCTORS FOR HIGH−CURRENT APPLICATIONS

Manufacturer	Part#	L (nH)	DCR (mΩ)	I_{MAXDC} (Note 5)	Component Dimensions		
					L	W	H
Vishay	IHLP1616ABERR47M01	470	20.0	5.0	4.5	4.1	1.2
Mag. Layers (Note 6)	MMD−04ABNR33M−M1−RU	330	12.5	7.5	4.5	4.1	1.2
Mag. Layers	MMD−04ABNR47M−M1−RU	470	20.0	5.0	4.5	4.1	1.2
Inter−Technical	SM1608−R33M	330	9.6	9.0	4.5	4.1	2.0
Bournes	SRP4012−R33M	330	15.0	6.7	4.7	4.2	1.2
Bournes	SRP4012−R47M	470	20.0	5.0	4.7	4.2	1.2
TDK	VLC5020T−R47M	470	15.0	5.4	5.0	5.0	2.0

5. I_{MAXDC} is the lesser current to produce 40°C temperature rise or 30% inductance roll−off.
6. Preferred inductor value is 330 nH and all dynamic characterization was performed with this coil.

FAN53555−24, −08, and −09 REDUCED OUTPUT CURRENT (4 A Max. RMS. for 08, and 24, 3 A Max. RMS for 09) SMALLER FOOTPRINT APPLICATION

The FAN53555−24, −08, and −09 were developed to provide power for core processors with high−performance graphics acceleration in Li−Ion−powered handheld devices. These applications require a very compact solution. The smaller input and output capacitors in the table below assume that additional bypass capacitance exists across the battery in fairly close proximity to the regulator(s). The C_{IN} capacitors specified below are the capacitors that are required in very close proximity to VIN and PGND *(see layout recommendations in Figure 2 below)*.

Table 4. RECOMMENDED EXTERNAL COMPONENTS FOR LOWER−CURRENT APPLICATIONS WITH FAN53555−08−09−24

Component	Description	Vendor	Parameter	Typ	Unit
L1	470 or 330 nH, 2016 case size	See Table 5			
C_{OUT}	−08, ,24 Option 2 Pieces 22 μF, 6.3 V, X5R, 0603	C1608X5R0J226M (TDK)	C	44	μF
	−09 Option 1 Piece 22 μF, 6.3 V, X5R, 0603			22	
C_{IN}	1 Piece; 10 μF, 10 V, X5R, 0402	GRM155R61A106M (Murata)	C	10	
C_{IN1}	10 nF, 25 V, X5R, 0201	TMK063CG100DT−F (Taiyo Yuden)	C	10	nF

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Table 5. RECOMMENDED INDUCTORS FOR LOWER−CURRENT APPLICATIONS WITH FAN53555−08−09−24

Manufacturer	Part#	L (nH)	DCR (mΩ Typ.)	I_{MAXDC} (Note 7)	Component Dimensions		
					L	W	H
Toko	DFE201612R-H−R33N	330	25	3.2	2.0	1.6	1.2
Toko	DFE201612C−R47N	470	40	3.2	2.0	1.6	1.2
Cyntek	PIFE20161B−R47MS−39	470	30	3.1	2.0	1.6	1.2
SEMCO	CIGT201610HMR47SCE	470	30	3.1	2.0	1.6	0.9

7. I_{MAXDC} is the lesser current to produce 40°C temperature rise or 30% inductance roll−off.

Layout

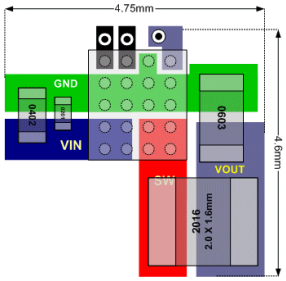


Figure 2. Reduced−Footprint Layout

Pin Configuration

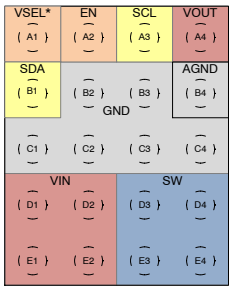
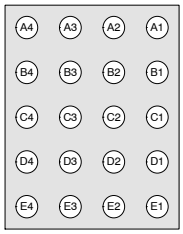


Figure 3. Top View



A1 = VSEL for 00, 01, 04, 05, 08, 09, 13, 18, 23, 24
A1 = PGOOD for 03,79

Figure 4. Bottom View

Table 6. PIN DEFINITIONS

Pin #	Name	Description
A1	VSEL (Except −03 Option)	Voltage Select. When this pin is LOW, V_{OUT} is set by the VSEL0 register. When this pin is HIGH, V_{OUT} is set by the VSEL1 register.
	PGOOD (03)	Power Good. This open−drain pin pulls LOW if an overload condition occurs or soft−start is in progress.
A2	EN	Enable. The device is in Shutdown Mode when this pin is LOW. All register values are kept during shut-down. Options 00, 01, 03, 05, 08 09, 13, 18, and 23 do not reset register values when EN is raised. The 04, 24, 79, and 042 options reset all registers to default values when EN pin is LOW. If pulled up to a low−im-pedance voltage source greater than 1.8 V, use at least 100 Ω series resistor.
A3	SCL	I^2C Serial Clock
A4	VOUT	VOUT. Sense pin for VOUT. Connect to COUT.
B1	SDA	I^2C Serial Data
B2, B3, C1 − C4	GND	Ground. Low−side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
B4	AGND	Analog Ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.

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Table 6. PIN DEFINITIONS (continued)

Pin #	Name	Description
D1, D2, E1, E2	VIN	Power Input Voltage. Connect to the input power source. Connect to C_{IN} with minimal path.
D3, D4, E3, E4	SW	Switching Node. Connect to the inductor.

Table 7. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{IN}	Voltage on SW, VIN Pins	IC Not Switching	−0.3	7.0	V
		IC Switching	−0.3	6.5	
	Voltage on EN Pin	Tied without Series Resistance	−0.3	2.0	V
		Tied through Series Resistance of at Least 100 Ω	−0.3	V_{IN} (Note 8)	
	Voltage on All Other Pins	IC Not Switching	−0.3	V_{IN} (Note 8)	V
V_{OUT}	Voltage on VOUT Pin		−0.3	3.0	V
V_{INOV_SLEW}	Maximum Slew Rate of V_{IN} > 6.5 V, PWM Switching			100	V/ms
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22−A114	2000		V
		Charged Device Model per JESD22−C101	1500		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

8. Lesser of 7 V or V_{IN} + 0.3 V.

Table 8. RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. **onsemi** does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Supply Voltage Range	2.5		5.5	V
I_{OUT}	Output Current	0		5	A
L	Inductor		0.33		μH
C_{IN}	Input Capacitor		10		μF
C_{OUT}	Output Capacitor		44		μF
T_A	Operating Ambient Temperature	−40		+85	°C
T_J	Operating Junction Temperature	−40		+125	°C

Table 9. THERMAL PROPERTIES

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance (Note 9)		38		°C/W

9. See Thermal Considerations in the Application Information section.

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Table 10. ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_{IN} = 2.5 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 5 V, and EN = HIGH.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
POWER SUPPLIES						
I_Q	Quiescent Current	I_{LOAD} = 0		60	100	μA
		I_{LOAD} = 0, MODE Bit = 1 (Forced PWM)		43		mA
I_{SD}	H/W Shutdown Supply Current	EN = GND		0.1	5.0	μA
	S/W Shutdown Supply Current	EN = V_{IN}, BUCK_ENx = 0		41	75	μA
V_{UVLO}	Under−Voltage Lockout Threshold	V_{IN} Rising		2.35	2.45	V
V_{UVHYST}	Under−Voltage Lockout Hysteresis			350		mV
EN, VSEL, SDA, SCL						
V_{IH}	High−Level Input Voltage		1.1			V
V_{IL}	Low−Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			160		mV
I_{IN}	Input Bias Current	Input Tied to GND or VIN		0.01	1.00	μA
PGOOD (03, 79 OPTION)						
I_{OUTL}	PGOOD Pull−Down Current				1	mA
I_{OUTH}	PGOOD HIGH Leakage Current			0.01	1.00	μA
V_{OUT} REGULATION						
V_{REG}	V_{OUT} DC Accuracy	$I_{OUT(DC)}$ = 0, Forced PWM, V_{OUT} = VSEL0 Default Value	−1.5		1.5	%
		08, 24 Options: 2.5 V ≤ V_{IN} ≤ 4.5 V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 4 A, Auto PFM/PWM	−2.0		4.0	%
		09 Option: 2.5 V ≤ V_{IN} ≤ 4.5 V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3 A, Auto PFM/PWM	−2.0		4.0	%
		13, 18, 23 Options: 2.5 V ≤ V_{IN} ≤ 4.5 V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 5 A, Auto PFM/PWM	−2.0		4.0	%
		All Other Options: 2.5 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 5 A, Auto PFM/PWM	−3.0		5.0	%
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation	$I_{OUT(DC)}$ = 1 to 5 A		−0.1		%/A
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	2.5 V ≤ V_{IN} ≤ 5.5 V, $I_{OUT(DC)}$ = 1.5 A		0.01		%/V
V_{TRSP}	Transient Response	I_{LOAD} Step 0.1 A to 1.5 A, t_r = t_f = 100 ns, V_{OUT} = 1.2 V		±40		mV
POWER SWITCH AND PROTECTION						
$R_{DS(on)P}$	P−Channel MOSFET On Resistance	V_{IN} = 5 V		28		mΩ
$R_{DS(on)N}$	N−Channel MOSFET On Resistance	V_{IN} = 5 V		17		mΩ

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Table 10. ELECTRICAL CHARACTERISTICS (continued)
Minimum and maximum values are at V_{IN} = 2.5 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 5 V, and EN = HIGH.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
POWER SWITCH AND PROTECTION						
I_{LIMPK}	P−MOS Peak Current Limit	00, 01, 03, 04, 13, 18, 23, 042, 79 Options	6.3	7.4	8.5	A
		05 Option	8.5	10.0	11.5	A
		08, 24 Options	5.0	5.9	6.8	A
		09 Option	4.0	4.75	5.5	
T_{LIMIT}	Thermal Shutdown			150		°C
T_{HYST}	Thermal Shutdown Hysteresis			17		°C
V_{SDWN}	Input OVP Shutdown	Rising Threshold		6.15		V
		Falling Threshold	5.50	5.85		V
FREQUENCY CONTROL						
f_{SW}	Oscillator Frequency		2.05	2.40	2.75	MHz
DAC						
	Resolution			6		Bits
	Differential Nonlinearity (Note 10)				0.5	LSB
TIMING						
I^2C_{EN}	EN = HIGH to I²C Start		100			µs
SOFT−START						
t_{SS}	Regulator Enable to Regulated V_{OUT}	R_{LOAD} > 5 Ω; to V_{OUT} = 1.2 V; 00, 01, 03, 04, 042, 05, 09, 13, 23 and 79 Options		300		µS
		2.5 V ≤ V_{IN} ≤ 4.5 V; R_{LOAD} = 2 Ω; to V_{OUT} = 1.127 V with 1.1 V Pre−Bias Voltage; 08 and 18 Options		135	175	µS
R_{OFF}	VOUT Pull−Down Resistance, Disabled	EN = 0 or V_{IN} < V_{UVLO}		160		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
10. Monotonicity assured by design.

Table 11. I²C TIMING SPECIFICATIONS
Guaranteed by design.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		Fast Mode Plus			1000	
		High−Speed Mode, C_B ≤100 pF			3400	
		High−Speed Mode, C_B ≤ 400 pF			1700	
t_{BUF}	Bus−Free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
		Fast Mode Plus		0.5		
$t_{HD;STA}$	START or REPEATED START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode		160		ns

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Table 11. I²C TIMING SPECIFICATIONS (continued)
Guaranteed by design.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{LOW}	SCL LOW Period	Standard Mode		4.7		μs
		Fast Mode		1.3		μs
		Fast Mode Plus		0.5		μs
		High−Speed Mode, $C_B \le 100$ pF		160.0		ns
		High−Speed Mode, $C_B \le 400$ pF		320.0		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode, $C_B \le 100$ pF		60		ns
		High−Speed Mode, $C_B \le 400$ pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		μs
		Fast Mode		600.0		ns
		Fast Mode Plus		260.0		ns
		High−Speed Mode		160.0		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		Fast Mode Plus		50		
		High−Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	μs
		Fast Mode	0		900.00	ns
		Fast Mode Plus	0		450.00	ns
		High−Speed Mode, $C_B \le 100$ pF	0		70.00	ns
		High−Speed Mode, $C_B \le 400$ pF	0		150.00	ns
t_{RCL}	SCL Rise Time	Standard Mode		$20+0.1C_B$	1000	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High−Speed Mode, $C_B \le 100$ pF		10	80	
		High−Speed Mode, $C_B \le 400$ pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High−Speed Mode, $C_B \le 100$ pF		10	40	
		High−Speed Mode, $C_B \le 400$ pF		20	80	
t_{RCL1}	Rise Time of SCL After a REPEATED START Condition and After ACK Bit	High−Speed Mode, $C_B \le 100$ pF		10	80	ns
		High−Speed Mode, $C_B \le 400$ pF		20	160	
t_{RDA}	SDA Rise Time	Standard Mode		$20+0.1C_B$	1000	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High−Speed Mode, $C_B \le 100$ pF		10	80	
		High−Speed Mode, $C_B \le 400$ pF		20	160	

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Table 11. I²C TIMING SPECIFICATIONS (continued)
Guaranteed by design.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{FDA}	SDA Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High−Speed Mode, $C_B \le 100$ pF		10	80	
		High−Speed Mode, $C_B \le 400$ pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		120		ns
		High−Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

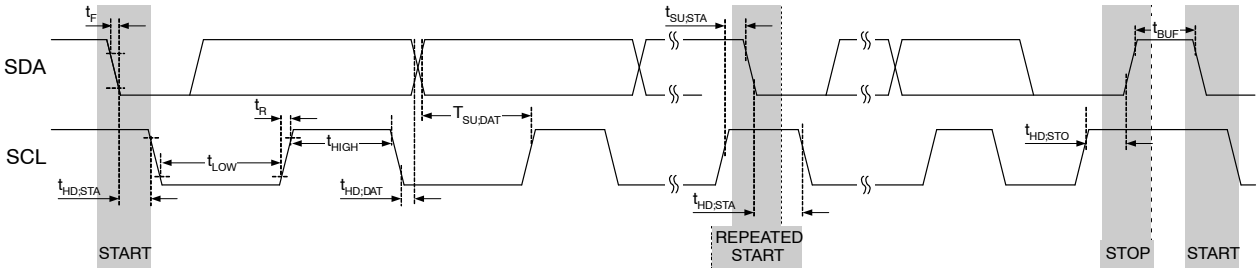
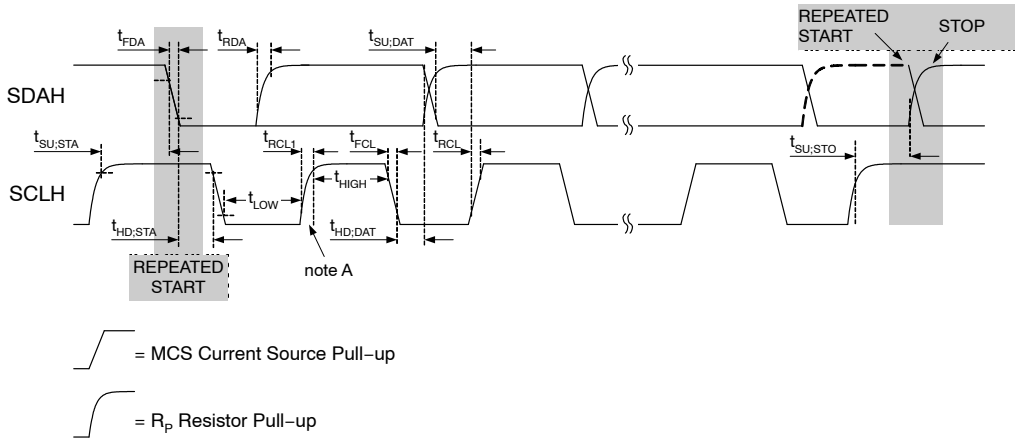


Figure 5. I²C Interface Timing for Fast Plus, Fast, and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 6. I²C Interface Timing for High−Speed Mode

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Typical Characteristics

Unless otherwise specified, Auto PFM/PWM, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, SCL = SDA = VSEL = EN = 1.8 V, T_A = 25°C; circuit and components according to Figure 1 and Table 1.

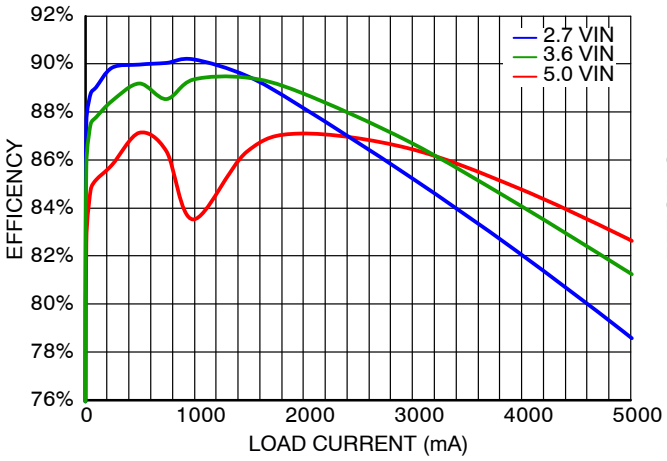


Figure 7. Efficiency vs. Load Current and Input Voltage

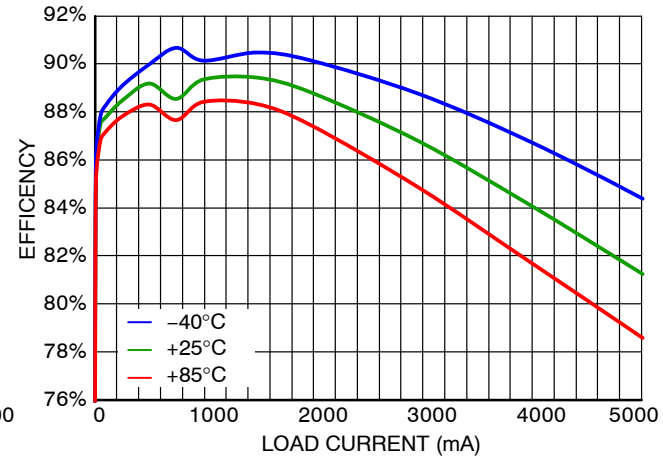


Figure 8. Efficiency vs. Load Current and Temperature

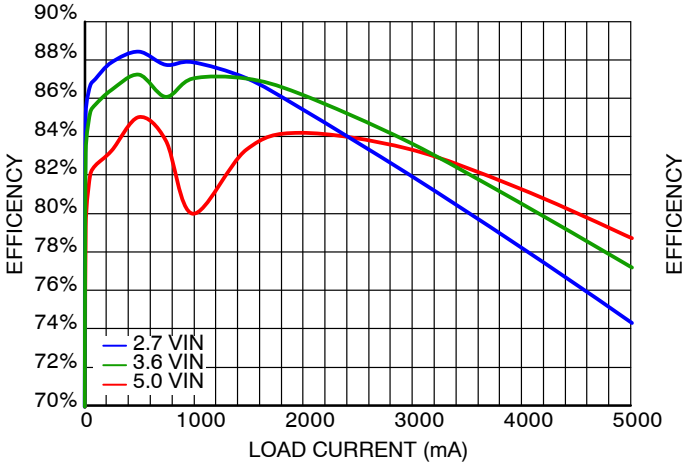


Figure 9. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 0.9 V

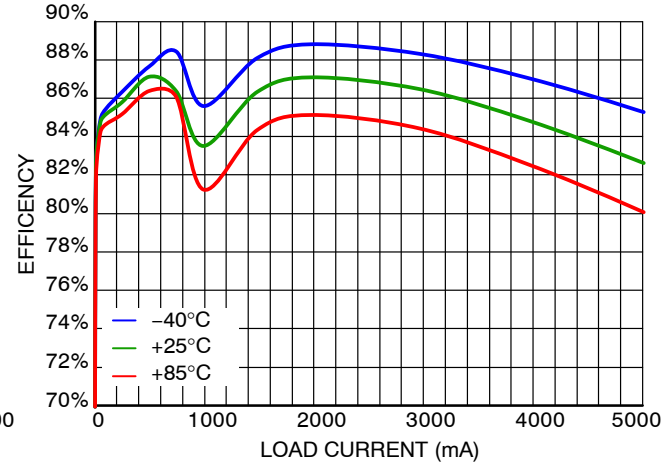


Figure 10. Efficiency vs. Load Current and Temperature, V_{IN} = 5 V, V_{OUT} = 1.2 V

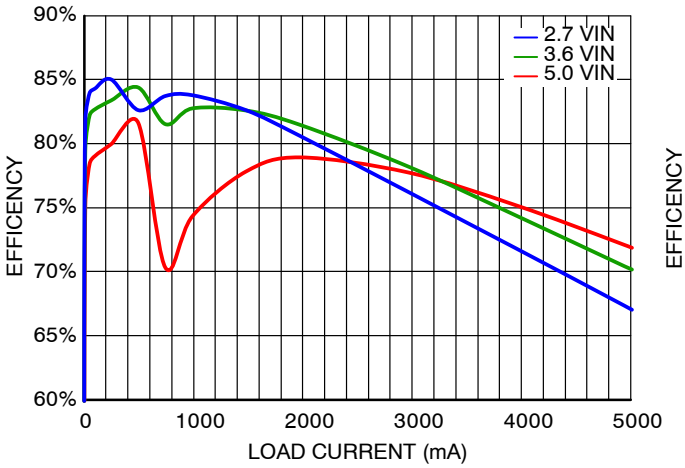


Figure 11. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 0.6 V

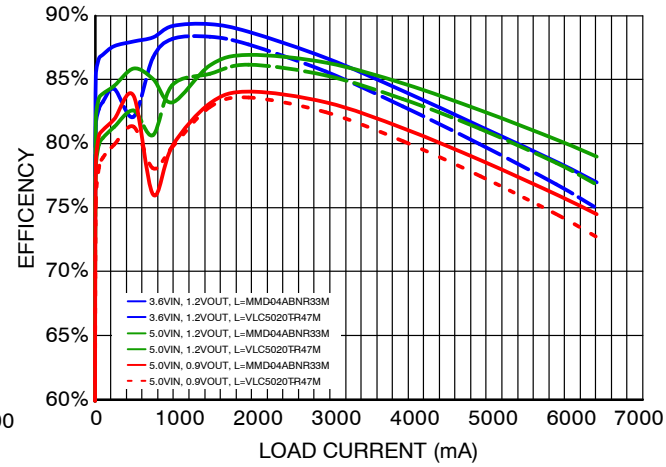


Figure 12. Efficiency vs. Load Current, V_{IN} = 3.6 V and 5 V, V_{OUT} = 1.2 V and 0.9 V

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Typical Characteristics (continued)

Unless otherwise specified, Auto PFM/PWM, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, SCL = SDA = VSEL = EN = 1.8 V, T_A = 25°C; circuit and components according to Figure 1 and Table 1.

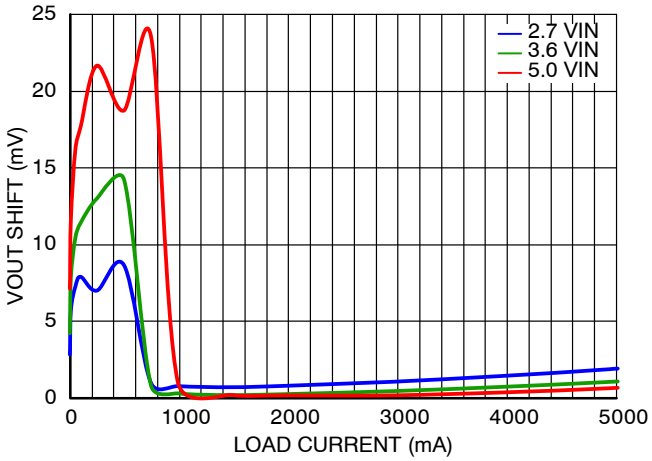


Figure 13. Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 1.2 V

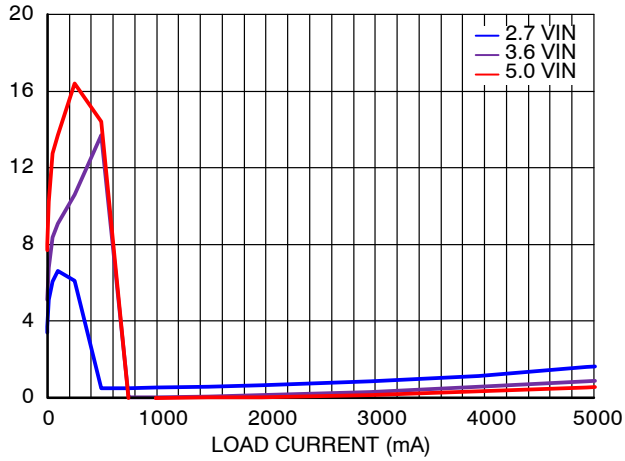


Figure 14. Output Regulation vs. Load Current and Input Voltage, V_{OUT}=0.9 V

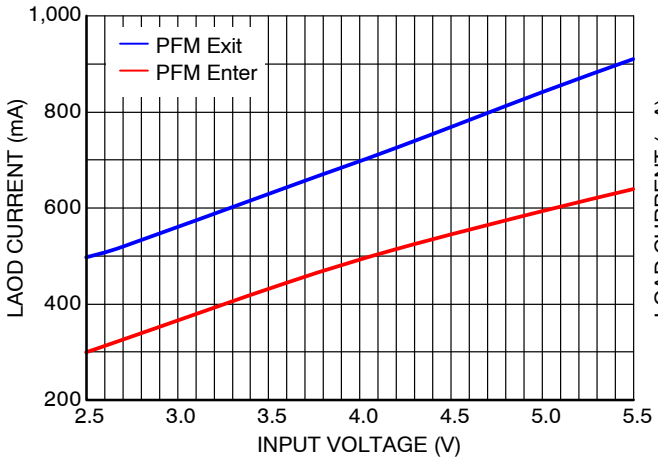


Figure 15. PFM Entry / Exit Level vs. Input Voltage, V_{OUT} = 1.2 V

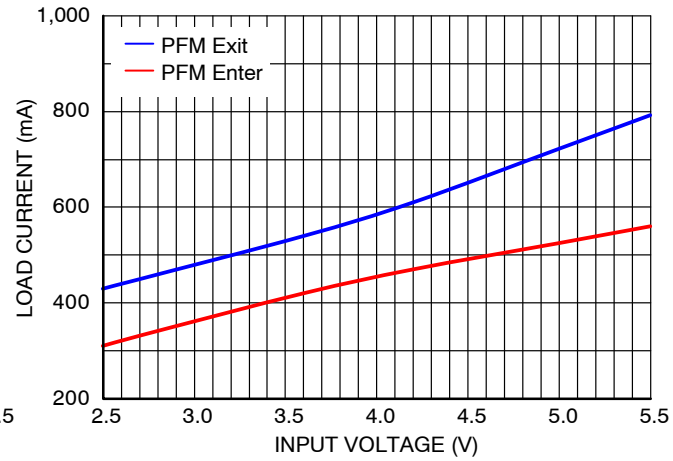


Figure 16. PFM Entry / Exit Level vs. Input Voltage, V_{OUT} = 0.9 V

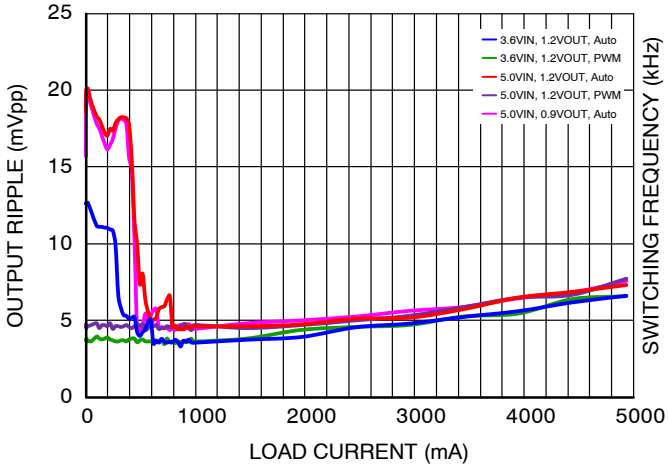


Figure 17. Output Ripple vs. Load Current, V_{IN} = 5 V and 3.6 V, V_{OUT} = 1.2 V and 0.9 V, Auto and FPWM

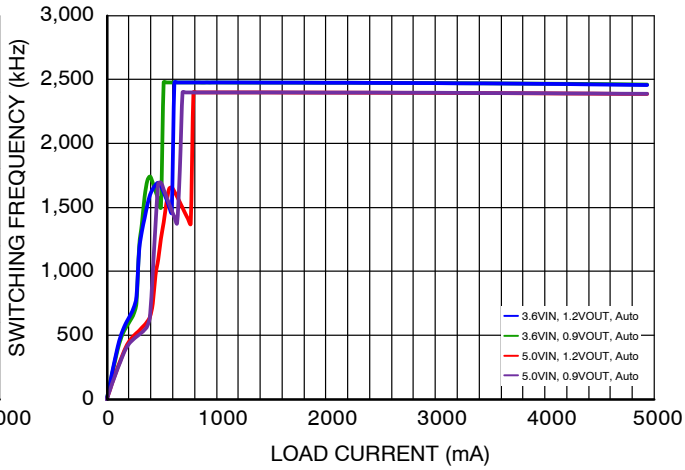


Figure 18. Frequency vs. Load Current, V_{IN} = 5 V and 3.6 V, V_{OUT} = 1.2 V and 0.9 V, Auto PWM

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Typical Characteristics (Continued)

Unless otherwise specified, Auto PFM/PWM, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, SCL = SDA = VSEL = EN = 1.8 V, T_A = 25°C; circuit and components according to Figure 1 and Table 1.

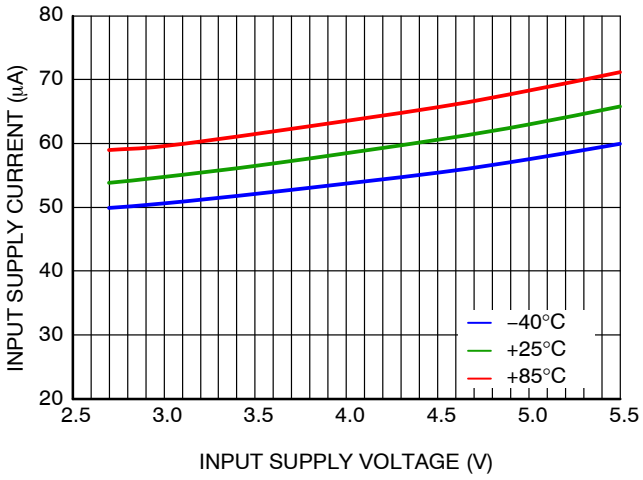


Figure 19. Quiescent Current vs. Input Voltage and Temperature, Auto PWM

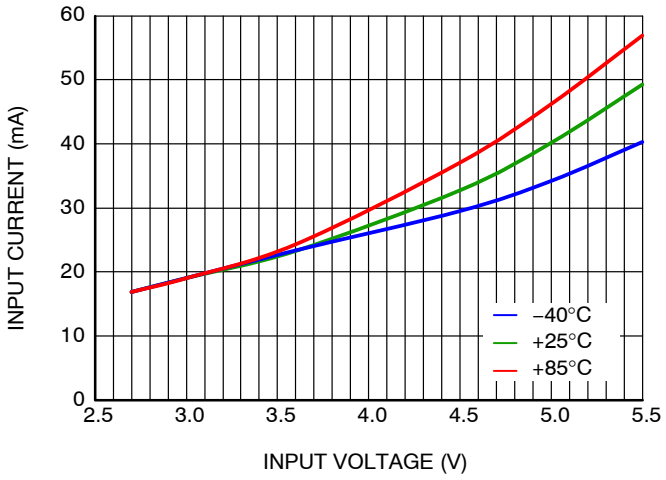


Figure 20. Quiescent Current vs. Input Voltage and Temperature, FPWM

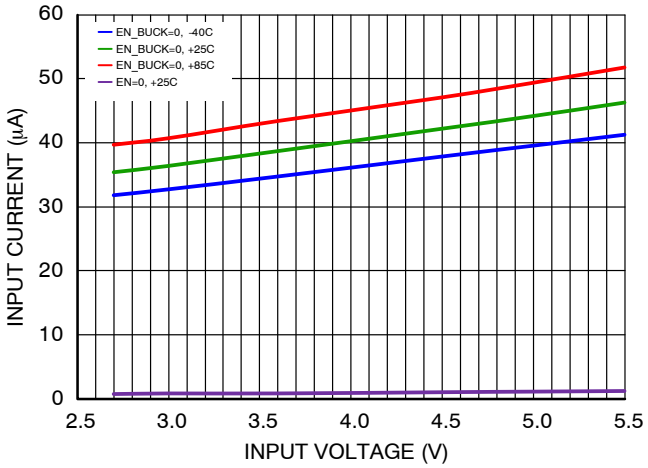


Figure 21. Shutdown Current vs. Input Voltage and Temperature

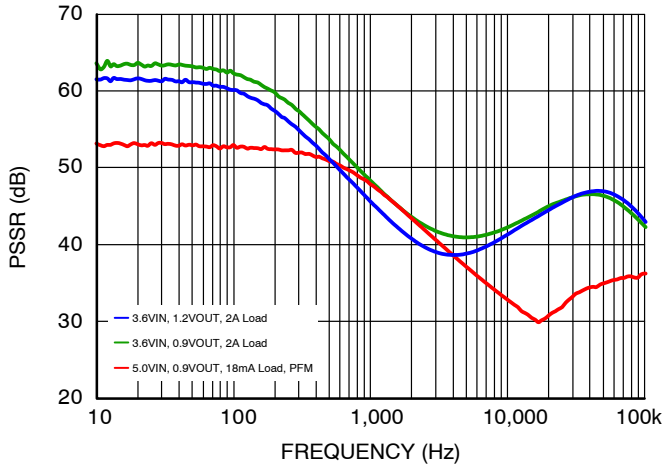


Figure 22. PSRR vs. Frequency

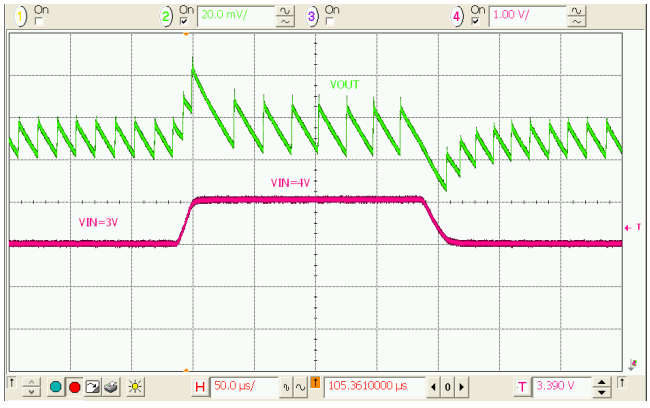


Figure 23. Line Transient, 3–4 V_{IN}, 1.2 V_{OUT}, 10 µs Edge, 50 Ω Load

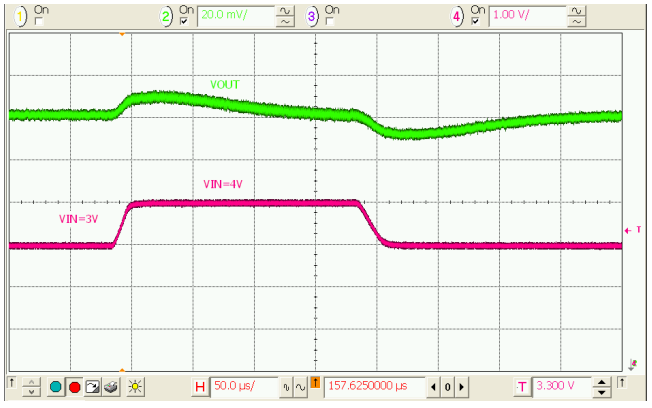


Figure 24. Line Transient, 3–4 V_{IN}, 1.2 V_{OUT}, 10 µs Edge, 1 A Load

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Typical Characteristics (Continued)

Unless otherwise specified, Auto PFM/PWM, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, SCL = SDA = VSEL = EN = 1.8 V, T_A = 25°C; circuit and components according to Figure 1 and Table 1.

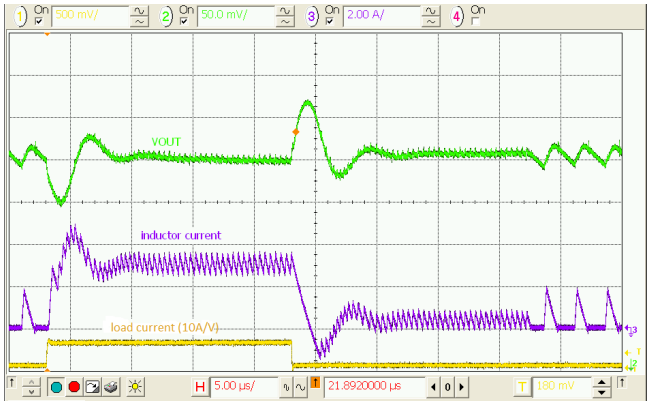


Figure 25. Load Transient, 5 V_{IN}, 0.9 V_{OUT}, 0.3–3 A, 100 ns Edge

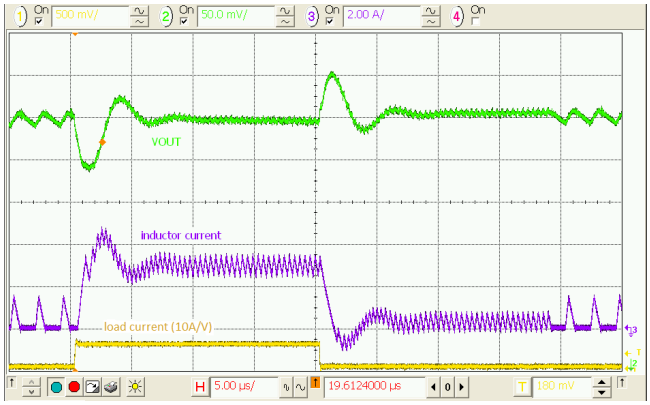


Figure 26. Load Transient, 3.6 V_{IN}, 1.2 V_{OUT}, 0.3–3 A, 100 ns Edge

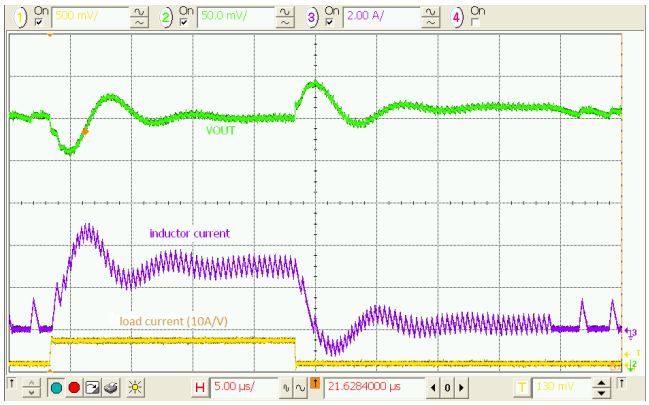


Figure 27. Load Transient, 3.6 V_{IN}, 1.2 V_{OUT}, 0.3–3 A, 100 ns Edge, C_{OUT} = 4x22 µF

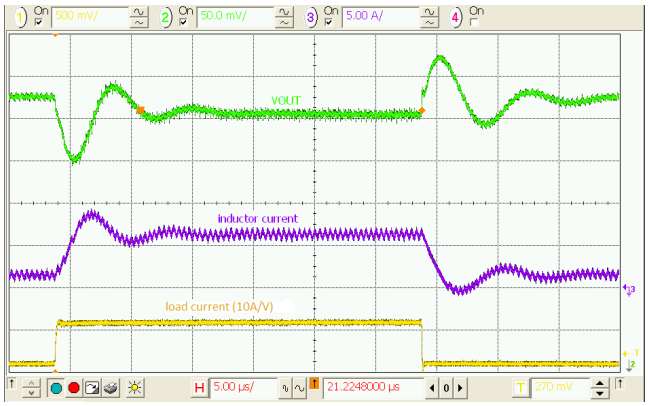


Figure 28. Load Transient, 3.6 V_{IN}, 1.2 V_{OUT}, 1.5–6 A, 100 ns Edge, C_{OUT} = 4x22 µF

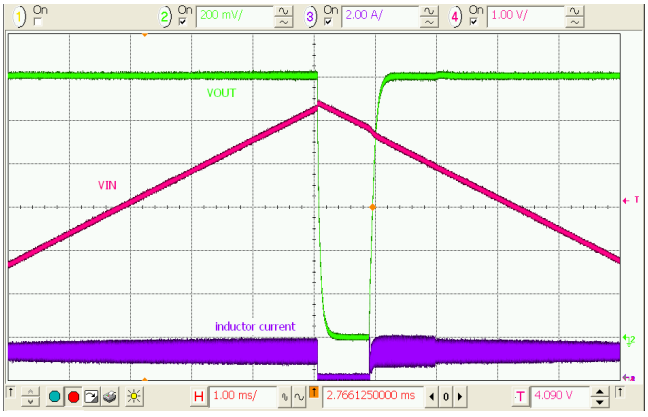


Figure 29. Input Over−Voltage Protection

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Typical Characteristics (Continued)

Unless otherwise specified, Auto PFM/PWM, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, SCL = SDA = VSEL = EN = 1.8 V, T_A = 25°C; circuit and components according to Figure 1 and Table 1.

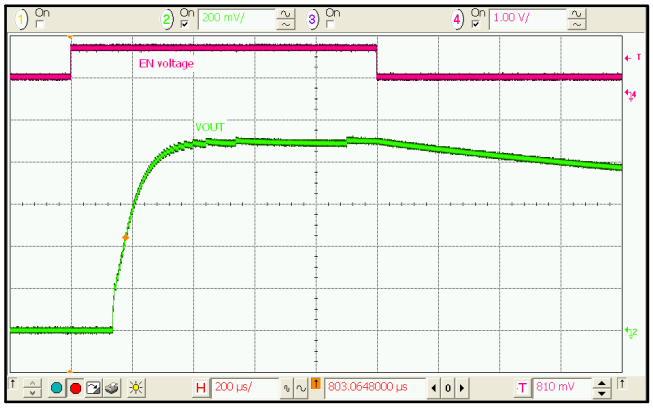


Figure 30. Startup / Shutdown, No Load, V_{OUT} = 0.9 V

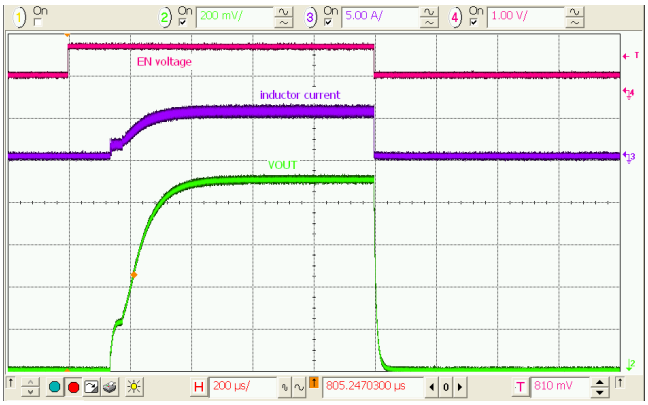


Figure 31. Startup / Shutdown, 180 mΩ Load, V_{OUT} = 0.9 V

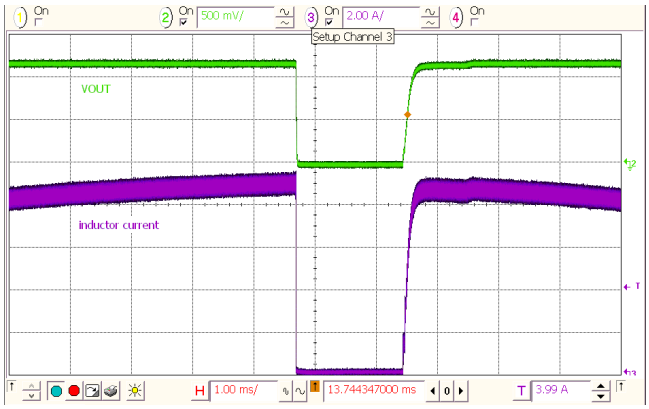


Figure 32. Overload Protection and Recovery

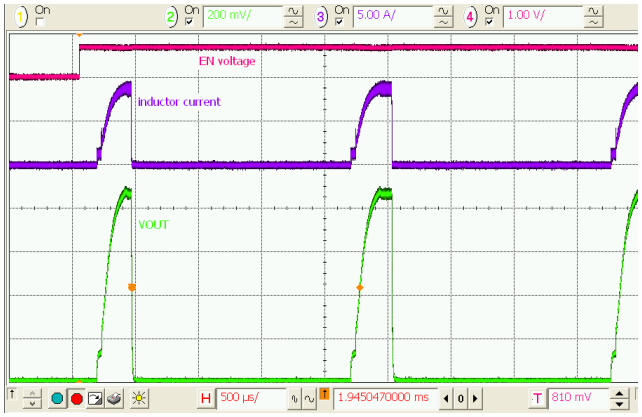


Figure 33. Startup into Faulted Load, V_{OUT} = 0.9 V

OPERATION DESCRIPTION

The FAN53555 is a step−down switching voltage regulator that delivers a programmable output voltage from an input voltage supply of 2.5 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53555 is capable of delivering 5 A at over 80% efficiency. Pulse currents as high as 6.5 A can be supported by the 05 option. The regulator operates at a nominal frequency of 2.4 MHz at full load, which reduces the value of the external components to 330 nH for the output inductor and 22 μF for the output capacitor. High efficiency is maintained at light load with single−pulse PFM.

The FAN53555 integrates an I^2C−compatible interface, allowing transfers up to 3.4 Mbps. This communication interface can be used to:

- Dynamically re−program the output voltage in 10 mV, 12.826 mV increments (option 04, 09, and 042), 12.5 mV increments (option 23), or 12.967 mV increments (option 24);
- Reprogram the mode to enable or disable PFM;
- Control voltage transition slew rate; or
- Enable / disable the regulator.

Control Scheme

The FAN53555 uses a proprietary non−linear, fixed−frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53555 operates in Discontinuous Current Diode (DCM) single−pulse PFM,

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which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is relatively seamless, providing a smooth transition between DCM and CCM Modes.

PFM can be disabled by programming the MODE bit HIGH in the VSEL registers.

Enable and Soft−Start

When the EN pin is LOW; the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, I^2C cannot be written to or read from. For all options except the 04, 24, and 042 options, all register values are kept while EN pin is LOW. For the 04, 24 042 and 79 options; registers are reset to default values when EN pin is LOW. For all options, registers are reset to default values during a Power On Reset (POR).

When the OUTPUT_DISCHARGE bit in the CONTROL register is enabled (logic HIGH) and the EN pin is LOW or the BUCK_ENx bit is LOW, a load is connected from VOUT to GND to discharge the output capacitors.

Raising EN while the BUCK_ENx bit is HIGH activates the part and begins the soft−start cycle. During soft−start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. Synchronous rectification is inhibited during soft−start, allowing the IC to start into a pre−charged capacitive load.

If large output capacitance values are used, the regulator may fail to start. Maximum C_{OUT} capacitance for successfully starting with a heavy constant−current load is approximately:

$$C_{OUTMAX} = \left(I_{LIMPK} - I_{LOAD}\right) \cdot \frac{320\mu}{V_{OUT}} \quad \text{(eq. 1)}$$

where C_{OUTMAX} is expressed in μF and I_{LOAD} is the load current during soft−start, expressed in A.

If the regulator is at its current limit for 16 consecutive current limit cycles, the regulator shuts down and enters 3−state before reattempting soft−start 1700 ms later. This limits the duty cycle of full output current during soft−start to prevent excessive heating.

The IC allows for software enable of the regulator, when EN is HIGH, through the BUCK_EN bits. BUCK_EN0 and BUCK_EN1 are both initialized HIGH in the 00, 04, 08, 09, 23, 24, 42 and 79 options. These options start after a POR regardless of the state of the VSEL pin.

In the 01 and 05 options, BUCK_EN0 and BUCK_EN1 are initialized to 10. Using these options, VSEL must be LOW after a POR if the IC is powering the processor used to communicate through I^2C. The 03 option has the VSEL input to the modulator logic internally tied LOW.

Table 12. HARDWARE AND SOFTWARE ENABLE

Pins		BITS		
EN	VSEL	BUCK_EN0	BUCK_EN1	Output
0	X	X	X	OFF
1	0	0	X	OFF
1	0	1	X	ON
1	1	X	0	OFF
1	1	X	1	ON

VSEL Pin and I^2C Programming Output Voltage

The output voltage is set by the NSELx control bits in VSEL0 and VSEL1 registers. The output voltage for options 00, 01, 03, 05, 08, 18 and 79 is given as:

$$V_{OUT} = 0.60\ V + NSELx \cdot 10\ mV \quad \text{(eq. 2)}$$

For example, when NSEL = 011111 (31 decimal), then V_{OUT} = 0.60 + 0.310 = 0.91 V.

For the 04, 042, and 09 options; the output voltage is given as:

$$V_{OUT} = 0.603 + NSELx \cdot 12.826\ mV \quad \text{(eq. 3)}$$

For the 13 option, the output voltage is given as:

$$V_{OUT} = 0.80 + NSELx \cdot 10\ mV \quad \text{(eq. 4)}$$

For the 23 option, the output voltage is given as:

$$V_{OUT} = 0.60\ V + NSELx \cdot 12.5\ mV \quad \text{(eq. 5)}$$

For the 24 option, the output voltage is given as:

$$V_{OUT} = 0.603\ V + NSELx \times 12.967\ mV \quad \text{(eq. 6)}$$

Output voltage can also be controlled by toggling the VSEL pin LOW or HIGH. VSEL LOW corresponds to VSEL0 and VSEL HIGH corresponds to VSEL1. Upon POR, VSEL0 and VSEL1 are reset to their default voltages, shown in Table 9.

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Transition Slew Rate Limiting

When transitioning from a low to high voltage, the IC can be programmed for one of eight possible slew rates using the SLEW bits in the CONTROL register.

Table 13. TRANSITION SLEW RATE

Decimal	Bin	Slew Rate	
0	000	64.00	mV / µs
1	001	32.00	mV / µs
2	010	16.00	mV / µs
3	011	8.00	mV / µs
4	100	4.00	mV / µs
5	101	2.00	mV / µs
6	110	1.00	mV / µs
7	111	0.50	mV / µs

Transitions from high to low voltage rely on the output load to discharge V_{OUT} to the new set point. Once the high−to−low transition begins, the IC stops switching until V_{OUT} has reached the new set point.

For options 04, 042, 09, 23, and 24 where the Dynamic Voltage Scaling (DVS) step is not 10 mV; the actual slew rate is the corresponding number shown in Table 6 scaled by the ratio of the DVS step to 10 mV. For example, the slew rate of option 13 for Bin=011 is 8.00 mV / µs x 12.5 mV / 10 mV = 10.00 mV / µs.

Under−Voltage Lockout

When EN is HIGH, the under−voltage lockout keeps the part from operating until the input supply voltage rises HIGH enough to properly operate. This ensures proper operation of the regulator during startup or shutdown.

Input Over−Voltage Protection (OVP)

When V_{IN} exceeds V_{SDWN} (about 6.2 V) the IC stops switching to protect the circuitry from internal spikes above 6.5 V. An internal filter prevents the circuit from shutting down due to noise spikes.

Power Good (03 & 79 Option)

The PGOOD pin is an open−drain output indicating that the regulator is enabled when its state is HIGH. PGOOD pulls LOW under the following conditions:

- Regulator is disabled (EN pin LOW, disabled by I^2C, fault time−out, UVLO, OVP, over−temperature);
- Regulator is performing a soft−start.

PGOOD remains HIGH during I^2C initiated V_{OUT} transitions.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from causing damage. Sixteen consecutive current limit cycles in current limit cause the regulator to shut down and stay off for about 1700 µs before attempting a restart.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 17°C hysteresis.

Monitor Register (Reg05)

The Monitor register indicates of the regulation state of the IC. If the IC is enabled and is regulating, its value is (1000 0000).

I^2C Interface

The FAN53555's serial interface is compatible with Standard, Fast, Fast Plus, and HS Mode I^2C−Bus specifications. The FAN53555's SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I^2C Slave Address

In hex notation, the slave address assumes a 0 LS Bit. The hex slave address is C0 for all options except −42, which has a hex slave address of C4.

Table 14. I^2C SLAVE ADDRESS

Option	Hex	Bits							
		7	6	5	4	3	2	1	0
00 to 24, 79	C0	1	1	0	0	0	0	0	R/$\overline{W}$
42	C4	1	1	0	0	0	1	0	R/$\overline{W}$

Other slave addresses can be assigned. Contact a **onsemi** representative.

Bus Timing

As shown in Figure 34, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

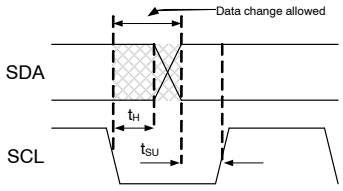


Figure 34. Data Transfer Timing

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Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 35.

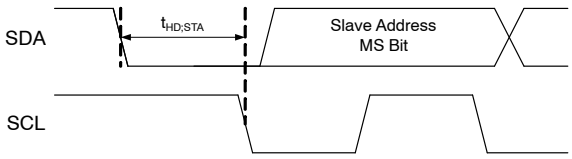


Figure 35. START Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 36.

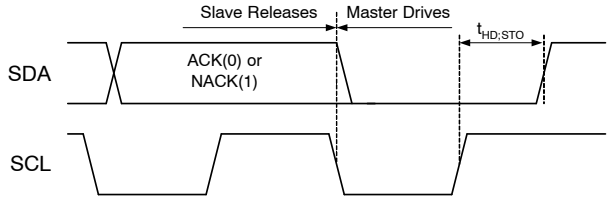


Figure 36. STOP Bit

During a read from the FAN53555, the master issues a REPEATED START after sending the register address, and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 37.

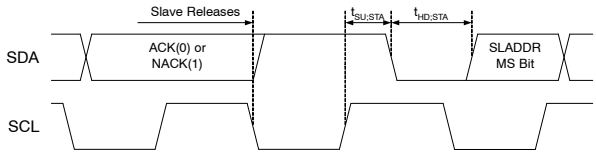


Figure 37. REPEATED START Timing

High−Speed (HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical, except the bus speed for HS mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition. The master code is sent in Fast or Fast−Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition () that causes all slaves on the bus to switch to HS Mode. The master then sends I^2C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 36) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 37).

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Buss. All addresses and data are MSB first.

Table 15. I^2C BIT DEFINITIONS FOR FIGURE 38 AND FIGURE 39

Symbol	Definition
R	REPEATED START, *see* Figure 37
P	STOP, *see* Figure 36
S	START, *see* Figure 35
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, *see* Figure 37.
P	STOP, *see* Figure 36.

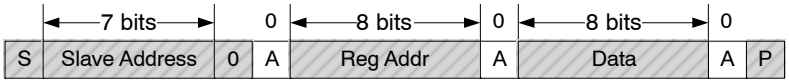


Figure 38. Write Transaction

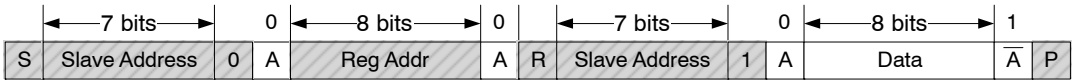


Figure 39. Read Transaction

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REGISTER DESCRIPTION

Table 16. REGISTER MAP

Hex Address	Name	Function	POR Default			
			Option	V_{OUT}	Binary	Hex
00	VSEL0	Controls V_{OUT} settings when VSEL pin = 0	00	1.050	10101101	AD
			08, 18	1.020	10101010	AA
			01, 03, 05	0.900	10011110	9E
			04	1.100	10100111	A7
			24	1.225	10110000	B0
			13	1.150	10100011	A3
			23	1.150	10101100	AC
			09	1.100	10100111	A7
			79	0.85	10011001	99
01	VSEL1	Controls V_{OUT} settings when VSEL pin = 1	00	1.200	11111100	FC
			01, 05	1.000	01101000	68
			04	1.200	11101111	EF
			24	1.212	10101111	AF
			08, 18	1.150	10110111	B7
			13	1.150	10100011	A3
			23	1.150	10101100	AC
			09	1.100	11100111	E7
02	CONTROL	Determines whether V_{OUT} output discharge is enabled and also the slew rate of positive transitions	00, 01, 03, 04, 05, 24		10000000	80
			08, 09, 18		00000000	00
			13, 23		10110000	B0
03	ID1	Read−only register identifies vendor and chip type	00, 13, 23, 24		10000000	80
			01		10000001	81
			79		10000010	82
			03		10000011	83
			04		10000100	84
			05		10000101	85
			08, 18		10001000	88
			09		10001100	8C
04	ID2	Read−only register identifies die revision	All		0000XXXX	0X
05	MONITOR	Indicates device status	All		X0000000	X0

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Table 17. BIT DEFINITIONS

The following table defines the operation of each register bit. Bold indicates power−on default values.

Bit	Name	Value	Description
VSEL0 R/W Register Address: 00			
7	BUCK_EN0	1	Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent.
6	MODE0	0	Allow Auto−PFM Mode during light load.
		1	Forced PWM Mode.
5:0	NSEL0	00 Option 101101	Sets V_{OUT} value from 0.6 to 1.23 V in 10 mV steps *(see Eq. (2))*.
		08, 18 Options 101010	
		01, 03, 05 Options 011110	
		79 Option **011001**	
		04 Option 100111	Sets V_{OUT} value from 0.603 to 1.411 V in 12.826 mV steps *(see Eq. (3))*.
		09 Option 100111	
		13 Option 100011	Sets V_{OUT} value from 0.8 to 1.43 V in 10 mV steps *(see Eq. (4))*.
		23 Option 101100	Sets V_{OUT} value from 0.6 to 1.3875 V in 12.5 mV steps *(see Eq. (5))*.
		24 Option 110000	Sets V_{OUT} value from 0.603 to 1.42 V in 12.967 mV steps *(see Eq. (6))*.
VSEL1 R/W Register Address: 01			
7	BUCK_EN1	00, 04, 08, 09,13, 18, 23, 24 Options 1	Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent.
		01, 05 Options 0	
6	MODE1	08, 13, 18, 23, 24 Options 0	Allow AUTO−PFM Mode during light load.
		00, 01, 04, 05, 09 Options 1	Forced PWM Mode.

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Table 17. BIT DEFINITIONS (continued)
The following table defines the operation of each register bit. Bold indicates power−on default values.

Bit	Name	Value	Description
VSEL1 R/W Register Address: 01			
5:0	NSEL1	00 Option 111100	Sets V_{OUT} value from 0.6 to 1.23 V in 10 mV steps *(see Eq. (2))*.
		01, 05 Options 101000	
		08, 18 Options 110111	
		04 Option 101111	Sets V_{OUT} value from 0.603 to 1.411 V in 12.826 mV steps *(see Eq. (3))*.
		09 Option 100111	
		13 Option 100011	Sets V_{OUT} value from 0.8 to 1.43 V in 10 mV steps *(see Eq. (4))*.
		23 Option 010100	Sets V_{OUT} value from 0.6 to 1.3875 V in 12.5 mV steps *(see Eq. (5))*.
		24 Option 101111	Sets V_{OUT} value from 0.603 to 1.42 V in 12.967 mV steps *(see Eq. (6))*.
CONTROL R/W Register Address: 02			
7	OUTPUT_DISCHARGE	08, 09, 18, 79 Options 0	When the regulator is disabled, V_{OUT} is not discharged.
		00, 01, 03, 04, 05,13, 23, 24 Options 1	When the regulator is disabled, V_{OUT} discharges through an internal pull−down.
6:4	SLEW	000 −111	Sets the slew rate for positive voltage transitions *(see*
		011	Default value for 13 and 23 options
3	Reserved	0	Always reads back 0
2	04, 09, 24, 79 Options RESET	0	Setting to 1 resets all registers to default values.
	All other options Reserved	0	Always reads back 0
1:0	Reserved	00	Always reads back 00
ID1 R Register Address: 03			
7:5	VENDOR	100	Signifies **onsemi** as the IC vendor
4	Reserved	0	Always reads back 0

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Table 17. BIT DEFINITIONS (continued)
The following table defines the operation of each register bit. Bold indicates power−on default values.

Bit	Name	Value	Description
ID1	**R**	**Register Address: 03**	
3:0	DIE_ID	0000	IC Type = 00 Option (FAN53555UC00X / FAN53555BUC24X)
		0001	IC Type = 01 Option (FAN53555UC01X)
		0010	IC Type = 79 Option (FAN53555BUC79X)
		0011	IC Type = 03 Option (FAN53555UC03X)
		0100	IC Type = 04 Option (FAN53555UC04X)
		0100	IC Type = 042 Option (FAN53555UC042X)
		0101	IC Type = 05 Option (FAN53555UC05X / FAN53555BUC05X)
		1000	IC Type = 08, 18 Options (FAN53555UC08X / FAN53555BUC08X, FAN53555UC18X / FAN53555BUC18X)
		1100	IC Type = 09 Option (FAN53555UC09X / FAN53555BUC09X)
		0000	IC Type = 13 Option (FAN53555UC13X / FAN53555BUC13X)
		0000	IC Type = 23 Option (FAN53555BUC23X)
ID2	**R**	**Register Address: 04**	
7:4	Reserved	0000	Always reads back 0000
3:0	DIE_REV	00 Option 0011	IC mask revision
		01 Option 0011	
		03 Option 0011	
		04 Option 1111	
		24−Option 0100	
		042 Option 1111	
		05 Option 0011	
		08, 18 Options 0001	
		BUC08, BUC18 Options 1111	
		09 Option 1111	
		13 Option 1111	
		23 Option 1100	
		79 Option **1000**	
MONITOR	**R**	**Register Address: 05**	
7	PGOOD	0	1: buck is enabled and soft−start is completed
6:0	Not used	000 0000	Always reads back 000 0000

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APPLICATION INFORMATION

Selecting the Inductor

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I = \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{sw}} \right) \quad \text{(eq. 7)}$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current such that:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad \text{(eq. 8)}$$

The FAN53555 is optimized for operation with L = 330 nH, but is stable with inductances up to 1.0 μH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so lowers the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin−effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^{\ 2} + \frac{\Delta I^2}{12}} \quad \text{(eq. 9)}$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs as well as the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Table 18. EFFECTS OF INDUCTOR VALUE (FROM 330 nH RECOMMENDED) ON REGULATOR PERFORMANCE

$I_{MAX(LOAD)}$	ΔV_{OUT} (Eq.(11))	Transient Response
Increase	Decrease	Degraded

Inductor Current Rating

The current limit circuit can allow substantial peak currents to flow through L1 under worst−case conditions. If it is possible for the load to draw such currents, the inductor should be capable of sustaining the current or failing in a safe manner.

For space−constrained applications, a lower current rating for L1 can be used. The FAN53555 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor.

Output Capacitor and V_{OUT} Ripple

Table 1 suggests 0805 capacitors, but 0603 capacitors may be used if space is at a premium. Due to voltage effects, the 0603 capacitors have a lower in−circuit capacitance than the 0805 package, which can degrade transient response and output ripple.

Increasing C_{OUT} has negligible effect on loop stability and can be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is calculated by:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right] \quad \text{(eq. 10)}$$

where C_{OUT} is the effective output capacitance.

The capacitance of C_{OUT} decreases at higher output voltages, which results in higher ΔV_{OUT}. Equation (10) is only valid for Continuous Current Mode (CCM) operation, which occurs when the regulator is in PWM Mode.

For large C_{OUT} values, the regulator may fail to start under a load. If an inductor value greater than 1.0 μH is used, at least 30 μF of C_{OUT} should be used to ensure stability.

The lowest ΔV_{OUT} is obtained when the IC is in PWM Mode and, therefore, operating at 2.4 MHz. In PFM Mode, f_{SW} is reduced, causing ΔV_{OUT} to increase.

ESL Effects

The Equivalent Series Inductance (ESL) of the output capacitor network should be kept low to minimize the square−wave component of output ripple that results from the division ratio C_{OUT} ESL and the output inductor (L_{OUT}). The square−wave component due to the ESL can be estimated as:

$$\Delta VOUT(SQ) \approx V_{IN} \cdot \frac{ESL_{COUT}}{L1} \quad \text{(eq. 11)}$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value. For example, to obtain C_{OUT} = 20 μF, a single 22 μF 0805 would produce twice the square wave ripple as two x 10 μF 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805s have lower ESL than 1206s. If low output ripple is a chief concern, some vendors produce 0508 or 0612 capacitors with ultra−low ESL. Placing additional small−value capacitors near the load also reduces the high−frequency ripple components.

Input Capacitor

The ceramic input capacitors should be placed as close as possible between the VIN pin and PGND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or

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tantalum) should be placed between C_{IN} and the power source lead to reduce under−damped ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective C_{IN} capacitance value decreases as V_{IN} increases due to DC bias effects. This has no significant impact on regulator performance.

Thermal Considerations

Heat is removed from the IC through the solder bumps to the PCB copper. The junction−to−ambient thermal resistance (θ_{JA}) is largely a function of the PCB layout (size, copper weight, and trace width) and the temperature rise from junction to ambient (ΔT).

For the FAN53555UC, θ_{JA} is 38°C/W when mounted on its four−layer evaluation board in still air with two−ounce outer layer copper weight and one−ounce inner layers. Halving the copper thickness results in an increased θ_{JA} of 48°C/W.

For long−term reliable operation, the IC's junction temperature (T_J) should be maintained below 125°C.

To calculate maximum operating temperature ($\leq$125°C) for a specific application:

1. Use efficiency graphs to determine efficiency for the desired V_{IN}, V_{OUT}, and load conditions.
2. Calculate total power dissipation using:

$$P_T = V_{OUT} \times I_{LOAD} \times \left(\frac{1}{\eta} - 1\right) \quad \text{(eq. 12)}$$

where η is efficiency from Figure 7 through Figure 12.

3. Estimate inductor copper losses using:

$$P_L = I_{LOAD}{}^2 \times DCR_L \quad \text{(eq. 13)}$$

4. Determine IC losses by removing inductor losses (step 3) from total dissipation:

$$P_{IC} = P_T - P_L \quad \text{(eq. 14)}$$

5. Determine device operating temperature:

$$\Delta T = P_{IC} \times \theta_{szie}7JA \quad \text{(eq. 15)}$$

and

$$T_{IC} = T_A + \Delta T \quad \text{(eq. 16)}$$

It is important to note that the $R_{DS(ON)}$ of the IC's power MOSFETs increases linearly with temperature at about 1.21%/°C. This causes the efficiency (η) to degrade with increasing die temperature.

LAYOTUT RECOMMENDATION

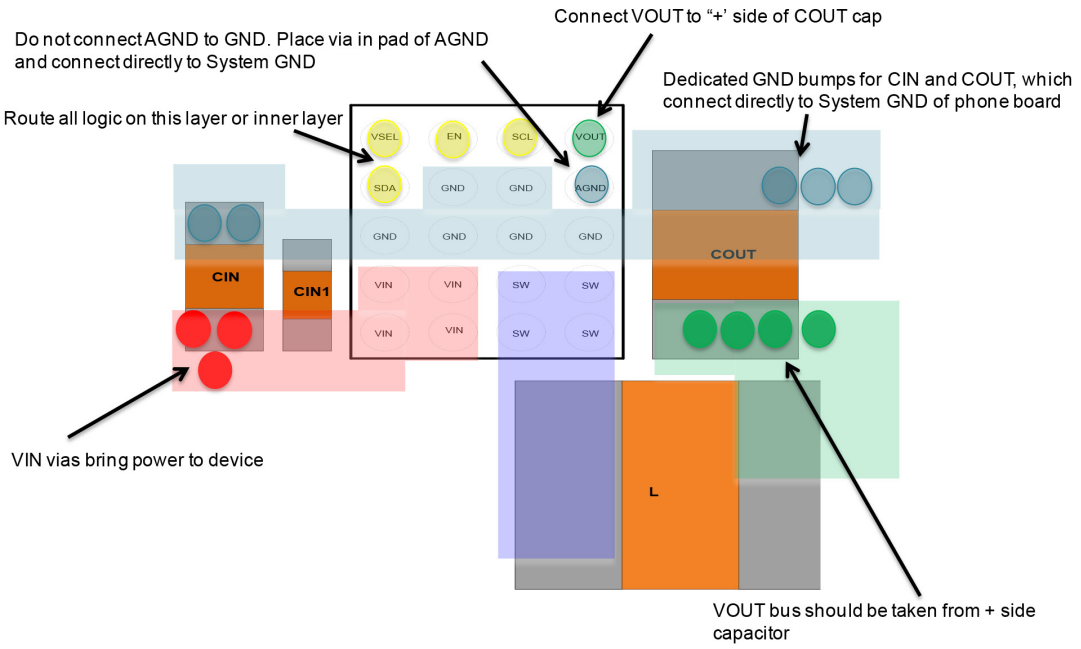


Figure 40. Guidance for Layer 1

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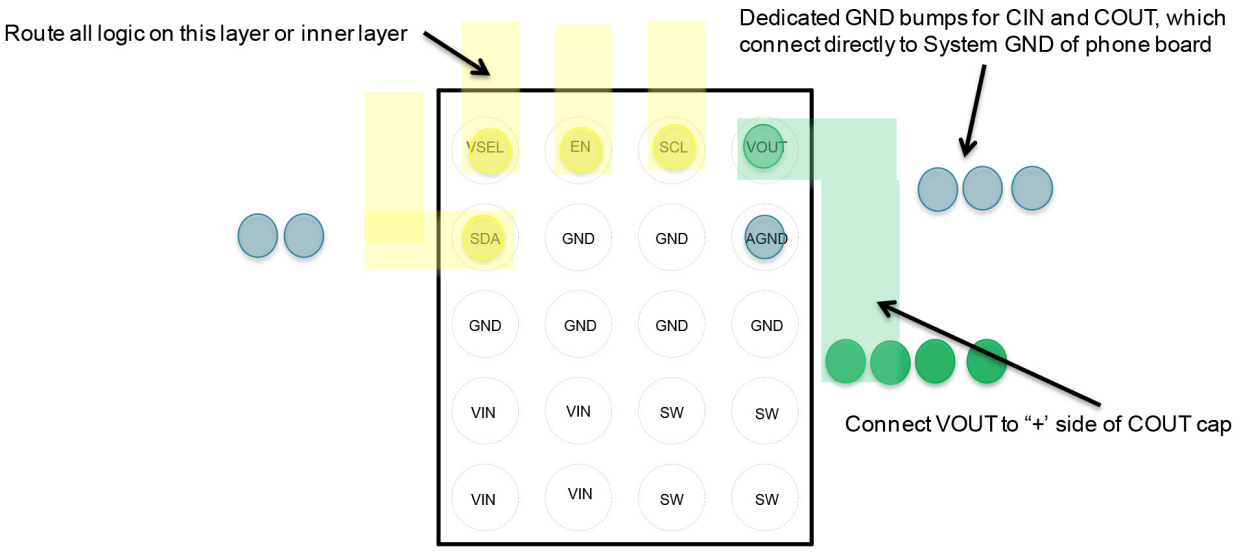


Figure 41. Guidance for Layer 2

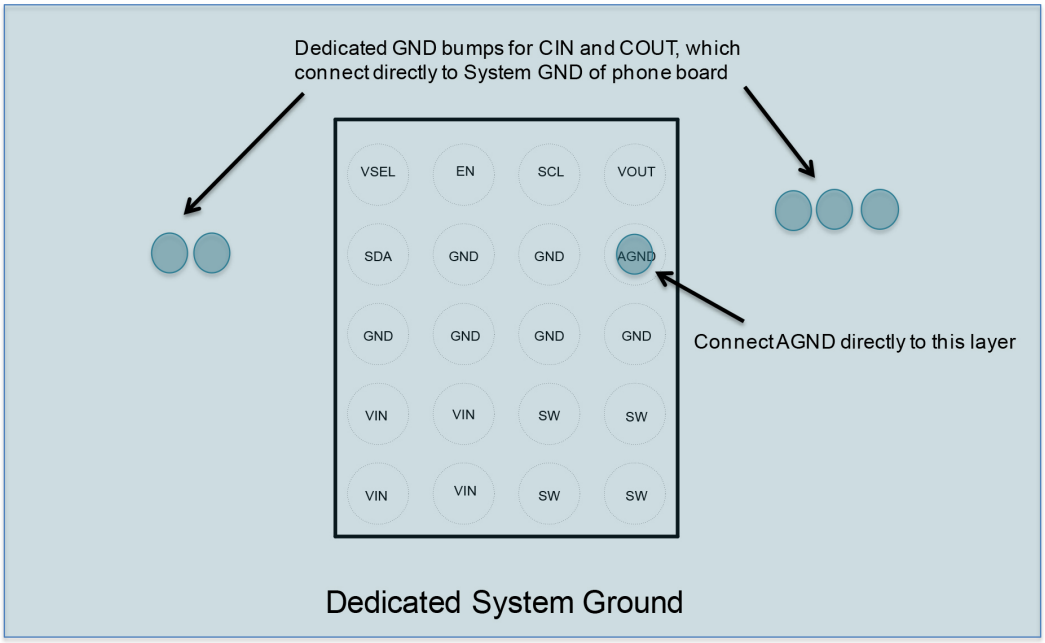
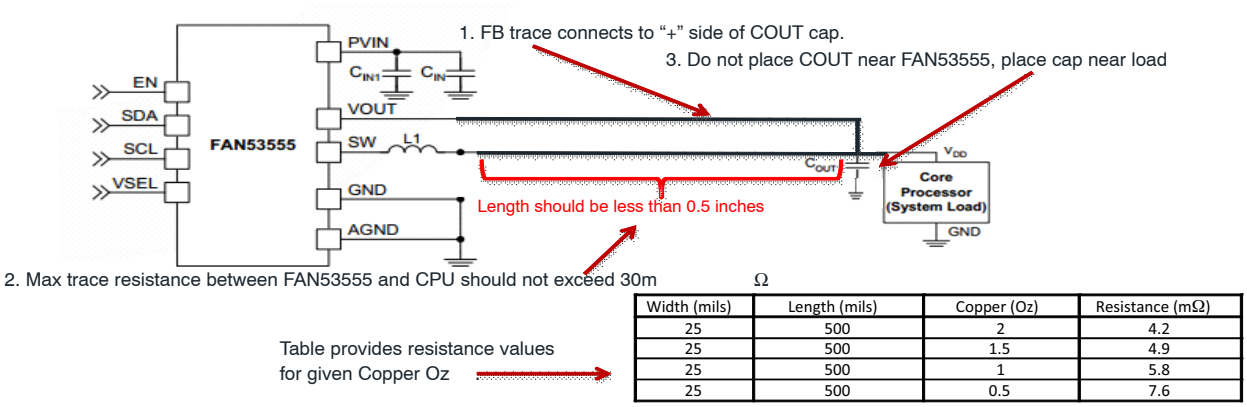


Figure 42. Guidance for Layer 3

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Width (mils)	Length (mils)	Copper (Oz)	Resistance (mΩ)
25	500	2	4.2
25	500	1.5	4.9
25	500	1	5.8
25	500	0.5	7.6

Figure 43. Remote Sensing Schematic

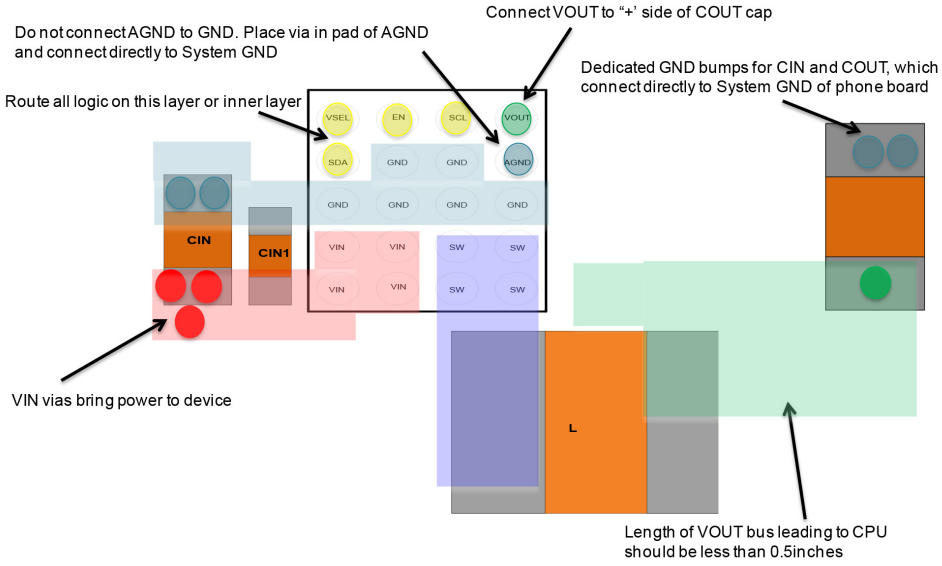


Figure 44. Remote Sensing Guidance, Top Layer

Table 19. Product−Specific Dimensions

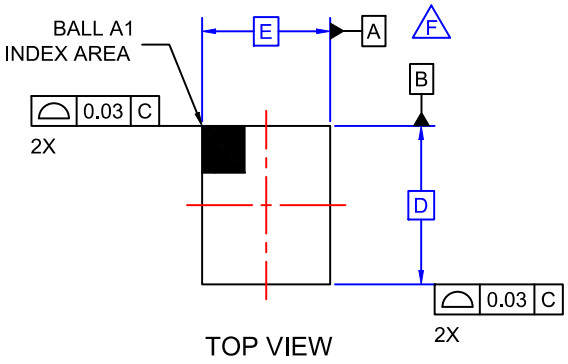
Product	D	E	X	Y	Land Pattern
FAN53555UC00 to FAN53555UC08X, FAN53555BUC05X, FAN53555UC042X	2.000 ±0.03	1.600 ±0.03	0.200	0.200	Option 1
FAN53555BUC08X, FAN53555BUC09X, FAN53555UC09X, FAN53555UC13X, FAN53555BUC13X, FAN53555UC18X, FAN53555BUC18X, FAN53555BUC23X, FAN53555UC24X, FAN53555BUC24X, FAN53555BUC79X	2.015 ±0.03	1.615 ±0.03	0.2075	0.2075	Option 2

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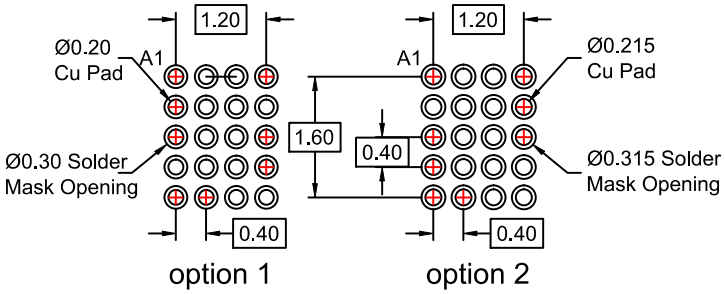
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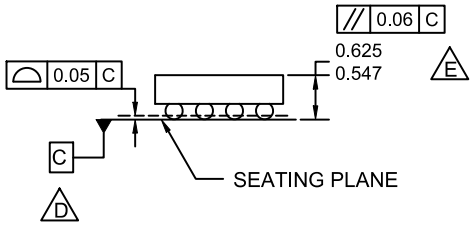
DATE 31 OCT 2016

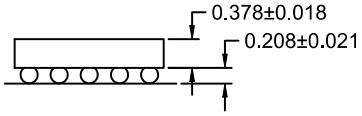


TOP VIEW

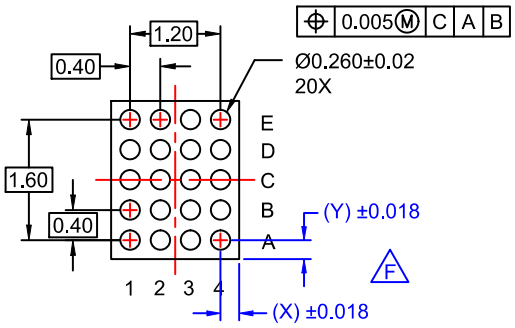


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SIDE VIEWS



BOTTOM VIEW

NOTES:

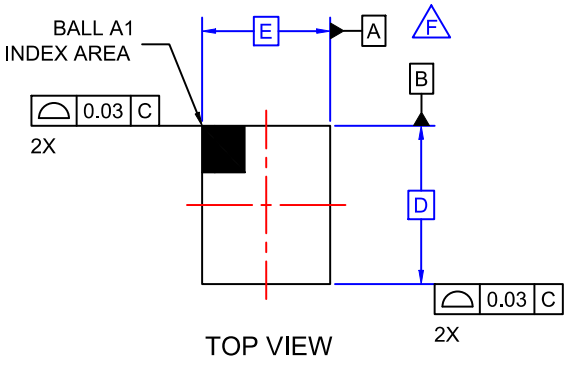
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B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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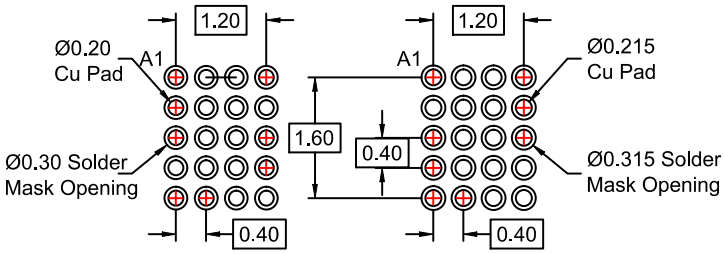
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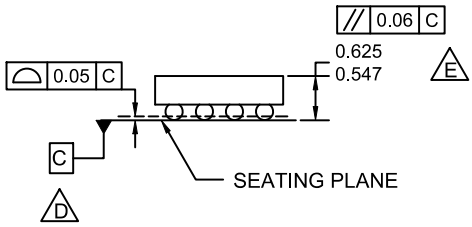
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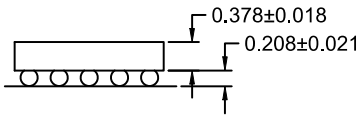


TOP VIEW

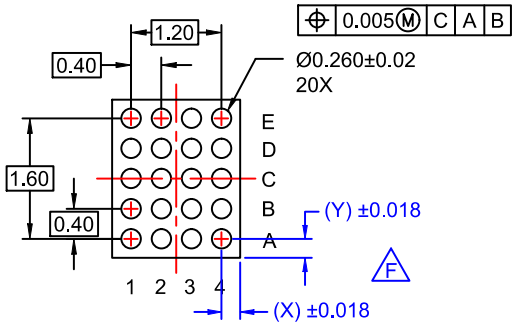


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SIDE VIEWS



BOTTOM VIEW

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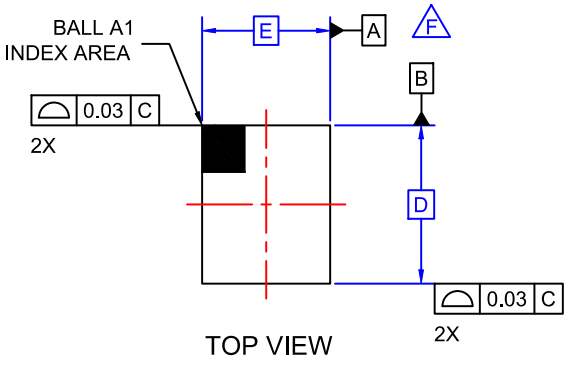
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C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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DESCRIPTION:	**WLCSP20 2.015x1.615x0.586**	**PAGE 1 OF 1**

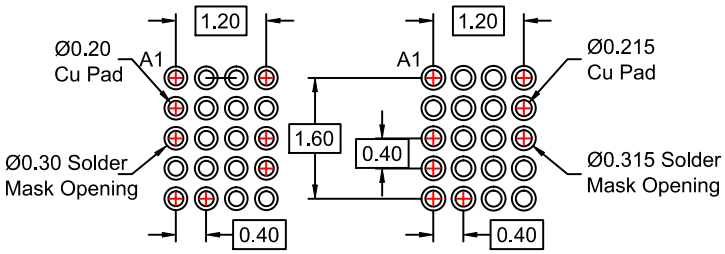
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WLCSP20 2.0x1.6x0.586
CASE 567SK
ISSUE O

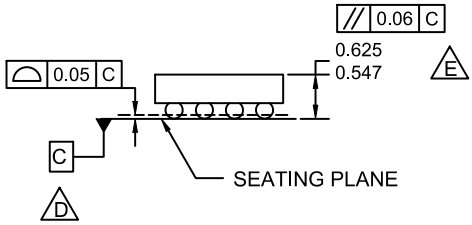
DATE 30 NOV 2016

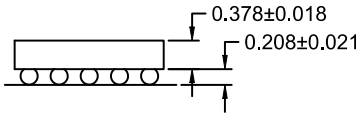


TOP VIEW

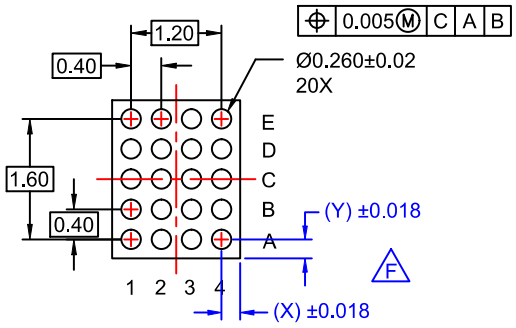


RECOMMENDED LAND PATTERN
(NSMD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
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