Complementary Silicon Plastic Power Transistors

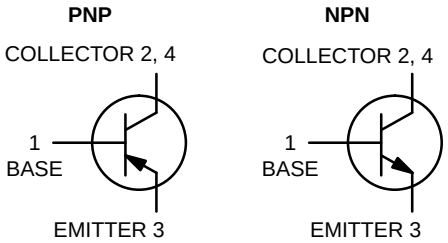
MJE2955T (PNP), MJE3055T (NPN)

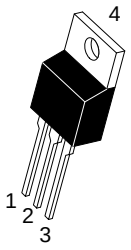
10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60 VOLTS − 75 WATTS

These devices are designed for use in general-purpose amplifier and switching applications.

Features

- High Current Gain − Bandwidth Product
- These Devices are Pb-Free and are RoHS Compliant*





TO-220
CASE 221A-09
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D (Note 1)	 75 0.6	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

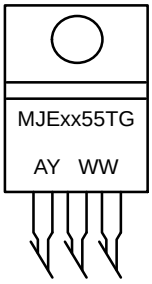
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.67	°C/W

MARKING DIAGRAM



MJExx55T = Device Code
xx = 29 or 30
G = Pb-Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJE2955TG	TO-220 (Pb-Free)	50 Units / Rail
MJE3055TG	TO-220 (Pb-Free)	50 Units / Rail

* For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (Note 2) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150 °C)	I_{CEX}	– –	1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150 °C)	I_{CBO}	– –	1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (Note 2) (I_C = 4.0 Adc, V_{CE} = 4 0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	100 –	–
Collector-Emitter Saturation Voltage (Note 2) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 8.0	Vdc
Base-Emitter On Voltage (Note 2) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	–	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 20%.

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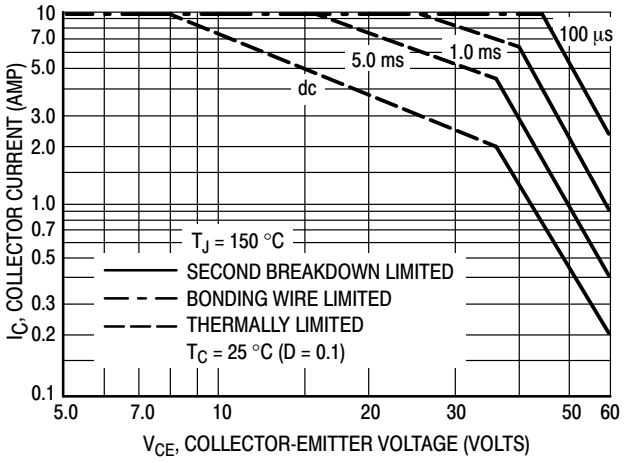


Figure 1. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150 °C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150$ °C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

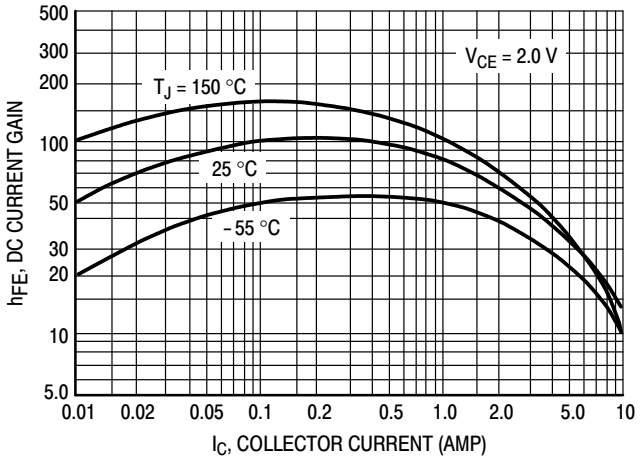


Figure 2. DC Current Gain

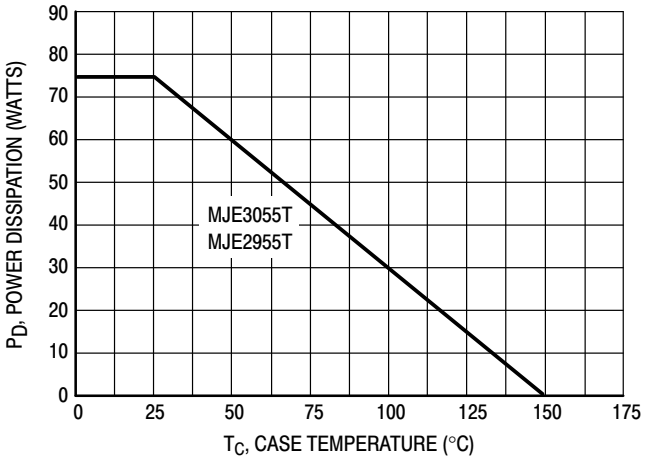


Figure 3. Power Derating

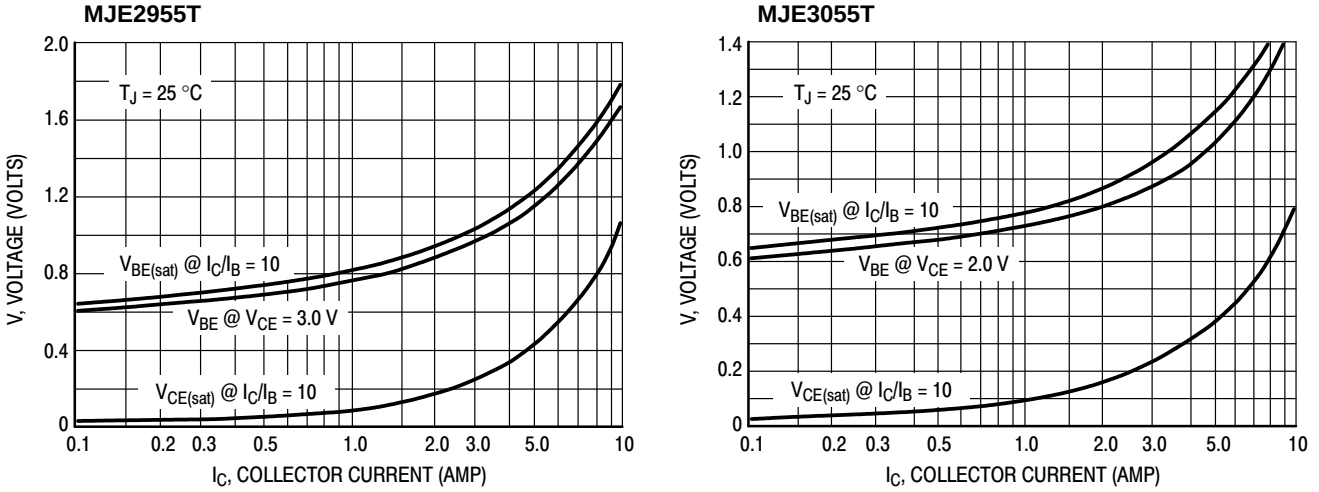


Figure 4. “On” Voltages

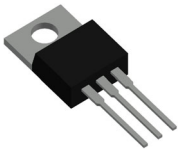
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REVISION HISTORY

Revision	Description of Changes	Date
13	Rebranded the document to **onsemi** format.	4/1/2026

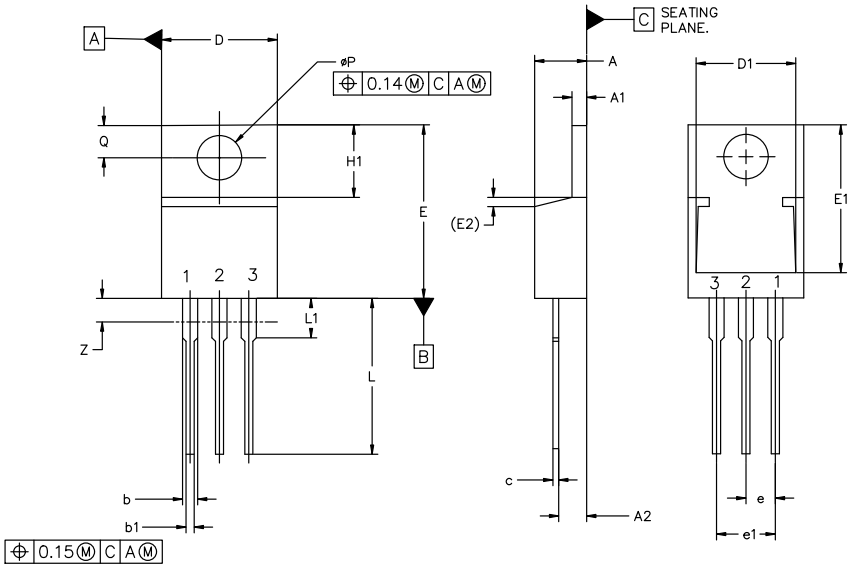
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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TO−220−3 10.10x15.12x4.45, 2.54P
CASE 221A
ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	−.−−	−.−−	3.48

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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