Octal 3-State Noninverting Bus Transceiver with LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

MC74HCT245A

The MC74HCT245A is identical in pinout to the LS245. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The MC74HCT245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

Features

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 V to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 304 FETs or 76 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

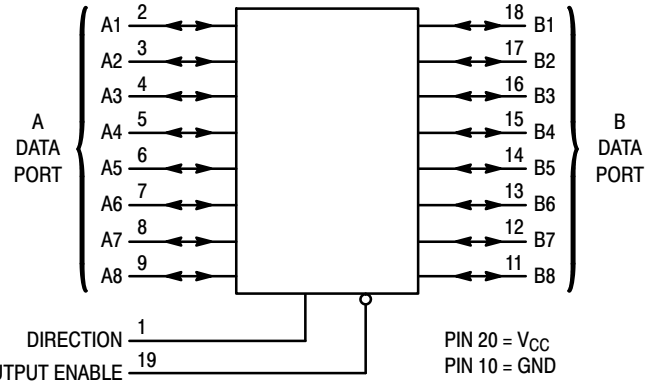
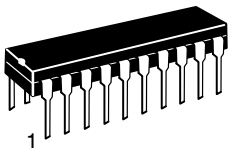


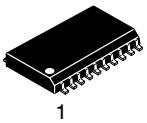
Figure 1. Logic Diagram

Design Criteria	Value	Unit
Internal Gate Count*	76	ea
Internal Gate Propagation Delay	1.0	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.005	pJ

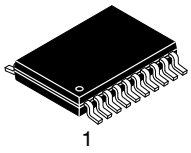
* Equivalent to a two-input NAND gate.



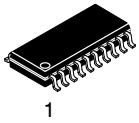
PDIP-20
N SUFFIX
CASE 738



SOIC-20W
DW SUFFIX
CASE 751D

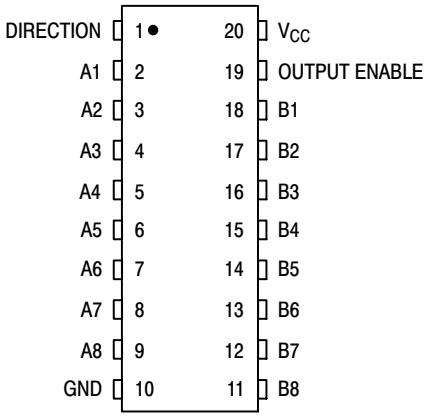


TSSOP-20
DT SUFFIX
CASE 948E



SOEIAJ-20
F SUFFIX
CASE 967

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering, shipping information, and marking information on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = Don't Care

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, PDIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Secs (PDIP, SOIC, SSOP or TSSOP Package)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

† Derating – Plastic DIP: – 10 mW/°C from 65 °C to 125 °C
SOIC Package: – 7 mW/°C from 65 °C to 125 °C
TSSOP Package: – 6.1 mW/°C from 65 °C to 125 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25 °C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\ \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$ mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND, Pins 1 or 19	5.5	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND, I/O Pins	5.5	±0.5	±5.0	±10	μA
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA		≥–55 °C	25 °C to 125 °C		mA
			5.5	2.9	2.4		

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		–55 to 25 °C	≤85 °C	≤125 °C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to B or B to A (Figures 2 and 4)	22	28	33	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 3 and 5)	30	36	42	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to A or 8 (Figures 3 and 5)	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time. any Output (Figures 2 and 4)	12	15	18	ns
C_{in}	Maximum Input Capacitance (Pin 1 or 19)	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance, (I/O in High-Impedance State)	15	15	15	pF

		Typical @ 25 °C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	97	pF

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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SWITCHING WAVEFORMS

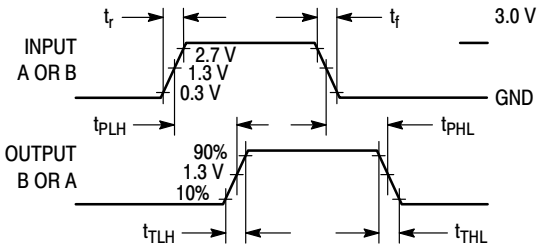


Figure 2.

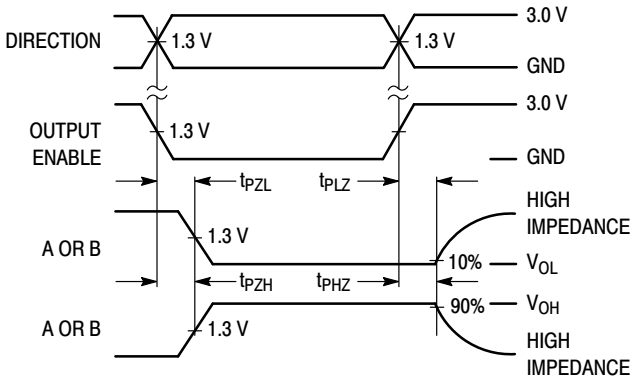
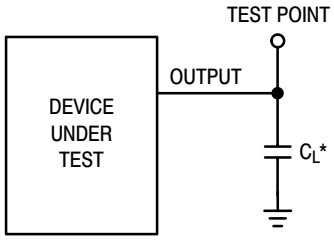
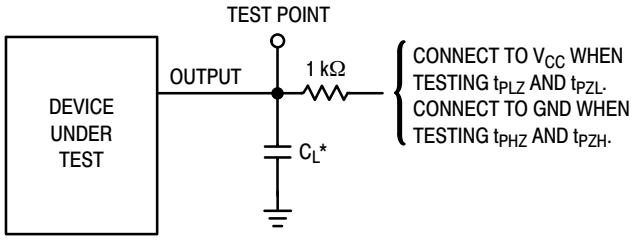


Figure 3.



* Includes all probe and jig capacitance

Figure 4.



* Includes all probe and jig capacitance

Figure 5. Test Circuit

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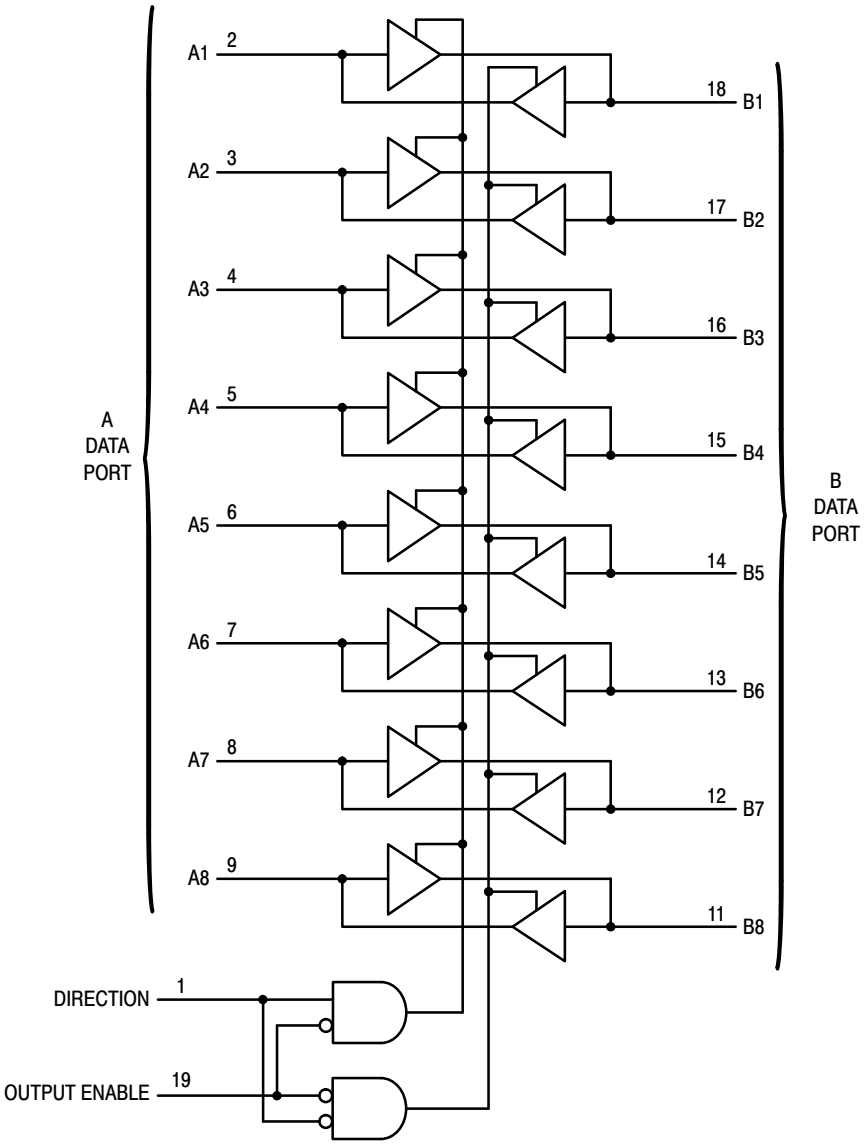


Figure 6. Expanded Logic Diagram

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ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT245ADWG	SOIC-20 (Pb-Free)	38 Units / Rail
MC74HCT245ADWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel
MC74HCT245ADTG	TSSOP-20*	75 Units / Rail
MC74HCT245ADTR2G	TSSOP-20*	2500 / Tape & Reel

DISCONTINUED (Note 1)

MC74HCT245ANG	PDIP-20 (Pb-Free)	18 Units / Rail
MC74HCT245AFELG	SOEIAJ-20 (Pb-Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* These packages are inherently Pb-Free.

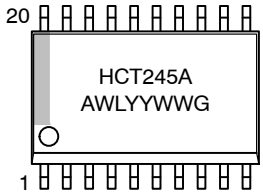
1. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

MARKING DIAGRAMS

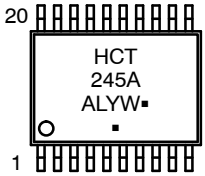
PDIP-20



SOIC-20W



TSSOP-20



SOEIAJ-20



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb-Free Package
(Note: Microdot may be in either location)

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REVISION HISTORY

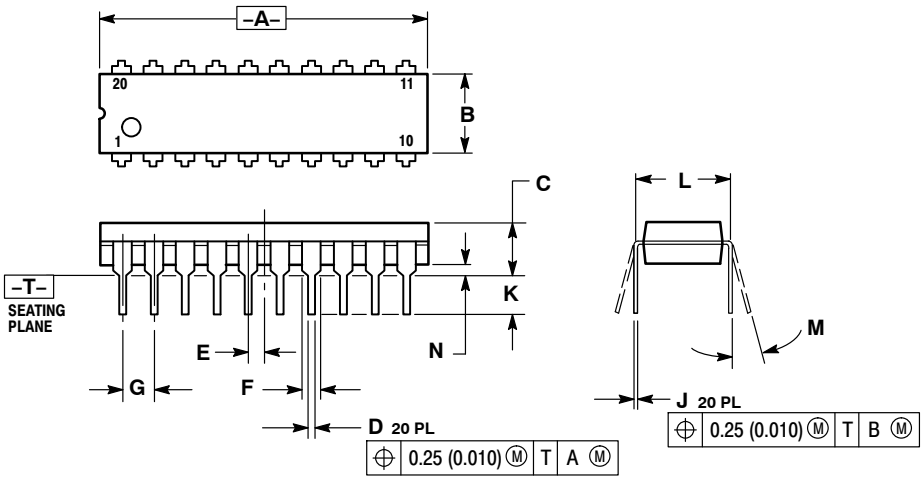
Revision	Description of Changes	Date
13	Rebranded the Data Sheet to **onsemi** format. MC74HCT245ANG, MC74HCT245AFELG OPNs Marked as Discontinued.	11/05/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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PACKAGE DIMENSIONS

PDIP−20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738−03
ISSUE E



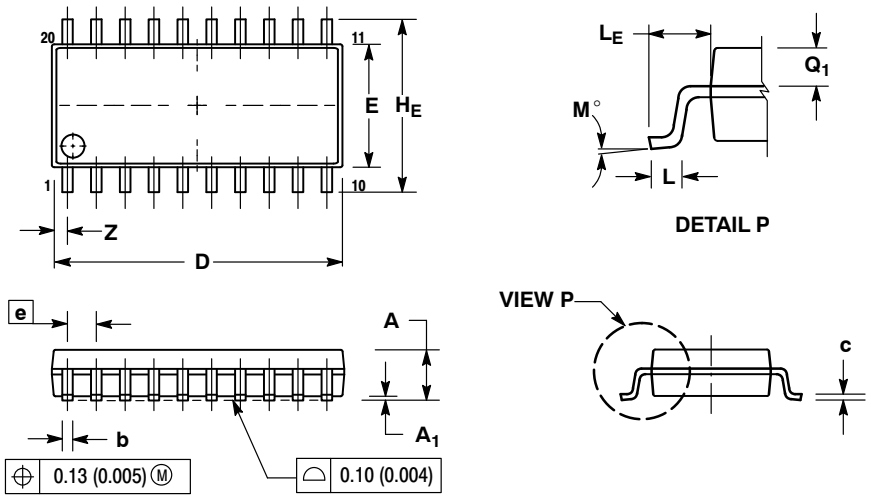
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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PACKAGE DIMENSIONS

SOEIAJ–20
F SUFFIX
CASE 967–01
ISSUE A



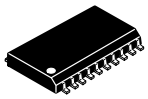
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

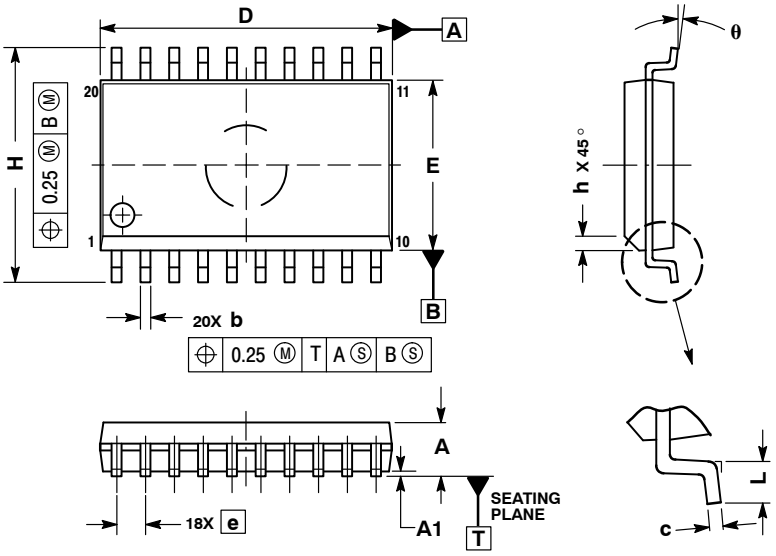
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SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



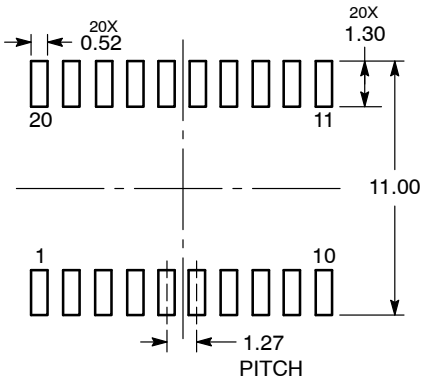
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

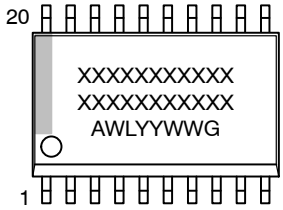
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

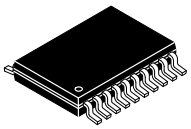
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−20 WB**		**PAGE 1 OF 1**

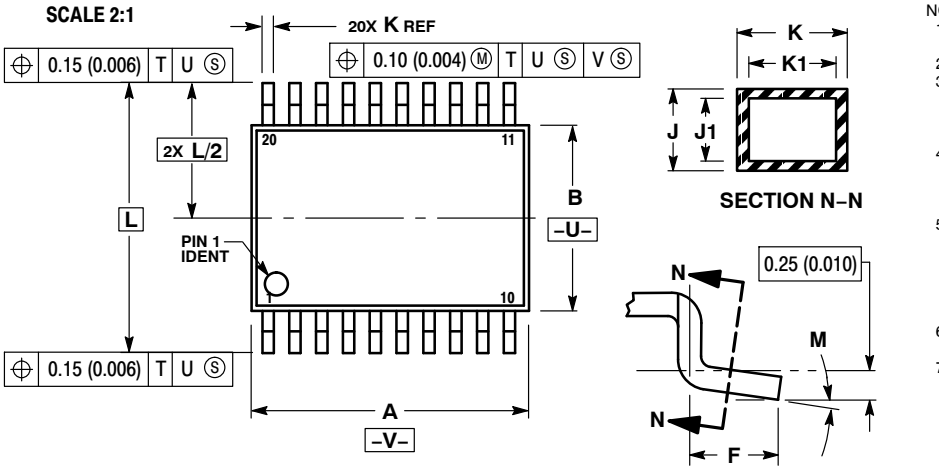
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TSSOP–20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

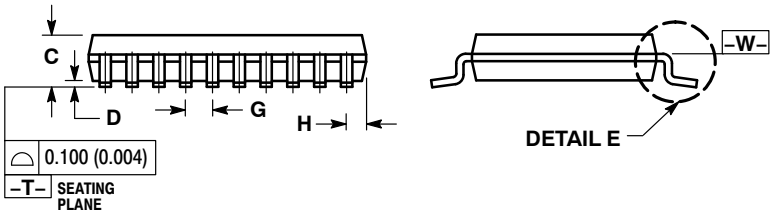


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SECTION N–N

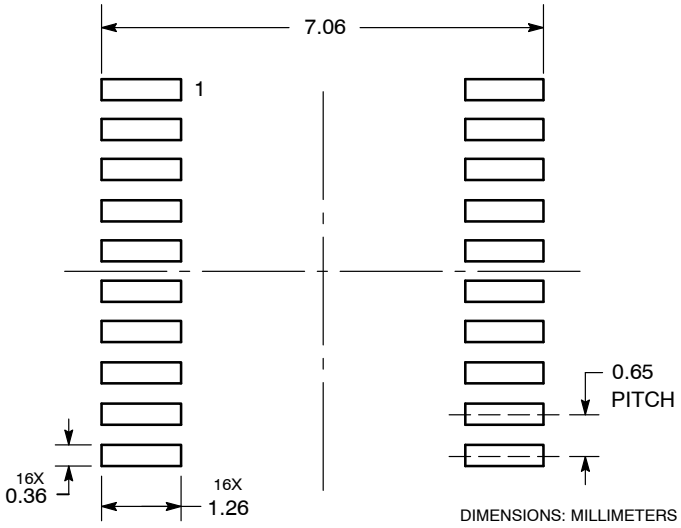
DETAIL E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

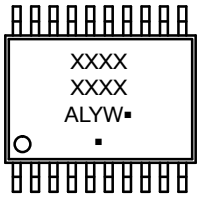
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP–20 WB**		**PAGE 1 OF 1**

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