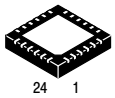
2.5 V/3.3 V ECL DUAL Differential 2:1 Multiplexer

NB100LVEP56



QFN24
MN SUFFIX
CASE 485L

Description

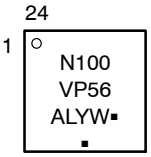
The NB100LVEP56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or differential data signals. The device features both individual and common select inputs to address both data path and random logic applications. Common and individual selects can accept both LVECL and LVCMOS input voltage levels. Multiple V_{BB} pins are provided.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input operation, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

- Maximum Input Clock Frequency > 2.5 GHz Typical
- Maximum Input Data Rate > 2.5 Gb/s Typical
- 525 ps Typical Propagation Delays
- Low Profile QFN Package
- PECL Mode Operating Range:
  V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = −2.375 V to −3.8 V
- Separate, Common Select, and Individual Select
  (Compatible with ECL and CMOS Input Voltage Levels)
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- Multiple V_{BB} Outputs
- These Devices are Pb-Free and are RoHS Compliant

MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

* For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NB100LVEP56MNG	QFN24 (Pb-Free)	92 Units / Tube

DISCONTINUED (Note 1)

NB100LVEP56MNR2G	QFN24 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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Table 1. PIN FUNCTION DESCRIPTION

Pin No. QFN	Name	I/O	Default State	Description
3,9,18,19, 20	V_{CC}	–	–	Positive Supply Voltage. All VCC Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
15,24	V_{EE}	–	–	Negative Supply Voltage. All VEE Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
6,12	V_{BB0}, V_{BB1}	–	–	ECL Reference Voltage Output
4	D0a	ECL Input	Low	Noninverted Differential Data a Input to MUX 0. Internal 75 kΩ to V_{EE}.
5	$\overline{D0a}$	ECL Input	High	Inverted Differential Data a Input to MUX 0. Internal 75 kΩ to V_{EE} and 37 kΩ to V_{CC}.
7	D0b	ECL Input	Low	Noninverted Differential Data b Input to MUX 0. Internal 75 kΩ to V_{EE}.
8	$\overline{D0b}$	ECL Input	High	Inverted Differential Data b Input to MUX 0. Internal 75 kΩ to V_{EE} and 37 kΩ to V_{CC}.
10	D1a	ECL Input	Low	Noninverted Differential Data a Input to MUX 1. Internal 75 kΩ to V_{EE}.
11	$\overline{D1a}$	ECL Input	High	Inverted Differential Data a Input to MUX 1. Internal 75 kΩ to V_{EE} and 37 kΩ to V_{CC}.
13	D1b	ECL Input	Low	Noninverted Differential Data b Input to MUX 1. Internal 75 kΩ to V_{EE}.
14	$\overline{D1b}$	ECL Input	High	Inverted Differential Data b Input to MUX 1. Internal 75 kΩ to V_{EE} and 37 kΩ to V_{CC}.
2	Q0	ECL Output	–	Noninverted Differential Output MUX 0. Typically Terminated with 50 Ω to V_{TT} = V_{CC} – 2.0 V.
1	$\overline{Q0}$	ECL Output	–	Inverted Differential Output MUX 0. Typically Terminated with 50 Ω to V_{TT} = V_{CC} – 2.0 V.
17	Q1	ECL Output	–	Noninverted Differential Output MUX 1. Typically Terminated with 50 Ω to V_{TT} = V_{CC} – 2.0 V.
16	$\overline{Q1}$	ECL Output	–	Inverted Differential Output MUX 1. Typically Terminated with 50 Ω to V_{TT} = V_{CC} – 2.0 V.
23	SEL0	ECL, CMOS Input	Low	Noninverted Differential Select Input to MUX 0. Internal 75 kΩ to V_{EE}.
22	COM_SEL	ECL, CMOS Input	Low	Noninverted Differential Common Select Input to Both MUX. Internal 75 kΩ to V_{EE}.
21	SEL1	ECL, CMOS Input	Low	Noninverted Differential Select Input to MUX 1. Internal 75 kΩ to V_{EE}.
–	EP	–		Exposed Pad. The exposed pad (EP) on the package bottom must be attached to a heat-sinking conduit. The exposed pad may only be electrically connected to V_{EE}.

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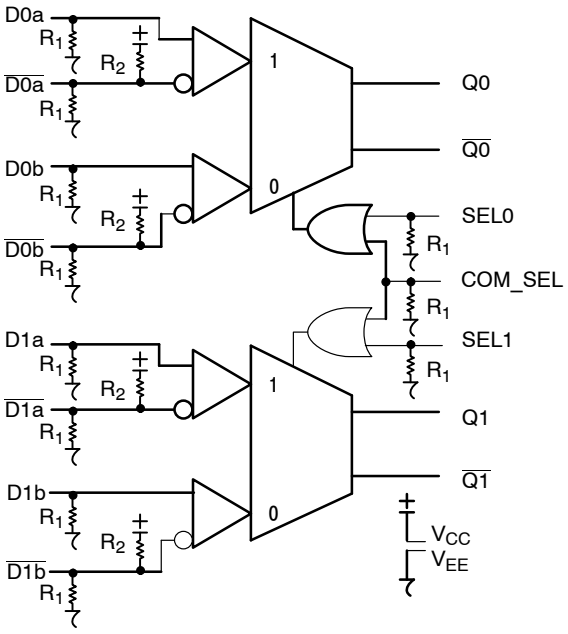

Figure 1. Logic Diagram

Table 2. TRUTH TABLE

SEL0	SEL1	COM_SEL	Q0, $\overline{Q0}$	Q1, $\overline{Q1}$
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

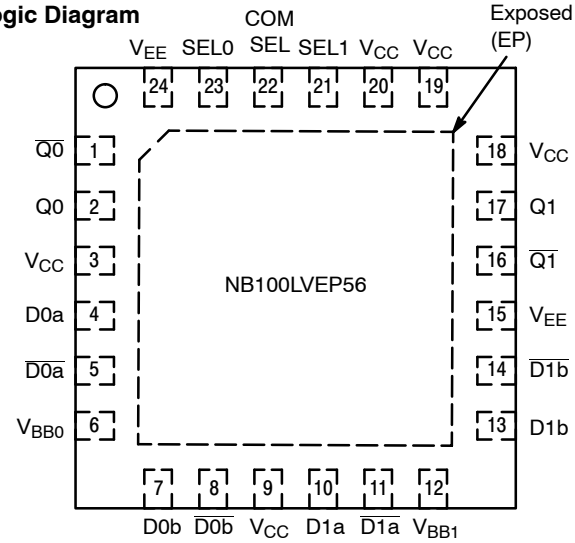

Figure 2. QFN-24 Lead Pinout (Top View)

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (R1)	75 kΩ
Internal Input Pullup Resistor (R2)	37 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 150 V > 2 kV
Moisture Sensitivity (Note 1) QFN-24	Pb-Free Pkg Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	354 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	Negative Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	Positive Mode Input Voltage Negative Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) JEDEC 51-6 (2S2P-Multi Layer Test Board) with Filled Thermal Vias	0 lfpm 500 lfpm	QFN-24 QFN-24	37 32	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	QFN-24	11	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. DC CHARACTERISTICS, PECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 2)

		−40 °C			25 °C			85 °C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Negative Power Supply Current	35	45	55	35	45	55	35	48	58	mA
V_{OH}	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 3)	555	775	900	555	775	900	555	775	900	mV
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs) (Note 4)	1335 1335		V_{CC} 1620	1335 1335		V_{CC} 1620	1275 1275		V_{CC} 1620	mV
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs) (Note 4)	V_{EE} 555		875 875	V_{EE} 555		875 875	V_{EE} 555		875 875	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current (@V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@V_{IL}) D $\overline{D}$ SEL	0.5 −150 −150			0.5 −150 −150			0.5 −150 −150			μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.125 V to +1.3 V.
3. All loading with 50 Ω to V_{CC} − 2.0 V.
4. Do not use V_{BB} at V_{CC} < 3.0 V.
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 6. DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 6)

Symbol	Characteristic	−40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	35	45	55	35	45	55	35	48	58	mA
V_{OH}	Output HIGH Voltage (Note 7)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 7)	1355	1575	1700	1355	1575	1700	1355	1575	1700	mV
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs)	2135 2135		V_{CC} 2420	2135 2135		V_{CC} 2420	2135 2135		V_{CC} 2420	mV
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs)	V_{EE} 1355		1675 1675	V_{EE} 1355		1675 1675	V_{EE} 1355		1675 1675	mV
V_{BB}	Output Reference Voltage (Note 8)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current (@V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@V_{IL}) D $\overline{D}$ SEL	0.5 −150 −150			0.5 −150 −150			0.5 −150 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.5 V to −0.3 V.
7. All loading with 50 Ω to V_{CC} − 2.0 V.
8. Single-Ended input operation is limited to $V_{CC} \geq$ 3.0 V in PECL mode.
9. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −3.8 V to −2.375 V (Note 10)

Symbol	Characteristic	−40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	35	45	55	35	45	55	35	48	58	mA
V_{OH}	Output HIGH Voltage (Note 11)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 11)	−1945	−1725	−1600	−1945	−1725	−1600	−1945	−1725	−1600	mV
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs)	−1165 −1165		V_{CC} −880	−1165 −1165		V_{CC} −880	−1165 −1165		V_{CC} −880	mV
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs)	V_{EE} −1945		−1600 −1600	V_{EE} −1945		−1600 −1600	V_{EE} −1945		−1600 −1600	mV
V_{BB}	Output Reference Voltage (Note 12)	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
I_{IH}	Input HIGH Current (@V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@V_{IL}) D $\overline{D}$ SEL	0.5 −150 −150			0.5 −150 −150			0.5 −150 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

10. Input and output parameters vary 1:1 with V_{CC}.
11. All loading with 50 Ω to V_{CC} − 2.0 V.
12. Single-Ended input operation is limited to V_{EE} from −3.0 V to −5.5 V in NECL mode.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 8. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −2.375 V to −3.8 V or V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V (Note 14)

Symbol	Characteristic	−40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (f_{in} ≤ 1 GHz) (See Figure 3) (f_{in} = 2 GHz) (f_{in} = 2.5 GHz)	525 500 400	700 600 500		550 500 350	700 600 450		500 400 200	700 500 300		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D to Q, $\overline{Q}$ SEL to Q, $\overline{Q}$ COM_SEL to Q, $\overline{Q}$	 375 575 550	 500 775 750	 625 975 950	 400 625 600	 525 825 800	 650 1025 1000	 450 700 700	 575 900 900	 700 1100 1100	ps
t_{Skew}	Pulse Skew (Note 15) Within Device Input Skew (Note 16) Within Device Output Skew (Note 17) Device-to-Device Skew (Note 18)		10 5 15 50	50 30 50 200		10 5 15 50			10 5 15 50	50 30 50 200	ps
t_{JITTER}	RMS Random Clock Jitter (Note 19) @ ≤1.0 GHz @ ≤1.5 GHz @ ≤2.0 GHz @ ≤2.5 GHz Peak-to-Peak Data Dependent Jitter (Note 20) @ 0.5 GHz @ 1.25 GHz @ 2.488 GHz	 	 0.269 0.306 0.250 0.339 4.1 32.2 30.8	 0.4 0.4 0.4 0.8 16 80 66	 	 0.307 0.303 0.305 0.895 4.6 22.6 27.2	 0.4 0.4 0.5 2.0 15 63 56	 	 0.371 0.391 0.722 2.443 4.4 22 24.4	 0.5 0.6 1.2 7.7 16 53 54	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 21)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times @ 50 MHz Q, $\overline{Q}$ (20% − 80%)	60	110	150	60	120	170	90	140	230	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V. Input edge rates 150 ps (20% − 80%).
15. Pulse Skew $|t_{PLH} - t_{PHL}|$
16. Worst case difference between D0a and D0b (or between D1a or D1b), when both output come from same input.
17. Worst case difference between Q0 and Q1 outputs.
18. Skew is measured between outputs under identical transitions.
19. Additive RMS jitter with 50% Duty Cycle Clock Signal.
20. Additive Peak-to-Peak jitter with input NRZ data at PRBS 2^{31}-1.
21. Input voltage swing is a single-ended measurement operating in differential mode.

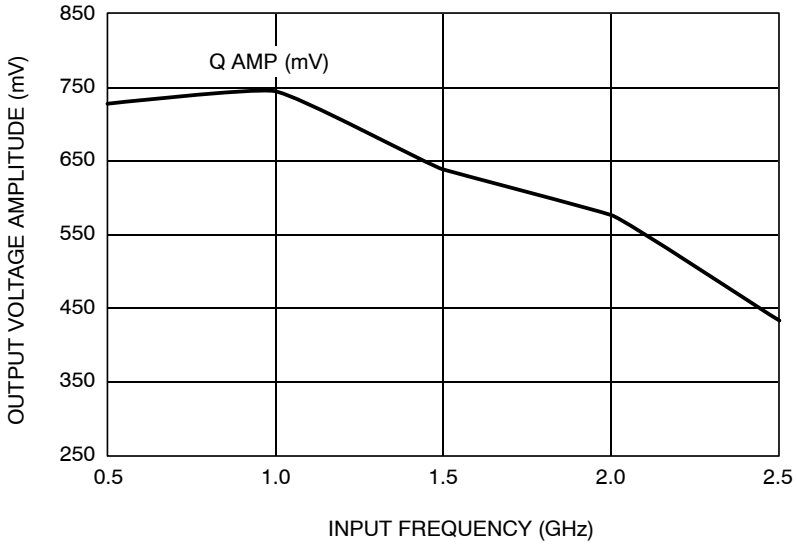

Figure 3. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at V_{CC} = 2.5 V, 25°C

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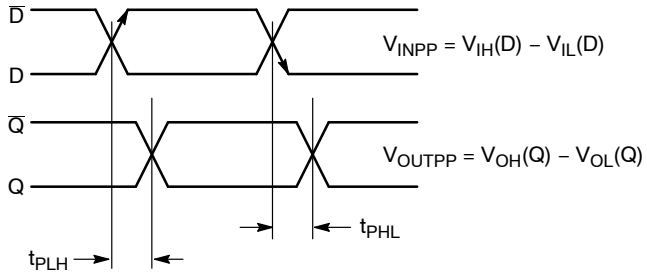

Figure 4. AC Reference Measurement

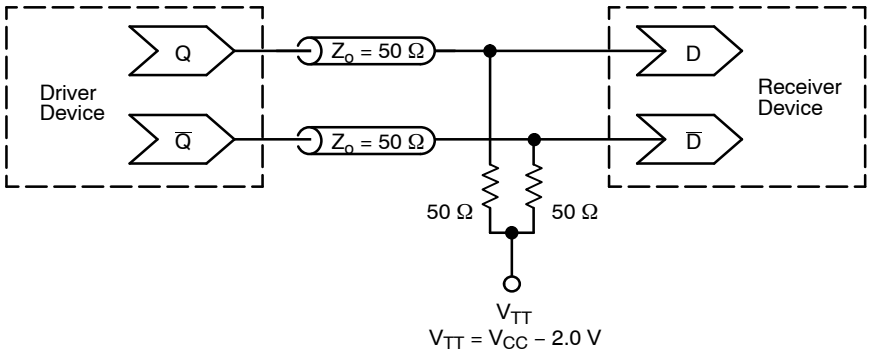

Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

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Resource Reference of Application Notes

AN1405/D	–	ECL Clock Distribution Techniques
AN1406/D	–	Designing with PECL (ECL at +5.0 V)
AN1503/D	–	ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D	–	Metastability and the ECLinPS Family
AN1568/D	–	Interfacing Between LVDS and ECL
AN1672/D	–	The ECL Translator Guide
AND8001/D	–	Odd Number Counters Design
AND8002/D	–	Marking and Date Codes
AND8020/D	–	Termination of ECL Logic Devices
AND8066/D	–	Interfacing with ECLinPS
AND8090/D	–	AC Characteristics of ECL Devices

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REVISION HISTORY

Revision	Description of Changes	Date
13	Rebranded the Data Sheet to **onsemi** format. NB100LVEP56MNR2G OPN Marked as Discontinued.	1/27/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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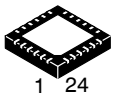
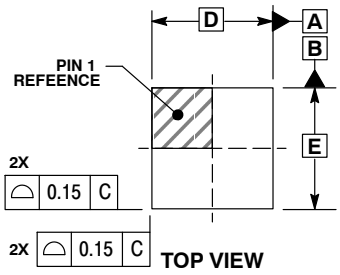
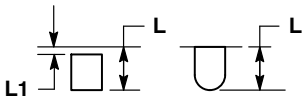
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

DATE 05 JUN 2012

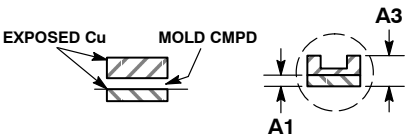


SCALE 2:1

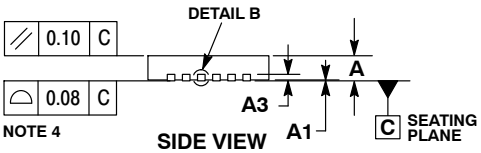


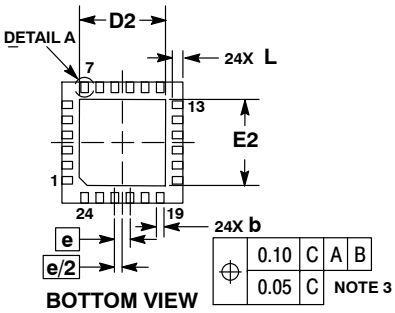


DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE TERMINAL CONSTRUCTIONS

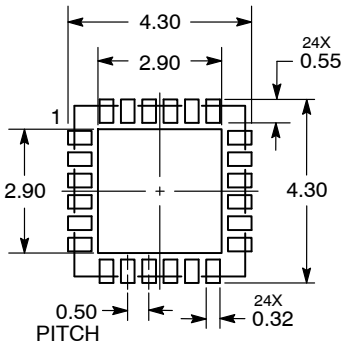




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.30	0.50
L1	0.05	0.15

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN24, 4X4, 0.5P**		**PAGE 1 OF 1**

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