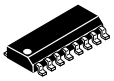
PWM Buck Controller, Synchronous, 100V

NCP1034



SOIC−16
D SUFFIX
CASE 751B

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

Description

The NCP1034 is a high voltage PWM controller designed for high performance synchronous Buck DC/DC applications with input voltages up to 100 V. The NCP1034 drives a pair of external N−MOSFETs. The switching frequency is programmable from 25 kHz up to 500 kHz allowing the flexibility to tune for efficiency and size. A synchronization feature allows the switching frequency to be set by an external source or output a synchronization signal to multiple NCP1034 controllers. The output voltage can be precisely regulated using the internally trimmed 1.25 V reference voltage for low voltage applications. Protection features include user programmable undervoltage lockout and hiccup current limit.

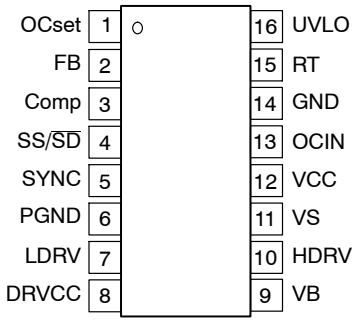
Features

- High Voltage Operating up to 100 V
- Programmable Switching Frequency up to 500 kHz
- 2 A Output Drive Capability
- Precision Reference Voltage (1.25 V)
- Programmable Soft−Start with Prebiased Load Capability
- Programmable Overcurrent Protection
- Programmable Undervoltage Protection
- Hiccup Current Limit Using MOSFET $R_{DS(on)}$ Sensing
- External Frequency Synchronization
- 16 Pin SOIC Package
- This is a Pb−Free Device

Applications

- 48 V Non−Isolated DC−DC Converter
- Embedded Telecom Systems
- Networking and Computing Voltage Regulator
- Distributed Point of Load Power Architectures
- General High Voltage DC−DC Converters

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 24 of this data sheet.

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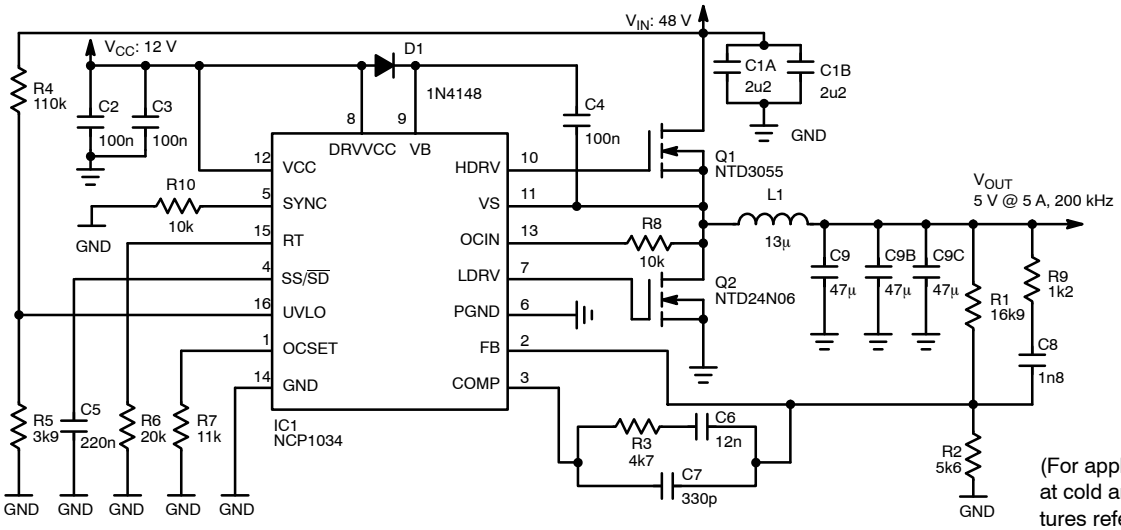

(For applications operating at cold ambient temperatures refer to the soft−start section on Page 15)

Figure 1. Typical Application Circuit

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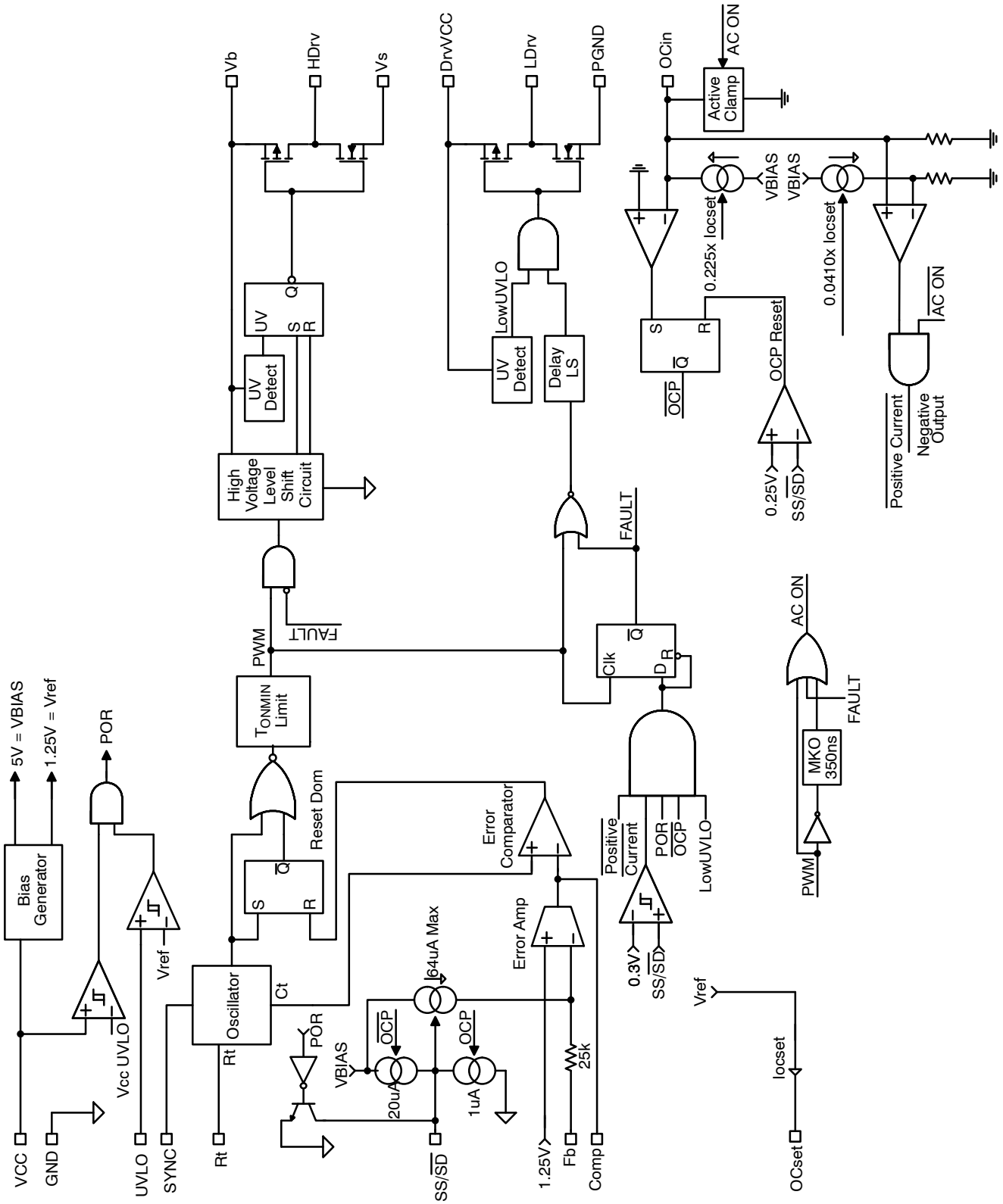

Figure 2. Internal Block Diagram

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PIN FUNCTION DESCRIPTION

PIN	PIN NAME	DESCRIPTION
1	OC_{set}	Current limit set point. A resistor from this pin to GND will set the positive and negative current limit threshold
2	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
3	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
4	SS/$\overline{SD}$	Soft−Start / Shutdown. This pin provides user programmable soft−start function. External capacitor connected from this pin to ground sets the startup time of the output voltage. The converter can be shutdown by pulling this pin below 0.3 V.
5	SYNC	The internal oscillator can be synchronized to an external clock via this pin and other IC's can be synchronized via this pin to internal oscillator. If it is not used this pin should be connected via 10 kΩ resistor to ground.
6	P_{GND}	Power Ground. This pin serves as a separate ground for the MOSFET driver and should be connected to the system's power ground plane.
7	LDRV	Output driver for low side MOSFET.
8	$DRVV_{CC}$	This pin provides biasing for the internal low side driver. A minimum of 0.1 μF, high frequency capacitor must be connected from this pin to power ground.
9	VB	This pin powers the high side driver and must be connected to a voltage higher than input voltage. A minimum of 0.1 μF, high frequency capacitor must be connected from this pin to switch node.
10	HDRV	Output driver for high side MOSFET
11	V_S	Switch Node. This pin is connected to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is return path for the upper gate driver.
12	V_{CC}	This pin provides power for the internal blocks of the IC. A minimum of 0.1 μF, high frequency capacitor must be connected from this pin to ground.
13	OC_{IN}	Overcurrent sensing input. A serial resistor from this pin to drain of low MOSFET must be used to limit the current into this pin.
14	GND	Signal ground for internal reference and control circuitry.
15	R_T	Connecting a resistor from this pin to ground sets the oscillator frequency.
16	UVLO	An external voltage divider is used to set the undervoltage threshold levels.

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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
FB, V_{UVLO}, R_T, OC_{set}		−0.3	10	V
COMP, SS/SD, SYNC, OC_{IN}		−0.3	6	V
LDRV		−0.3	V_{CC} + 0.3	V
$DRVV_{CC}$, V_{CC}		−0.3	20	V
VB		V_S	V_S + 20	V
HDRV		V_S − 0.3	V_B + 0.3	V
V_S		−1.0	150	V
OC_{in} Input Current			20	mA

All voltages referenced to GND

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	130	°C/W
Operating Ambient Temperature Range	T_A	−40 to 125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Junction Operating Temperature	T_J	−40 to 150	°C
ESD Withstand Voltage (Note 1) Human Body Model Machine Model	V_{ESD}	 2000 200	 V V
Latchup Capability per Jedec JESD78			

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Excluding pins V_b, V_S and H_{DRV}.

TYPICAL ELECTRICAL PARAMETERS

RECOMMENDED OPERATING CONDITIONS

Symbol	Definition	Min	Max	Unit
V_{IN}	Converting Voltage		100	V
V_{CC}	Supply Voltage	10	18	V
DRV_{CC}	Supply Voltage	10	18	V
V_B to V_S	Supply Voltage	10	18	V
F_{SW}	Operating Frequency	25	500	kHz
T_J	Junction Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, these specifications apply over V_{CC} = 12 V, $DRVV_{CC}$ = V_B = 12 V, −40°C < TJ < 125°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REFERENCE VOLTAGE						
Feedback Voltage	V_{FB}			1.25		V
Accuracy		−40°C < T_J < 125°C	−1.5		+1.5	%
FB Voltage Line Regulation	L_{REG}	10 V < V_{CC} < 18 V (Note 3)			2.0	mV
SUPPLY CURRENT						
V_{CC} Supply Current (Stat)	$I_{CC(Static)}$	S_S = 0 V, No Switching, R_T = 10 kΩ, R_{OCSET} = 10 kΩ		2.0	3.0	mA
$DRVV_{CC}$ Supply Current (Stat)	$I_{C(Static)}$	S_S = 0 V, No Switching		0.1	0.3	mA
V_B Supply Current (Stat)	$I_{B(Static)}$	S_S = 0 V, No Switching		0.1	0.3	mA
UNDERVOLTAGE LOCKOUT						
V_{CC}−Start−Threshold	V_{CC_UVLO} (R)	Supply Ramping Up	7.9	8.9	9.8	V
V_{CC}−Stop−Threshold	V_{CC_UVLO} (F)	Supply Ramping Down	7.3	8.2	9.0	V
V_{CC}−Hysteresis		Supply Ramping Up and Down		0.7		V
DRV_{CC}−Start−Threshold	DRV_{CC_UVLO} (R)	Supply Ramping Up	7.9	8.9	9.8	V
DRV_{CC}−Stop−Threshold	DRV_{CC_UVLO} (F)	Supply Ramping Down	7.3	8.2	9.0	V
DRV_{CC}−Hysteresis		Supply Ramping Up and Down		0.7		V
V_B−Start−Threshold	V_{B_UVLO} (R)	Supply Ramping Up	7.9	8.9	9.8	V
V_B−Stop−Threshold	V_{B_UVLO} (F)	Supply Ramping Down	7.3	8.2	9.0	V
V_B−Hysteresis		Supply Ramping Up and Down		0.7		V
Undervoltage Threshold Value	U_{UVLO} (Rising)		1.19	1.25	1.31	V
Undervoltage Threshold Value	U_{UVLO} (Falling)		1.10	1.15	1.20	V
OSCILLATOR						
Frequency	F_S	R_T = 20 kΩ R_T = 10 kΩ	170 320	200 375	230 430	kHz
Ramp Amplitude	V_{ramp}	(Note 3)		2.0		V
Min Duty Cycle	D_{min}	FB = 2 V			0	%
Min Pulse Width	$D_{min(ctrl)}$	F_S = 200 kHz, (Note 3)			200	ns
Max Duty Cycle	D_{max}	F_S = 400 kHz, FB = 1.2 V	80			%
SYNC Frequency Range	SYNC(F_S)	20% Above Free Running Frequency			500	kHz
SYNC Pulse Duration	$SYNC_{(pulse)}$		200			ns
SYNC High Level	$SYNC_{(H)}$		2.0			V
SYNC Low Level	$SYNC_{(L)}$				0.8	V
SYNC Input Threshold	$SYNC_{(Thre)}$			1.6		V
SYNC Input Hysteresis	$SYNC_{(Hyst)}$		300			mV
SYNC Input Impedance	$SYNC_{(ZIN)}$	(Note 3)		16		kΩ
SYNC Output Impedance	$SYNC_{(OUT)}$	(Note 3)		2.5		kΩ
SYNC Output Pulse Width	$SYNC_{(Pulse\ Width)}$	F_S = 500 kHz, (Note 3)		300		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.
3. Guaranteed by design but not tested in production.

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, these specifications apply over V_{CC} = 12 V, $DRVV_{CC}$ = V_B = 12 V, −40°C < TJ < 125°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ERROR AMPLIFIER						
Input Bias Current	I_{FB}	S_S = 3 V, FB = 1 V		−0.1	−0.4	μA
Source/Sink Current	$I_{(Source/Sink)}$		50	100	120	μA
Bandwidth		(Note 3)	4.0	10		MHz
DC gain		(Note 3)		55		dB
Transconductance	g_m	(Note 3)	1500	3150	4000	μmho
SOFT−START/SD						
Soft−Start Current	I_{SS}	S_S = 0 V	15	20	25	μA
Shutdown Output Threshold	S_D			0.3	0.4	V
OVERCURRENT PROTECTION						
OCSET Voltage	V_{OCSET}			1.25		V
Hiccup Current	I_{Hiccup}	(Note 3)		1.0		μA
Hiccup Duty Cycle	$Hiccup_{(duty)}$	I_{Hiccup}/I_{SS}, (Note 3)			5.0	%
OUTPUT DRIVERS						
LO, Drive Rise Time	t_r(Lo)	C_L = 1.5 nF (See Figure 3)		17		ns
HI Drive Rise Time	t_r(Hi)	C_L = 1.5 nF (See Figure 3)		17		ns
LO Drive Fall Time	t_f(Lo)	C_L = 1.5 nF (See Figure 3)		10		ns
HI Drive Fall Time	t_f(Hi)	C_L = 1.5 nF (See Figure 3)		10		ns
Dead Band Time	t_{dead}	(See Figure 3)	30	60	120	ns
LO Output High Short Circuit Pulsed Current	$t_{LDRVhigh}$	V_{LDRV} = 0 V, $P_W \leq$ 10 μs, T_J = 25°C (Note 3)		1.4		A
HI Output High Short Circuit Pulsed Current	$t_{HDRVhigh}$	V_{HDRV} = 0 V, $P_W \leq$ 10 μs, T_J = 25°C (Note 3)		2.2		A
LO Output Low Short Circuit Pulsed Current	$t_{LDRVhigh}$	V_{LDRV} = $DRVV_{CC}$, $P_W \leq$ 10 μs, T_J = 25°C (Note 3)		1.4		A
HI Output Low Short Circuit Pulsed Current	$t_{HDRVhigh}$	V_{HDRV} = V_B, $P_W \leq$ 10 μs, T_J = 25°C (Note 3)		2.2		A
LO Output Resistor, Source	R_{LOH}	Typical Value @ 25°C, (Note 3)		7	12	Ω
LO Output Resistor, Sink	R_{LOL}	Typical Value @ 25°C, (Note 3)		2	8	Ω
HI Output Resistor, Source	R_{HIH}	Typical Value @ 25°C, (Note 3)		7	12	Ω
HI Output Resistor, Sink	R_{HIL}	Typical Value @ 25°C, (Note 3)		2	8	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.
3. Guaranteed by design but not tested in production.

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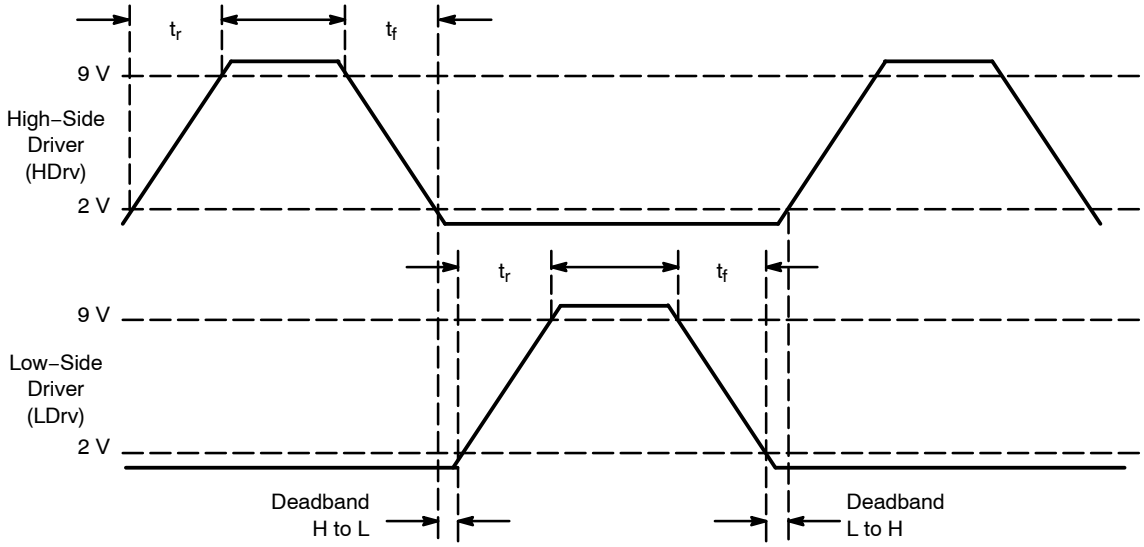

Figure 3. Definition of Rise−Fall Time and Deadband Time

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TYPICAL OPERATING CHARACTERISTICS

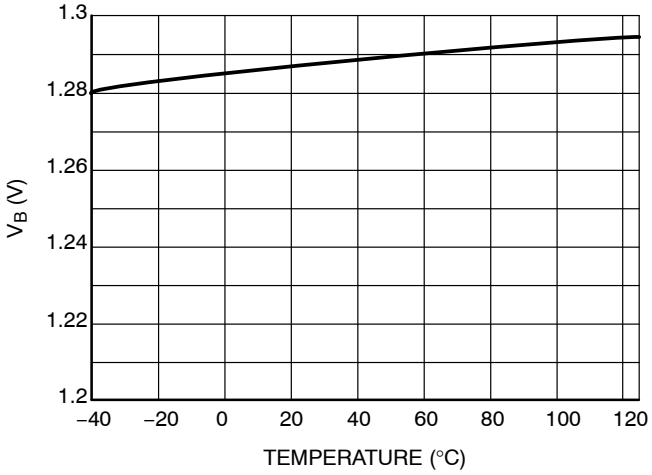

Figure 4. V_{FB}

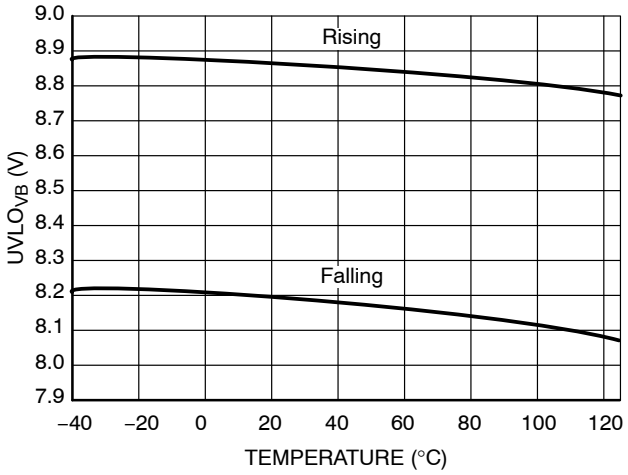

Figure 5. $UVLO_{VB}$

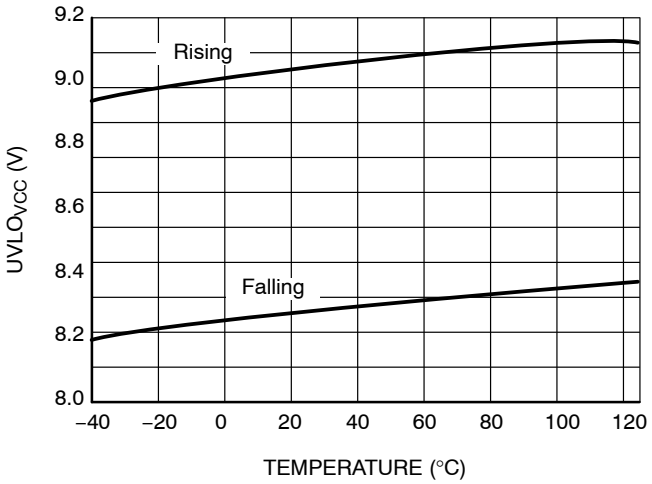

Figure 6. $UVLO_{VCC}$

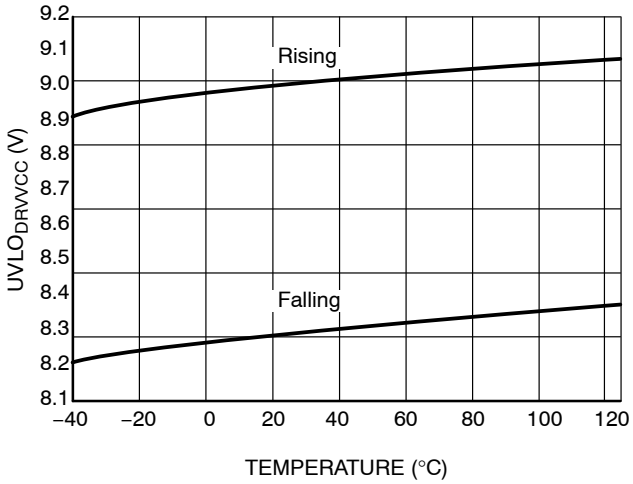

Figure 7. $UVLO_{DRVVCC}$

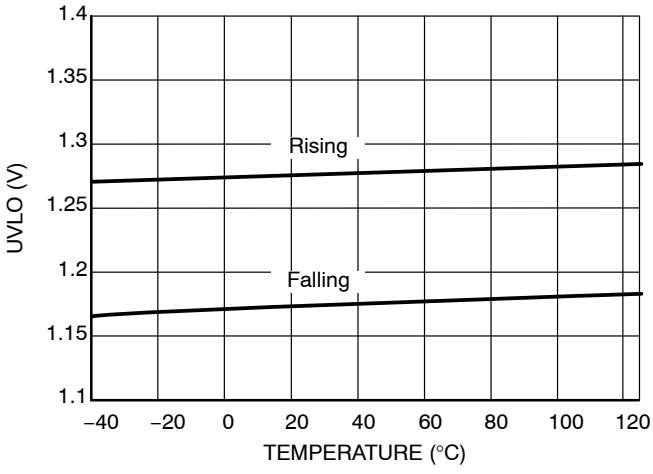

Figure 8. UVLO

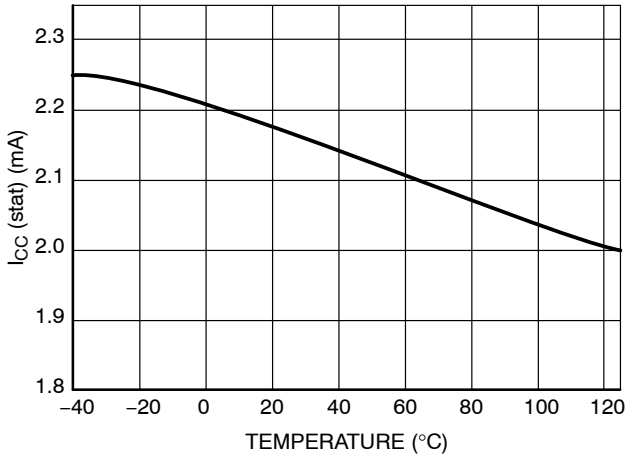

Figure 9. I_{CC} (Stat)

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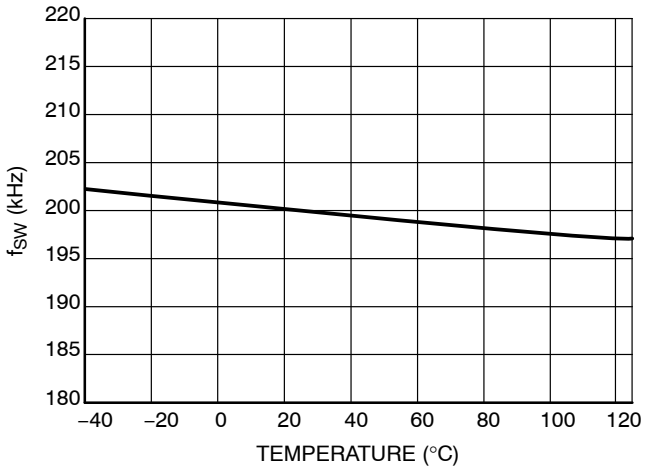

Figure 10. Switching Frequency @ R_T = 20 kΩ

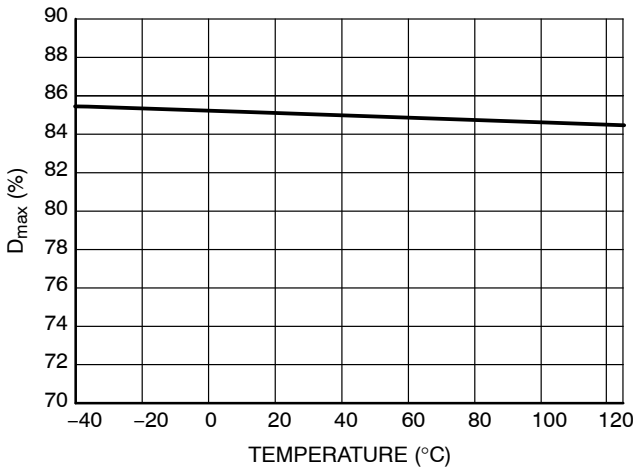

Figure 11. Maximum Duty Cycle @ f = 400 kHz

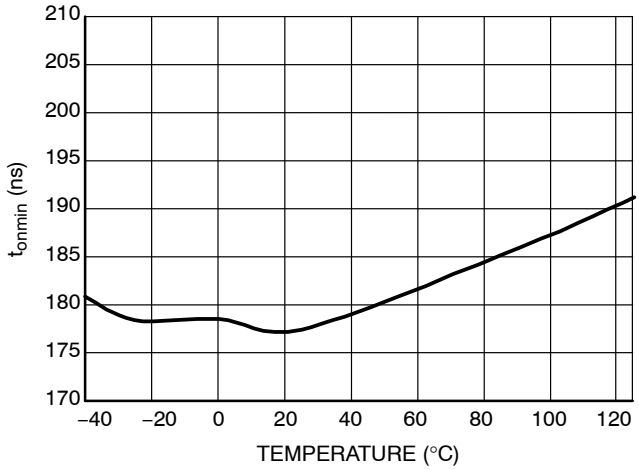

Figure 12. Minimum on Time

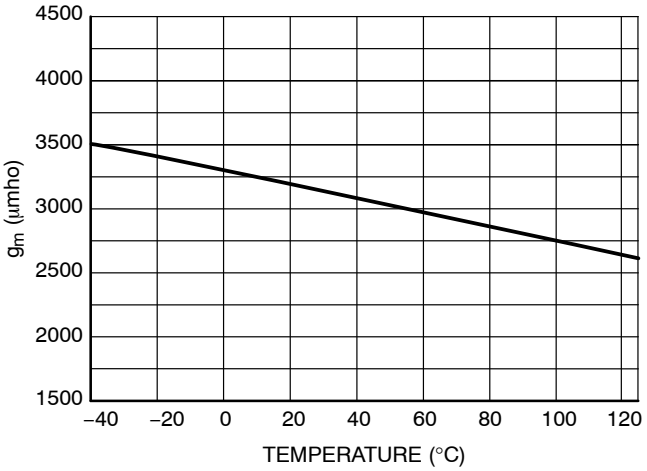

Figure 13. Error Amplifier Transconductance

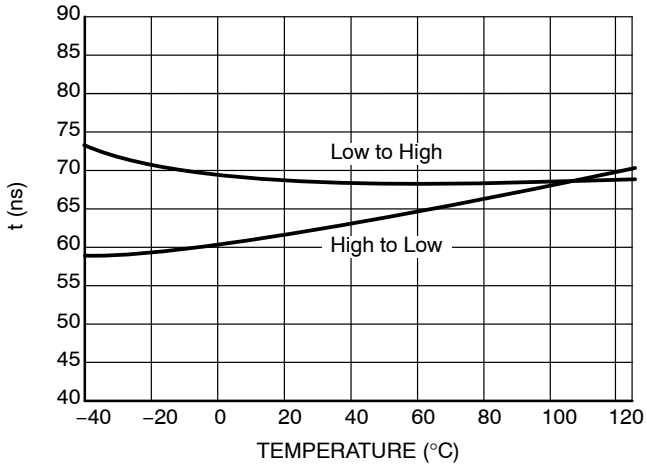

Figure 14. Deadtime

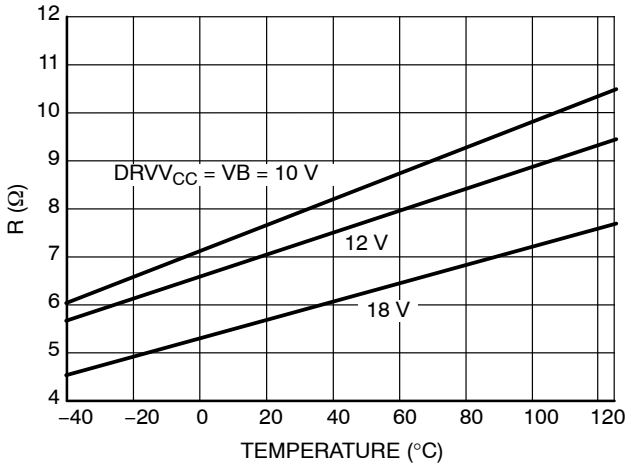

Figure 15. Driver Pullup Resistance

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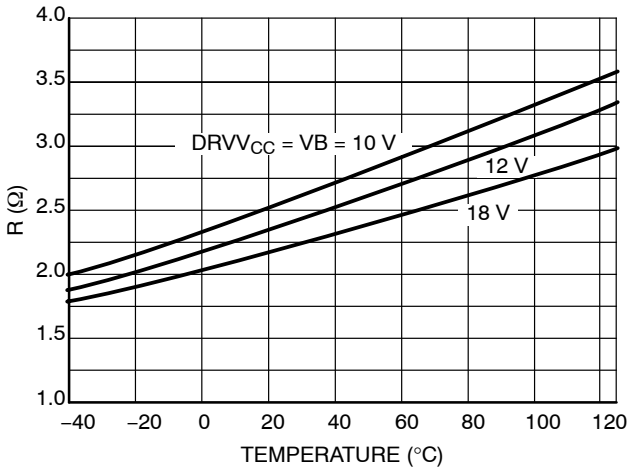

Figure 16. Driver Pulldown Resistance

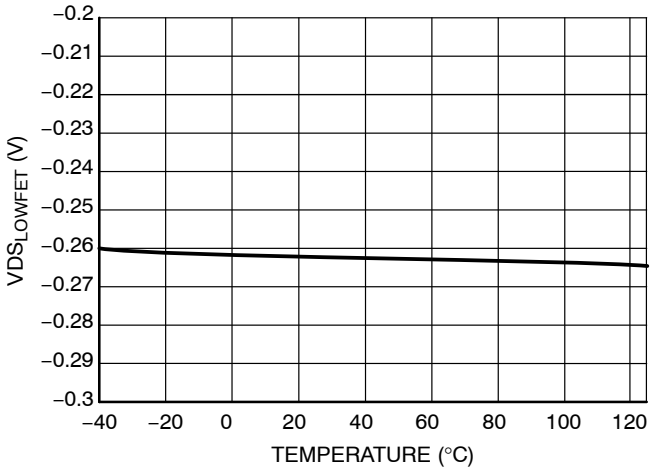

Figure 17. OCP @ R_8 = 10 kΩ, R_{OCIN} = 10 kΩ

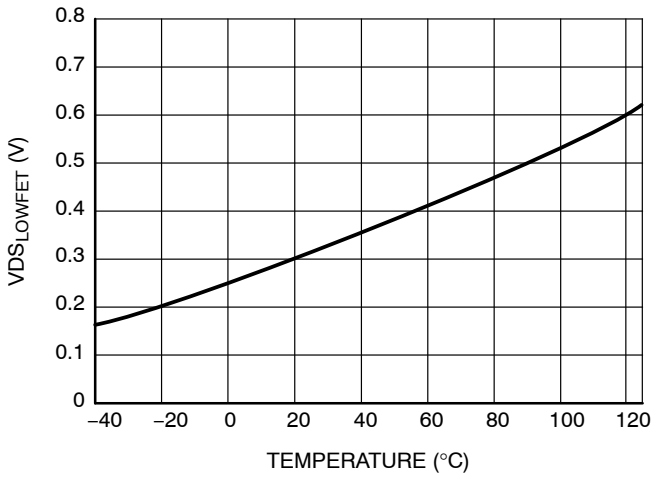

Figure 18. POSOCP @ R_8 = 10 kΩ, R_{OCIN} = 10 kΩ

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APPLICATION INFORMATION

Undervoltage Lock−out

There are four undervoltage lock−out circuits. Two of them protect external high−side and low−side drivers, the third ensures that the IC does not start until V_{CC} is under a set threshold. The last one can be programmed by the user. It has a rising threshold at 1.25 V and a falling threshold at 1.15 V, and the user can define the undervoltage level by an external resistor divider. If the voltage is not over the threshold value, the device stops operating. The high−side driver UVLO only stops switching the high−side MOSFET Programmed falling and rising UVLO voltage can be calculated by Equations 1 and 2:

$$V_{UVLO,falling} = 1.15 \cdot \left(1 + \frac{R4}{R5}\right) \quad \text{(eq. 1)}$$

and

$$V_{UVLO,rising} = 1.25 \cdot \left(1 + \frac{R4}{R5}\right) \quad \text{(eq. 2)}$$

Shutdown

The output voltage can be disabled by pulling the SS/$\overline{SD}$ pin below 0.3 V. A small transistor can be used to pull it down as shown in Figure 19. During this time, both external MOSFETs are turned off. After the SS/$\overline{SD}$ pin is released, the IC starts its operation with a soft−start sequence.

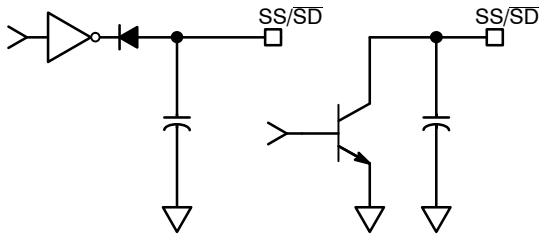

Figure 19. Shutdown Interface

Operating Frequency Selection

The operating frequency is set by an external resistor connected from the R_t Pin to ground. The value of this resistor can be selected from Figure 20, which shows switching frequency versus the timing resistor value.

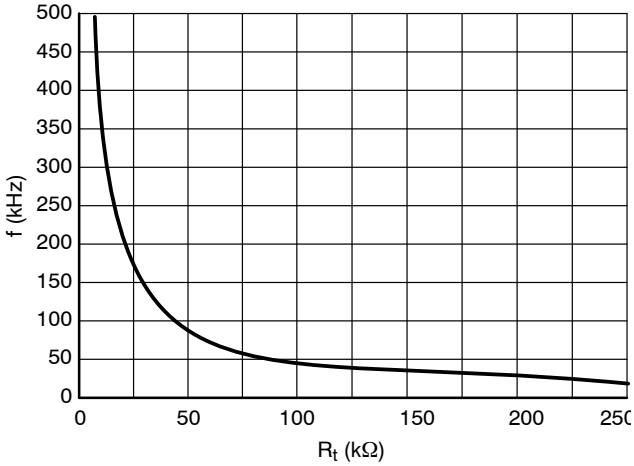

Figure 20. Frequency Dependence of R_t Value

Frequency Synchronization

The NCP1034 can be synchronized to an external clock signal. The input synchronization signal should be a TTL logic level. The oscillator is synchronized to the rising edge of the synchronizing signal. When synchronization is used, the free running frequency must be set by the timing resistor to a frequency at least 80% of the external synchronization frequency (Example: R_T = 20 kΩ / 200 kHz and external TTL = 220 kHz).

The NCP1034 can also output synchronization pulses on the SYNC pin. Pulses are generated when the internal oscillator ramp reaches the high threshold voltage. The frequency of these pulses is set by an external R_T resistor. Up to five NCP1034 controllers can be connected directly to the SYNC pin, all of which are synchronized to the controller with the highest frequency. The lowest frequency must be at least 80% of the highest one.

The equivalent internal circuit of the Sync pin is shown in Figure 21.

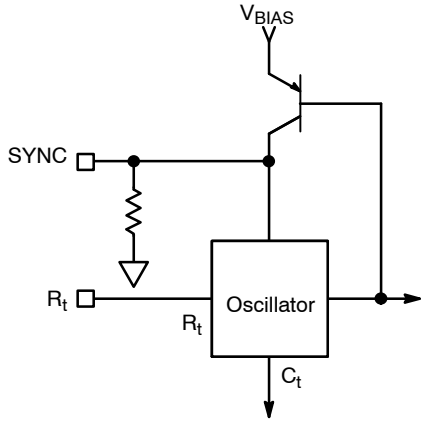

Figure 21. Equivalent Connection of the Sync Pin

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Figure 22 shows the part with no synchronization. In this circuit the internal clock is fixed by the external timing resistor R_T. The SYNC pin can be tied to GND through a series resistor to prevent false triggering in a noisy environment.

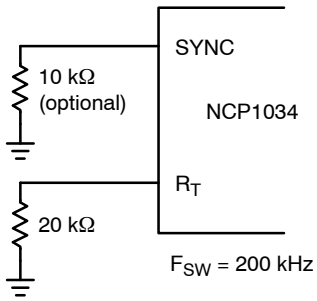

Figure 22. Fixed Frequency

Figure 23 shows the part synchronized to an external clock through the SYNC pin. The synchronization frequency can be up to 20% greater then the programmed fixed frequency (Example: R_T = 20 kΩ / 200 kHz and the SYNC input frequency can range from 200−220 kHz). The clock frequency at the SYNC pin replaces the master clock generated by the internal oscillator circuit. Pulling the SYNC pin low programs the part to run freely at the frequency programmed by R_T. When pulling the SYNC pin low a 4.7 kΩ resistor should be used.

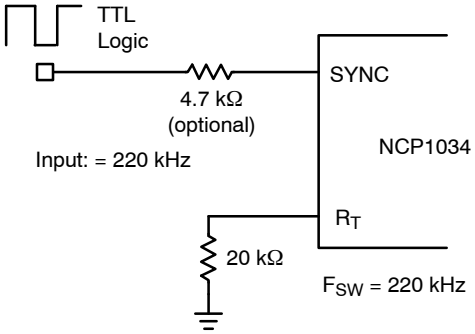

Figure 23. External Synchronization

Figure 24 shows the part operating in the master slave synchronization configuration. In this configuration all three parts are connected together through the SYNC pin in order to synchronize the system switching frequency. The R_T timing resistor can be the same value for all three parts (R_T = 20 kΩ / 20 kΩ / 20 kΩ) which would make the highest frequency part the master, or to guarantee one part is the master the timing resistor can be slightly lower in value. (R_T = 20 kΩ / 22 kΩ / 22 kΩ)

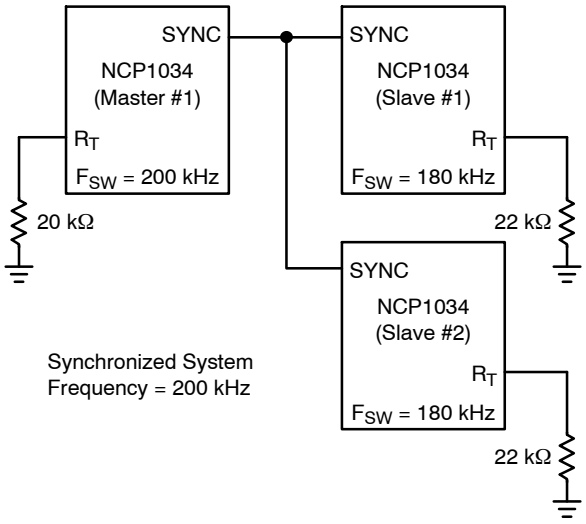

Figure 24. Master Slave Synchronization

Output Voltage

Output voltage can be set by an external resistor divider according to this Equation 3:

$$V_{OUT} = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \qquad \text{(eq. 3)}$$

Where V_{ref} is the internal reference voltage 1.25 V. Absolute values of resistors R1 and R2 depend on compensation network type. See compensation paragraph for details.

Inductor Selection

The inductor selection is based on the output power, frequency, input and output voltage and efficiency requirements. High inductor values cause low current ripple, slower transient response, higher efficiency and increased size. Inductor design can be reduced to desire maximum current ripple in the inductor. It is good to have current ripple (ΔI_{Lmax}) between 20% and 50% of the output current.

For buck converter, the inductor should be chosen according to Equation 4.

$$L = \left(\frac{V_{OUT}}{f \cdot \Delta I_{Lmax}}\right)\left(1 - \frac{V_{OUT}}{V_{INmax}}\right) \qquad \text{(eq. 4)}$$

Output Capacitor Selection

The output voltage ripple and transient requirements determine the output capacitor type and value. The important parameter for the selection of the output capacitor is equivalent serial resistance (ESR). If the capacitor has low ESR, it often has sufficient capacity for filtering as well as an adequate RMS current rating.

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The value of the output capacitor should be calculated using the following equation:

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot f \cdot \left(\Delta V_{OUT} - \Delta I_L \cdot ESR\right)} \quad \text{(eq. 5)}$$

For higher switching frequency, it is suitable to use multi−layer ceramic capacitor (MLCC) with very low ESR. The advantages are small size, low output voltage ripple and fast transient response. The disadvantage of MLCC type is the requirement to use a Type III compensation network.

Input Capacitor Selection

The input capacitor is used to supply current pulses while high−side MOSFET is on. When the MOSFET is off, the input capacitor is being charged. The value of this capacitor can be selected with Equation 6:

$$C_{IN} \geq \frac{I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f \cdot \Delta V_{IN}} \quad \text{(eq. 6)}$$

Where ΔV_{IN} is the input voltage ripple and the recommended value is about 2% − 5% of V_{IN}. The input capacitor must be large enough to handle the input ripple current. Its value should be calculated using Equation 7:

$$I_{RMS} = I_{OUT} \cdot \sqrt{\frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{V_{IN}}} \quad \text{(eq. 7)}$$

Power MOSFET Selection

The NCP1034 uses two N−channel MOSFET's. They can be primary selected by $R_{DS(on)}$, maximum drain−to−source voltage and gate charge. $R_{DS(on)}$ impacts conductive losses and gate charge impacts switching losses. The low side MOSFET is selected primarily for conduction losses, and the high−side MOSFET is selected to reduce switching losses especially when the output voltage is less than 30% of the input voltages. The drain−to−source breakdown voltage must be higher than the maximum input voltage. Conductive power losses can be calculated using the Equations 8 and 9:

$$P_{COND-HIGHFET} = I^2_{OUT} \cdot R_{DS(on)} \cdot \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 8)}$$

$$P_{COND-LOWFET} = I^2_{OUT} \cdot R_{DS(on)} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 9)}$$

Switching losses are depended on drain−to−source voltage at turn−off state, output current and switch−on and switch−off time as is shown by Equation 10.

$$P_{SW} = \frac{V_{DS(off)}}{2} \cdot \left(t_{ON} + t_{OFF}\right) \cdot f \cdot I_{OUT} \quad \text{(eq. 10)}$$

t_{ON} and t_{OFF} times are dependent on the transistor gate. The MOSFET output capacitance loss is caused by the charging and discharging during the switching process and can be computed using Equation 11.

$$P_{COSS} = \frac{C_{OSS} \cdot V_{IN}{}^2 \cdot f}{2} \quad \text{(eq. 11)}$$

Where $C_{OSS} = C_{DS} + C_{GD}$.

Significant power dissipation is caused by the reverse recovery charge in the low−side MOSFET body diode, which conducts at dead time. This charge is needed to close the diode. The current from the input power supply flows through the high−side MOSFET to the low−side MOSFET body diode. This power dissipation can be calculated using Equation 12.

$$P_{QRR} = Q_{RR} \cdot V_{IN} \cdot f \quad \text{(eq. 12)}$$

Q_{RR} is the diode recovery charge as given in the manufacturer's datasheet. For some types of MOSFETs, this dissipation may be dominant at high input voltages. It is necessary to take care when selecting a MOSFET. An external Schottky diode across the low−side MOSFET can be used to eliminate the reverse recovery charge power loss. The Schottky diode's forward voltage should be lower than that of the body diode, and reverse recovery time (t_{rr}) should be lower then that of the body diode. The Schottky diode's capacitance loss can be calculated as shown in Equation .

$$P_{C(Schottky)} = \frac{C_{Schottky} \cdot V_{IN}{}^2 \cdot f}{2} \quad \text{(eq. 13)}$$

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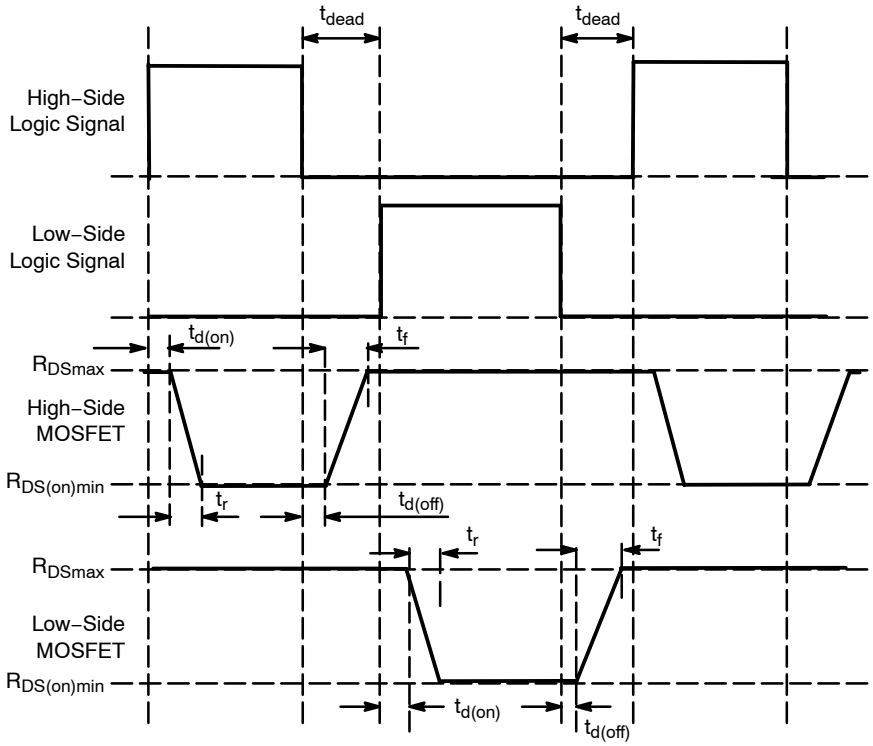

Figure 25. MOSFETs Timing Diagram

MOSFETs delays, turn−on and turn−off times must be short enough to prevent cross conduction. If not, there will be cross conduction from the input through both MOSFETs to ground. Due to this fact, the following conditions must be true:

$$t_{d(on)high} + t_{dead} > t_{d(off)low} + t_{f\,low}$$
$$t_{d(on)low} + t_{dead} > t_{d(off)high} + t_{f\,high} \qquad \text{(eq. 14)}$$

Where t_{dead} is the controller dead band time, $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f are MOSFETs parameters. These parameters can be found in the datasheet for specific conditions.

It is NOT recommended to add external resistor or other circuit on MOSFETs' gates to slow−down their turn−off. If gate resistance is a must, please make sure the above condition in eq. 14 is still satisfied to avoid cross conduction.

Bootstrap Circuit

This circuit is used to obtain a voltage higher than the input voltage in order to switch−on high side N MOSFET. The bootstrap capacitor is charged from the IC's supply voltage through D1, when the low side MOSFET is switched−on up to the IC's supply voltage. It must have enough capacity to supply power for the high−side circuit when the high−side MOSFET is being switched on. The minimum value recommended for the bootstrap capacitor is 100 nF. Diode D1 has to be designed to withstand a reverse voltage given by the following equation:

$$D1_{VRmin} = V_{IN} - V_{CC} \qquad \text{(eq. 15)}$$

Soft−Start

The soft−start time is set by capacitor connected between SS/$\overline{SD}$ Pin and ground. This function is used for controlling the output voltage slope and limiting startup currents. The start−up sequence initiates when Power On Ready (POR) internal signal rises to logic high level. That means the supply voltage, low side drive supply voltage and external UVLO are over the set thresholds. The soft−start capacitor is charged by 20 μA current source. If POR is low, the SS/$\overline{SD}$ Pin is internally pulled to GND, which means that the NCP1034 is in a shutdown state. The SS/$\overline{SD}$ Pin voltage (0 V to 2.6 V) controls internal current source (64 μA to 0 μA) with negative linear characteristic. This current source injects current into the resistor (25 kΩ) connected between the Fb pin and negative input of the error amplifier and into the external feedback resistor network. Voltage drop on these resistors is over 1.6 V, which is enough to force the error amplifier into negative saturation state and to block switching.

Note that at cold ambient temperatures (−35°C) the internal 25 kΩ drops up to 25% in value and so does the internal current source (64 μA) up to 10%. For those reasons, users must compensate for these variations by increasing the external lower resistive divider value in order to force the error amplifier into negative saturation at Soft−Start. Here is an example at −35°C showing how to select the proper R2 resistor:

$R_{internal}$ ~ 19 kΩ
Internal Current Source ~ 58 μA
$V_{Rinternal}$ = 19 kΩ x 58 μA = 1.1 V
Select R2 such that;
V_{R2} = 1.6 V − 1.1 V = 0.5 V

$$R_{2min} = \frac{0.5\ V}{58\ \mu A} = 8.6\ k\Omega.$$

The minimum value required for R2 to keep Comp at GND is 8.6 kΩ.

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When the soft−start pin reaches around 1.2 V (exact value depends on feedback and compensation network and on soft−start capacitor; a larger soft−start capacitor and a lower compensation capacity decrease this level) the IC starts switching. The impact of controlled current source decreases and the output voltage starts to rise. When the soft−start capacitor voltage reaches 2.6 V, the output voltage is at nominal value.

The soft−start time must be at least 10 times longer than the time needed to charge the compensation network from the output of the error amplifier. If the soft−start time is not long enough, the soft−start sequence would be faster than the charging compensation network and the IC would start without slowly increasing the output voltage. The soft−start capacitance can be calculated using Equation 16.

$$C_{SS} = 15 \cdot 10^{-6} \cdot T_{SS} \quad \text{(eq. 16)}$$

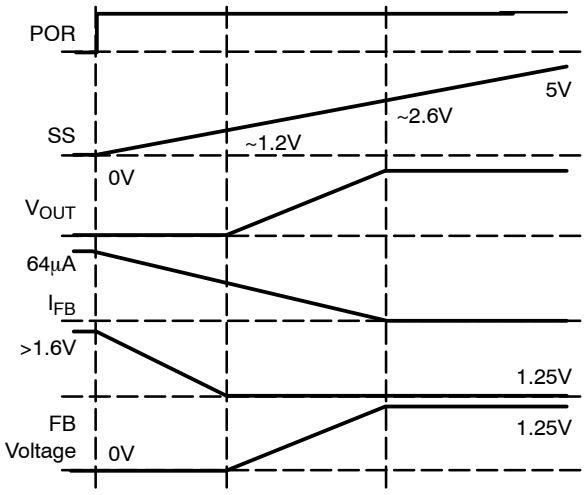

Figure 26. Soft−Start

Start to Prebiased Output

The NCP1034 is able to startup into a prebiased output capacitor. The low−side MOSFET does not turn on before high−side MOSFET gets the first turn−on pulse. During this time, the energy is not discharged by the low−side MOSFET until the soft−start sequence crosses the programmed output voltage.

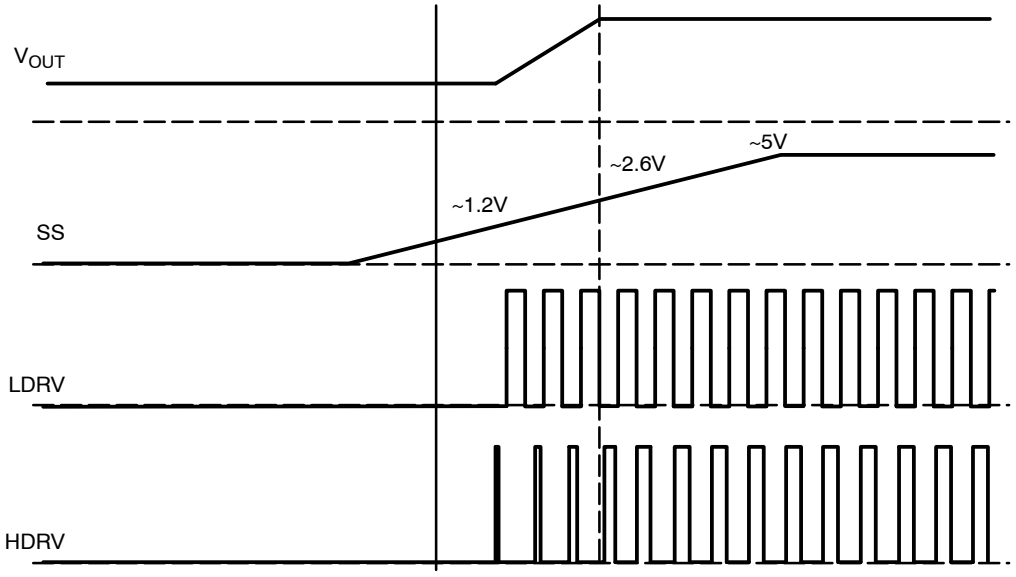

Figure 27. Startup to Prebiased Output

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Overcurrent Protection

The voltage drop across the low side MOSFET $R_{DS(on)}$ is connected through resistor R8 and into the IC though pin 13 OC_{in}. Within the IC, this value is compared with the value programmed by resistor R7 to set the overcurrent limit. The programmed current limit is set by selecting the value of R7, which is connected between pin 1 OCset and GND. If the voltage drop is larger than the set value, the NCP1034 goes into hiccup mode. During this time, both external MOSFETs are turned off and the soft start capacitor is discharged with a current equal to 5% of the charging current. The capacitor continues to discharge until the voltage reaches 0.25 V, and then the IC initiates a standard soft start sequence.

The recommended value for the protection resistor R8 is 10 kΩ. The R7 resistance value can be calculated using Equation 17:

$$R_7 = \frac{R8}{3.56 \cdot R_{DS(on)} \cdot I_{pk}} \qquad \text{(eq. 17)}$$

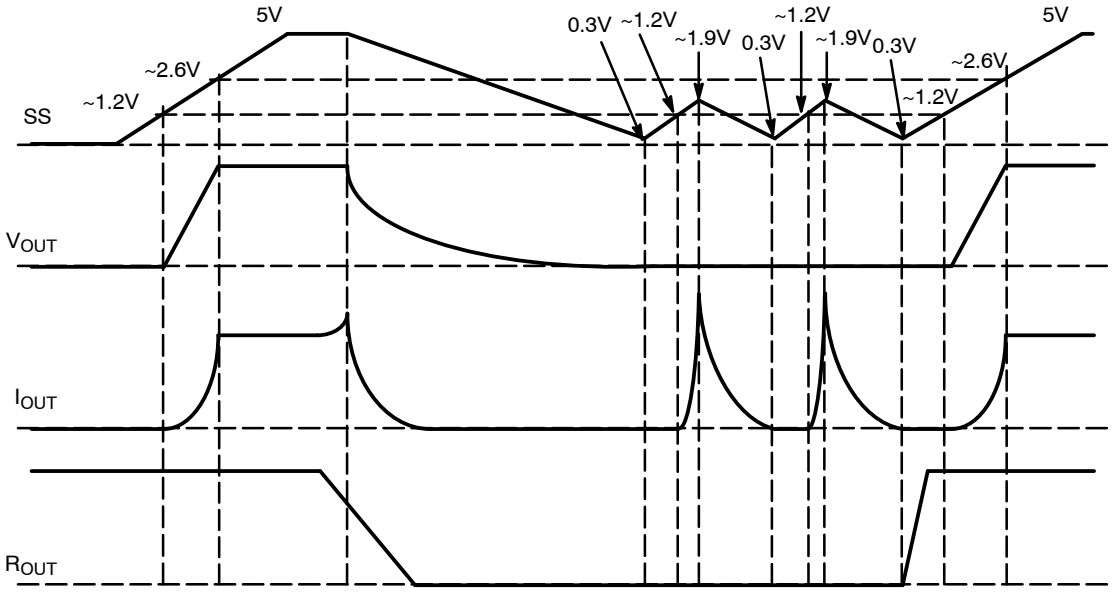

Figure 28. Overcurrent Protection (Hi−Cup Mode)

The NCP1034 provides protection of the low−side MOSFET against positive overcurrent (from output to this MOSFET). Its value can be calculated using Equation 18:

$$I_{Pos} = \frac{5125 - 0.184 \cdot R8 \cdot 1.25}{R7 \cdot R_{DS(on)}} \qquad \text{(eq. 18)}$$

NCP1034's overcurrent protection threshold could be affected by external circuits and PCB layout. Please pay attention to the following:

- Do not slow down the low−side MOSFET turning−on by any resistance or other circuit on its gate. About 80 ns after the rising edge of LDRV pin, the NCP1034 overcurrent protection function starts. If the low−side MOSFET hasn't been fully turned−on then, the overcurrent protection may be falsely triggered, even at very low load current.
- OCin trace layout
  The OCin trace, between OCin pin and R8, is a high impedance node. Any noise coupling to it may falsely trigger overcurrent protection. Please avoid any noise source near this OCin trace, such as VS, VB, HDRV and LDRV nodes. Any capacitance on the OCin pin impacts the overcurrent protection threshold as well. Therefore, it is not recommended.
- The voltage difference between PGND pin and low−side MOSFET source pin affects overcurrent protection threshold. As shown in Figure 2, the overcurrent comparator input pin OCin is reference to PGND pin. Therefore, the overcurrent protection threshold should factor in the voltage difference between the external MOSFET's source pins and the NCP1034's PGND pin.
- fix R8 = 10 kΩ
  As shown in Eq. 17 and Eq. 18, R8 resistance affects overcurrent limit threshold and positive overcurrent limit threshold in opposite directions. To simplify the design, please fix R8 at 10 kΩ as possible, and use R7 to program overcurrent limit threshold.

Compensation Circuit

The NCP1034 is a voltage mode buck convertor with a transconductance error amplifier compensated by an external compensation network. Compensation is needed to achieve accurate output voltage regulation and fast transient response. The goal of the compensation circuit is to provide a loop gain function with the highest crossing frequency and adequate phase margin (minimally 45°).

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The transfer function of the power stage (the output LC filter) is a double pole system. The resonance frequency of this filter is expressed as follows:

$$f_{P0} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}} \quad \text{(eq. 19)}$$

One zero of this LC filter is given by the output capacitance and output capacitor ESR. Its value can be calculated by using the following equation:

$$f_{Z0} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR} \quad \text{(eq. 20)}$$

The next parameter that must be chosen is the zero crossover frequency f_0. It can be chosen to be 1/10 – 1/5 of the switching frequency. These three parameters show the necessary type of compensation that can be selected from Table 1.

Table 1. COMPENSATION TYPES

Zero Crossover Frequency Condition	Compensation Type	Typical Output Capacitor Type
$f_{P0} < f_{Z0} < f_0 < f_S/2$	Type II (PI)	Electrolytic, Tantalum
$f_{P0} < f_0 < f_{Z0} < f_S/2$	Type III (PID) Method I	Tantalum, Ceramic
$f_{P0} < f_0 < f_S/2 < f_{Z0}$	Type III (PID) Method II	Ceramic

Compensation Type II (PI)

This compensation is suitable for low−cost electrolytic capacitor. The zero created by the capacitor's ESR is a few kHz and the zero crossover frequency is chosen to be 1/10 of the switching frequency. Components of the PI compensation (Figure 29) network can be specified by the following equations:

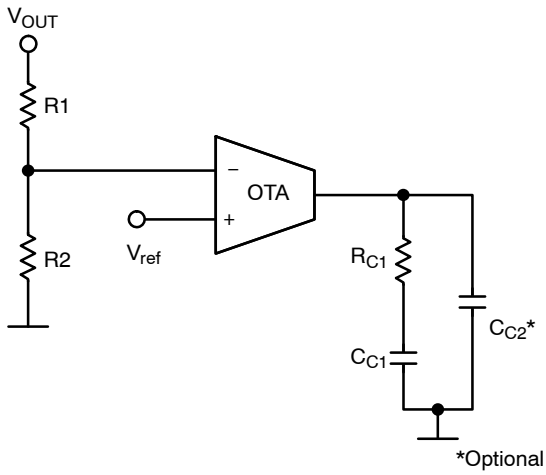

Figure 29. PI compensation (II Type)

$$R_{C1} = \frac{2 \cdot \pi \cdot f_0 \cdot L \cdot V_{RAMP} \cdot V_{OUT}}{ESR \cdot V_{IN} \cdot V_{ref} \cdot gm}$$

$$C_{C1} = \frac{1}{0.75 \cdot 2 \cdot \pi \cdot f_{P0} \cdot R_{C1}} \quad \text{(eq. 21)}$$

$$C_{C2} = \frac{1}{\pi \cdot R_{C1} \cdot f_S}$$

$$R1 = \frac{V_{OUT} - V_{ref}}{V_{ref}} \cdot R2$$

V_{RAMP} is the peak−to−peak voltage of the oscillator ramp and gm is the transconductance error amplifier gain. Capacitor C_{C2} is optional.

Compensation Type III (PID)

Tantalum and ceramics capacitors have lower ESR than electrolytic, so the zero of the output LC filter goes to a higher frequency above the zero crossover frequency. This situation needs to be compensated by the PID compensation network that is show in Figure 30.

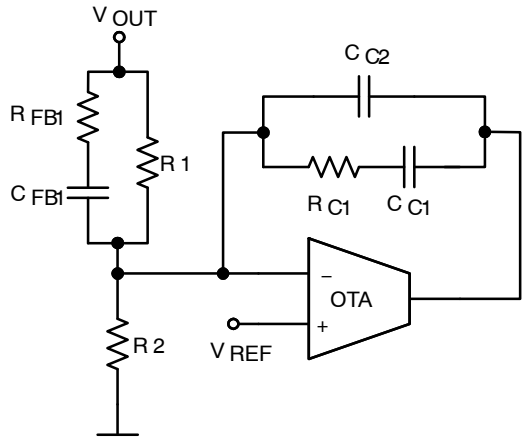

Figure 30. PID Compensation (III Type)

There are two methods to select the zeros and poles of compensation network. The first one (method I) is useable for tantalum output capacitors, which have a higher ESR than ceramic, and its zeros and poles can be calculated shown below:

$$f_{Z1} = 0.75 \cdot f_{P0}$$

$$f_{Z2} = f_{P0}$$

$$f_{P2} = f_{Z0} \quad \text{(eq. 22)}$$

$$f_{P3} = \frac{f_S}{2}$$

The second one (method II) is for ceramic capacitors:

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$$f_{Z2} = f_0 \cdot \sqrt{\frac{1 - \sin\theta_{max}}{1 + \sin\theta_{max}}}$$
$$f_{P2} = f_0 \cdot \sqrt{\frac{1 + \sin\theta_{max}}{1 - \sin\theta_{max}}} \quad \text{(eq. 23)}$$
$$f_{Z1} = 0.5 \cdot f_{Z2}$$
$$f_{P3} = 0.5 \cdot f_S$$

The remaining calculations are the same for both methods.

$$R_{C1} >> \frac{2}{gm}$$
$$C_{C1} = \frac{1}{2 \cdot \pi \cdot f_{Z1} \cdot R_{C1}}$$
$$C_{C2} = \frac{1}{2 \cdot \pi \cdot f_{P3} \cdot R_{C1}}$$
$$C_{FB1} = \frac{2 \cdot \pi \cdot f_0 \cdot L \cdot V_{RAMP} \cdot C_{OUT}}{V_{IN} \cdot R_{C1}} \quad \text{(eq. 24)}$$
$$R_{FB1} = \frac{1}{2\pi \cdot C_{FB1} \cdot f_{P2}}$$
$$R1 = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot f_{Z2}} - R_{FB1}$$
$$R2 = \frac{V_{ref}}{V_{OUT} - V_{ref}} \cdot R1$$

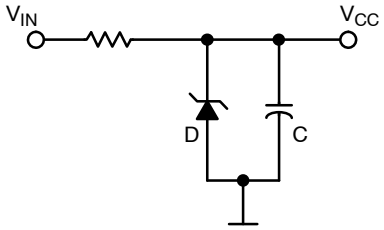

Figure 31. Linear Shunt Voltage Regulator

For the linear shunt voltage regulator (option a) the V_{CC} voltage is the same as the zener diode reverse voltage V_Z. The value of the resistor R can be calculated using Equation 28, where I_{ZT} is the minimum reverse current at V_Z. The value selected should be lower than the calculated value. The maximum power losses of resistor R and the zener diode D can be calculated by Equations 29 and 30.

$$R < \frac{V_{INmin} - V_{CC}}{I_{CS} + I_{CD} + I_{ZT}} \quad \text{(eq. 28)}$$
$$P_R = (V_{INmax} - V_{CC}) \cdot (I_{CS} + I_{CD}) \quad \text{(eq. 29)}$$
$$P_D = \left(\frac{V_{INmax} - V_{CC}}{R} - ICS\right) \quad \text{(eq. 30)}$$

To check the design of this compensation network, the equation must be true

$$R1 \parallel R2 \parallel R_{FB1} > \frac{1}{gm} \quad \text{(eq. 25)}$$

If it is not true, then a higher value of R_{C1} must be selected.

Input Power Supply

The NCP1034 controller and built−in drivers need to be powered through V_{CC}, $DRVV_{CC}$ and V_b pins with a voltage between 10 V – 18 V. The supply current requirement is a summation of the static and dynamic currents. Static current consumption can be calculated by the following equation:

$$I_{CS} = I_{CC} + I_C + I_B \quad \text{(eq. 26)}$$

Dynamic current consumption is calculated using the following equation, base on the switching frequency and MOSFET gate charge.

$$I_{CD} = \left(Q_{G(low)} + Q_{G(high)}\right) \cdot f \quad \text{(eq. 27)}$$

To power the device, an external power supply or voltage regulator from V_{IN} can be used. Two options are a linear shunt voltage regulator and a shunt voltage regulator with transistor, as shown in Figure 31. A voltage regulator without a transistor can be used when the power consumption is low and zener diode power dissipation is acceptable. Otherwise, a shunt regulator with transistor can be used.

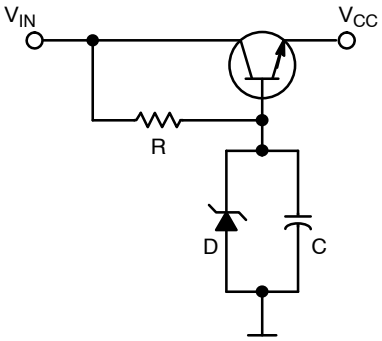

Figure 32. Shunt Voltage Regulator with Transistor

The shunt voltage regulator with transistor (option b) is advantageous when the zener diode loss is too high or when input voltage varies across a wide range and it is difficult to set a bias point. The output voltage is lower than V_Z due to the V_{BE} of the transistor. The maximum resistor value of R can be calculated by Equation 31, where β is the transistor DC current gain. The maximum power dissipation of the resistor, zener diode and transistor are calculated by Equations 32 to 34. The transistor reverse breakdown voltage must be selected to be able to withstand the voltage difference between maximum input voltage and VCC.

$$R < \frac{V_{INmin} - V_{ZT}}{\frac{I_{CS}+I_{CD}}{\beta} + I_{ZT}} \quad \text{(eq. 31)}$$

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$$P_R = \left(V_{INmax} - V_{CC}\right) \cdot \left(\frac{I_{CS} + I_{CD}}{\beta} + I_{ZT}\right) \quad \text{(eq. 32)}$$

$$P_D = \left(\frac{V_{INmax} - V_{ZT}}{R} - \frac{I_{CS}}{\beta}\right) \cdot V_{ZT} \quad \text{(eq. 33)}$$

$$P_D = \left(\frac{V_{INmax} - V_{ZT}}{R} - \frac{I_{CS}}{\beta}\right) \cdot V_{ZT} \quad \text{(eq. 34)}$$

$$P_T = \left(V_{INmax} - V_{CC}\right) \cdot \left(I_{CS} + I_{CD}\right) \quad \text{(eq. 35)}$$

Table 2. POWER SUPPLY REGULTOR EXAMPLES

Components	MOSFETs	$Q_{G(TOT)}$ (nC)	f (kHz)	V_{INmax} (V)	V_{INmin} (V)	$I_{SUPPLYmax}$ (mA)	R_{BIAS} (kΩ)	ZD	Transistor
LS−FET	NTD24N06	24	200	60	36	8.7	2.6	MMSZ4699	−
HS−FET	NTD3055	7.1							
LS−FET	NTD24N06	24	300	60	20	16.9	10	MMSZ4699	MJD31
HS−FET	NTD24N06	24							

PCB Layout

The layout of high−frequency and high−current switching converters has a large impact on the circuit parameters. It is important, therefore, to pay close attention to the PCB layout.

The input capacitor, MOSFETs, inductor and output capacitor should be placed as close as possible to one another. This is suitable to reduce EMI and to minimize VS overshoots. Connecting the signal and power ground at one point near the output connector improves load regulation. Connection between the source pin of the low side MOSFET and the IC should be very short with wide traces and optimally using two layers to achieve minimum inductance between them.

The blocking and bootstrap capacitors should be placed as close as possible to the IC. The feedback and compensation network should be close to the IC to minimize noise.

TYPICAL APPLICATION

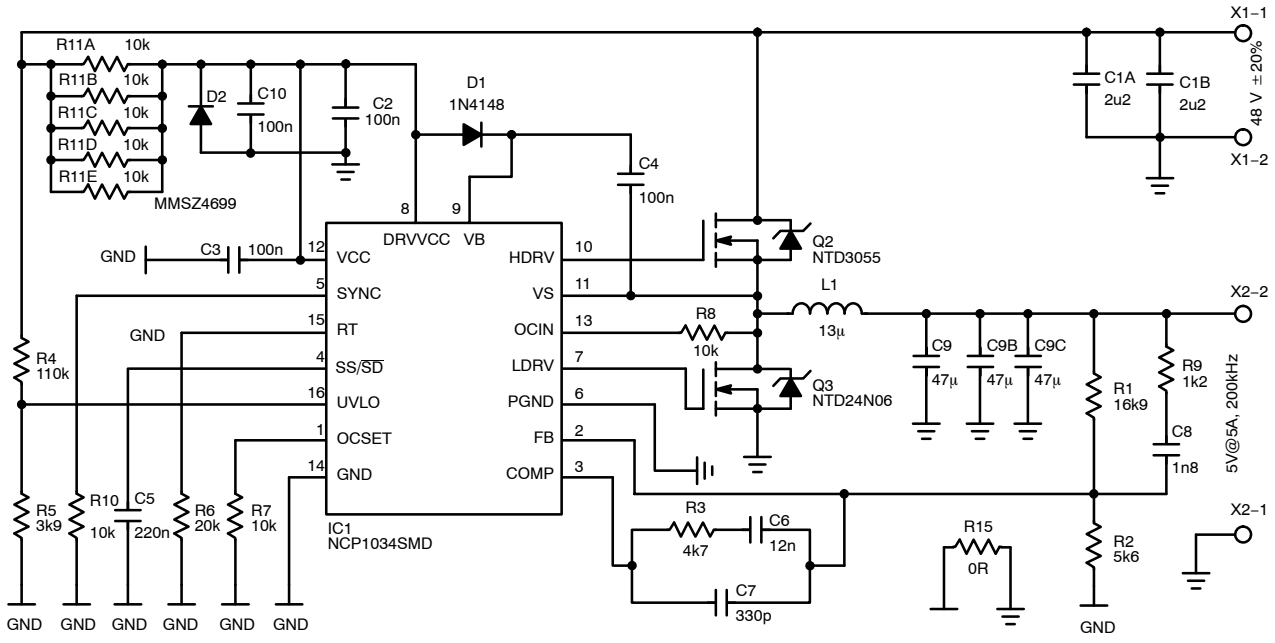

Figure 33. Single Output Buck Converter from 38 V − 58 V to 5 V/5 A @ 200 kHz

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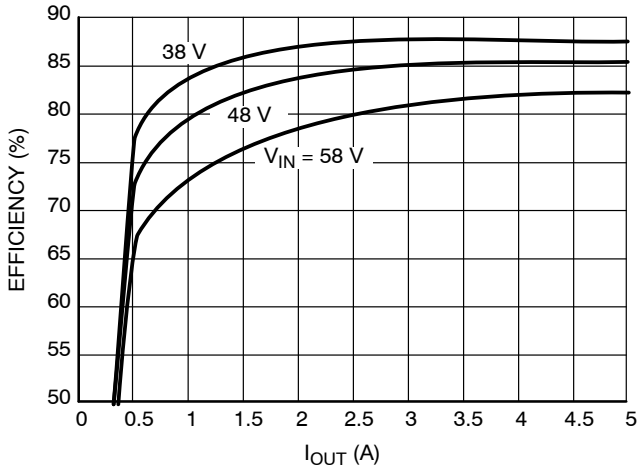

Figure 34. Efficiency and Power Loss of Circuit at Figure 33

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Bill of Materials

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
R9	1	Resistor	1k2	1%	1206	Vishay	CRCW10261K20FKEA
R5	1	Resistor	3k9	1%	1206	Vishay	CRCW10263K90FKEA
R3	1	Resistor	4k7	1%	1206	Vishay	CRCW10264K60FKEA
R2	1	Resistor	5k6	1%	1206	Vishay	CRCW10265K60FKEA
R1	1	Resistor	16k9	1%	1206	Vishay	CRCW102616K9FKEA
R6	1	Resistor	20k	1%	1206	Vishay	CRCW102620K0FKEA
R11A, R11B, R11C, R11D, R11E	5	Resistor	12k	1%	1206	Vishay	CRCW102612K0FKEA
R4	1	Resistor	110k	1%	1206	Vishay	CRCW1206110KFKEA
R7, R8, R10	3	Resistor	10k	1%	1206	Vishay	CRCW120610K0FKEA
C8	1	Ceramic Capacitor	1n8	10%	1206	Kemet	C1206C182K5FA−TU
C6	1	Ceramic Capacitor	12n	10%	1206	Kemet	C1206C123K5FACTU
C5	1	Ceramic Capacitor	220n	10%	1206	Kemet	C1206C224K5RACTU
C7	1	Ceramic Capacitor	330p	10%	1206	Kemet	−
C2, C3, C4, C10	4	Ceramic Capacitor	100n	10%	1206	Kemet	C1206F104K1RACTU
C9A, C9B, C9C	3	Ceramic Capacitor	47μ/6.3V	20%	1210	Kemet	C1210C476M9PAC7800
C1A, C1B	2	Ceramic Capacitor	2.2μ/100V	10%	1210	Murata	GRM32ER72A225KA35L
L1	1	Inductor SMD	13μ	20%	13x13	Würth	744355131
D1	1	Switching Diode	MMSD4148	−	SOD123	**onsemi**	MMSD4148T1G
D2	1	Zener Diode 12V	MMSZ4699	−	SOD123	**onsemi**	MMSZ4699T1G
Q2	1	Power N−MOSFET	NTD3055	−	DPAK	**onsemi**	NTD3055−150G
Q3	1	Power N−MOSFET	NTD24N06	−	DPAK	**onsemi**	NTD24N06T4G
IO1	1	Synchronous PWM Buck Controller	NCP1034	−	SOIC16	**onsemi**	NCP1034DR2G

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Your Opinion Matters

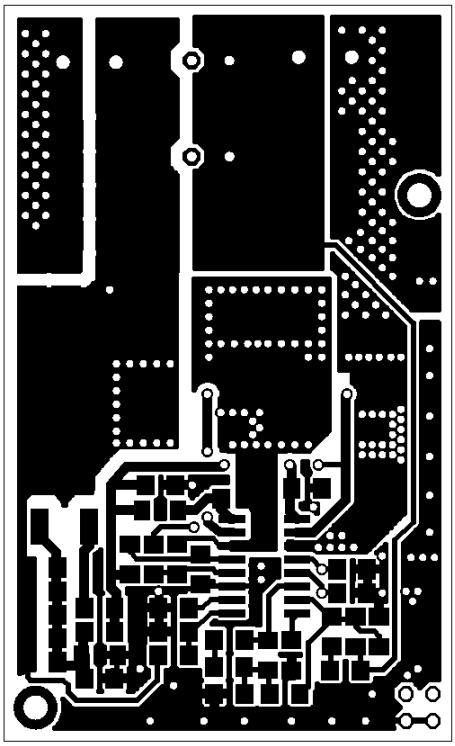

Figure 35. Top Layer

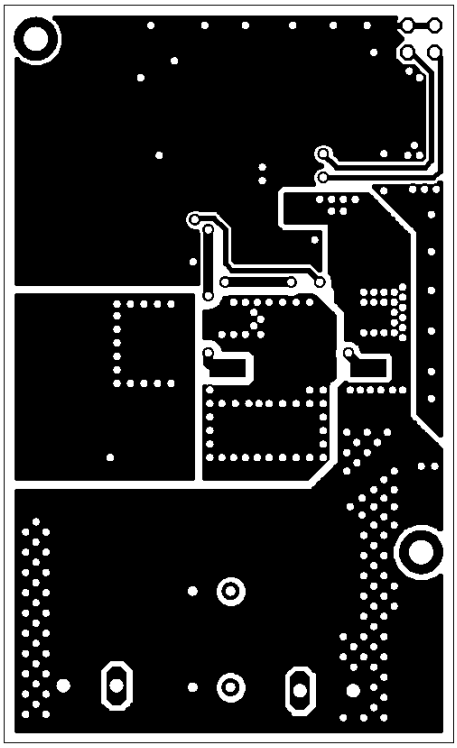

Figure 36. Bottom Layer

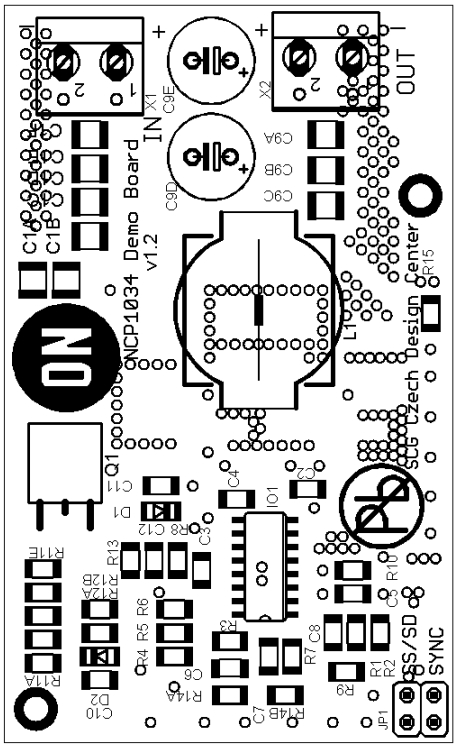

Figure 37. Top Side Components

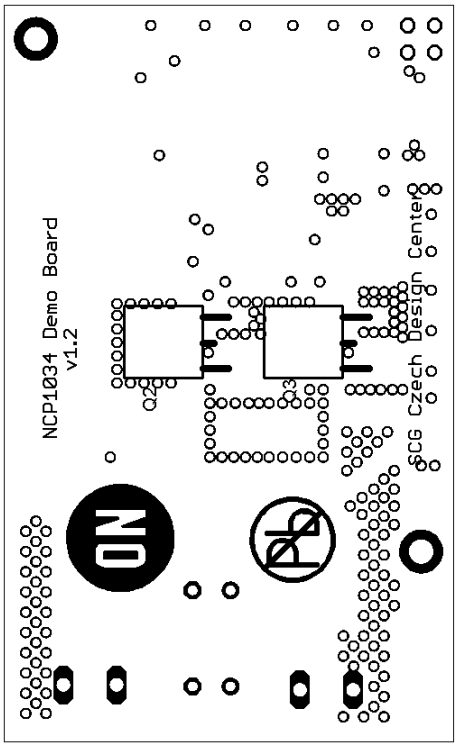

Figure 38. Bottom Side Components

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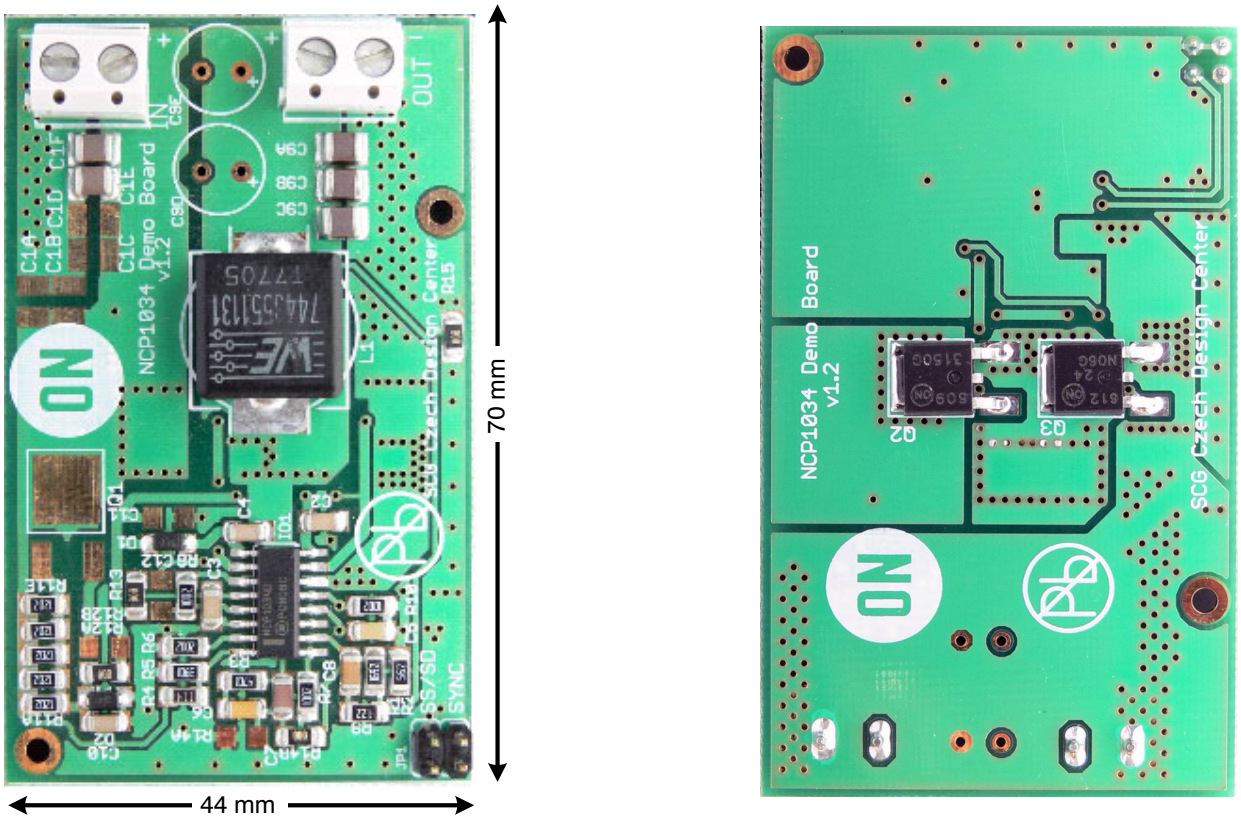


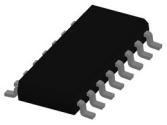
Figure 39. Typical Application Board Photos

ORDERING INFORMATION

Device	Package	Shipping†
NCP1034DR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

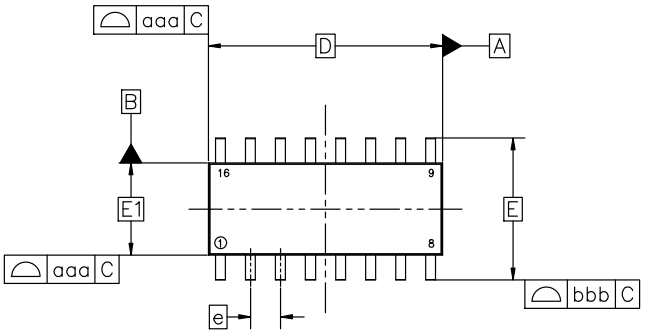
Share Feedback
Your Opinion Matters



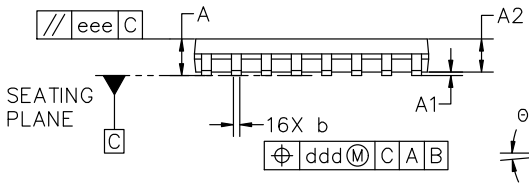
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

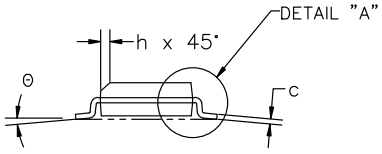
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



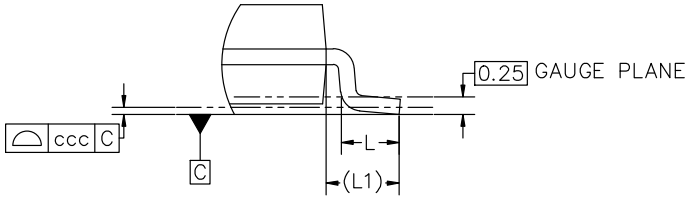
TOP VIEW



SIDE VIEW

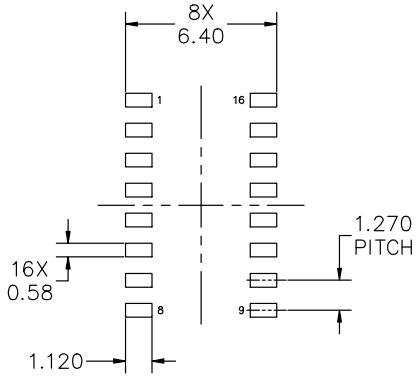


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

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SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

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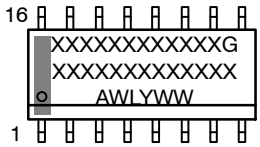
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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