LDO Regulator - CMOS, Low Iq, Enable, TSOP-5

150 mA

NCP699

The NCP699 series of fixed output LDO's are designed for handheld communication equipment and portable battery powered applications which require low quiescent current. The NCP699 series features a very low ground current of 40 µA, independent of load current. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, internal resistors for setting output voltage, current limit, and temperature limit protection circuits.

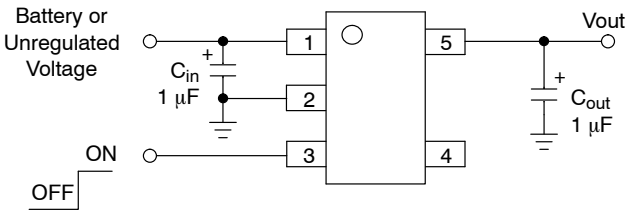
The NCP699 has been designed to be used with low cost capacitors. The device is housed in the micro-miniature TSOP-5 surface mount package. Standard voltage versions are 1.3, 1.4, 1.5, 1.8, 2.5, 2.8, 2.9, 3.0, 3.1, 3.3, 3.4, 4.5 and 5.0 V. Other voltages are available in 100 mV steps.

Features

- Enable Control (Active High, Supports Sub 1 V Logic)
- Very Low Ground Current of 40 µA Typical
- Low Dropout Voltage of 340 mV at 150 mA, and 3.0 V V_{out}
- Multiple Fixed Output Voltage Option
- Output Voltage Accuracy of 2.0%
- Operating Temperature Range of −40 °C to 85 °C
- Stable with 1 µF Ceramic or Tantalum Capacitors
- These are Pb-Free Devices

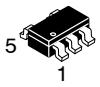
Typical Applications

- Cellular Phones
- Battery Powered Consumer Products
- Hand-Held Instruments
- Camcorders and Cameras
- Printers and Office Equipment



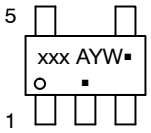
This device contains 86 active transistors

Figure 1. Typical Application Diagram



TSOP-5
(SOT23-5, SC59-5)
SN SUFFIX
CASE 483

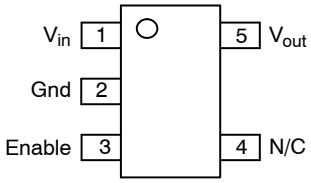
MARKING DIAGRAM



xxx	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.

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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	Vin	Positive power supply input voltage.
2	Gnd	Power supply ground.
3	Enable	This input is used to place the device into low-power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to Vin.
4	N/C	No internal connection.
5	Vout	Regulated output voltage.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	2.1 to 6.0	V
Enable Voltage	Enable	−0.3 to V_{in} +0.3	V
Output Voltage	V_{out}	−0.3 to V_{in} +0.3	V
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature	T_J	+150	°C
Maximum Junction Temperature	$T_{J(max)}$	+150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL-STD-883, Method 3015
   Machine Model Method 200 V
2. Latch-up capability (85 °C) ±200 mA DC with trigger voltage.

THERMAL CHARACTERISTICS

Rating	Symbol	Test Conditions	Typical Value	Unit
Junction-to-Ambient	$R_{\theta JA}$	1 oz Copper Thickness, 100 mm^2	250	°C/W
PSIJ-Lead 2	Ψ_{JL2}	1 oz Copper Thickness, 100 mm^2	68	°C/W

NOTE: Single component mounted on an 80 x 80 x 1.5 mm FR4 PCB with stated copper head spreading area. Using the following boundary conditions as stated in EIA/JESD 51-1, 2, 3, 7, 12.

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ELECTRICAL CHARACTERISTICS (V_{in} = $V_{out(nom.)}$ + 1.0 V, V_{enable} = V_{in}, C_{in} = 1.0 μF, C_{out} = 1.0 μF, T_A = 25 °C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_{out} = 10 mA, T_A = −40 °C to 85 °C) 1.3 V 1.4 V 1.5 V 1.8 V 2.5 V 2.8 V 2.9 V 3.0 V 3.1 V 3.3 V 3.4 V 4.5 V 5.0 V	V_{out}	 1.261 1.358 1.455 1.746 2.425 2.716 2.813 2.910 3.007 3.201 3.298 4.365 4.850	 1.3 1.4 1.5 1.8 2.5 2.8 2.9 3.0 3.1 3.3 3.4 4.5 5.0	 1.339 1.442 1.545 1.854 2.575 2.884 2.987 3.090 3.193 3.399 3.502 4.635 5.150	V
Line Regulation (I_{out} = 10 mA) 1.3 V–4.4 V (V_{in} = $V_{out(nom.)}$ + 1.0 V to 6.0 V) 4.5 V–5.0 V (V_{in} = 5.5 V to 6.0 V)	Reg_{line}	 – –	 1.0 1.0	 3.0 3.0	mV/V
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	0.3	0.8	mV/mA
Output Current Limit 1.3 V–3.9 V (V_{in} = $V_{out(nom.)}$ + 2.0 V) 4.0 V–5.0 V (V_{in} = 6.0 V)	$I_{o(nom.)}$	 150 150	 240 240	 – –	mA
Dropout Voltage (I_{out} = 150 mA, Measured at V_{out} = $V_{out(nom)}$ −3.0%) 1.3 V 1.4 V 1.5 V 1.8 V 2.5 V 2.8 V 2.9 V 3.0 V 3.1 V 3.3 V 3.4 V 4.5 V – 5.0 V	V_{in}–V_{out}	 – – – – – – – – – – – –	 800 750 690 570 400 360 350 340 330 320 300 240	 900 850 750 620 450 420 420 400 400 360 360 300	mV
Disable Current (T_A = −40 °C to 85 °C) (Enable Input = 0 V)	DIS	 –	 0.03	 1.0	μA
Ground Current (T_A = −40 °C to 85 °C) (Enable Input = V_{in}, I_{out} = 1.0 mA to $I_{o(nom.)}$)	I_{GND}	 –	 40	 90	μA
Output Short Circuit Current (V_{out} = 0 V) 1.3 V–3.9 V (V_{in} = $V_{out(nom.)}$ + 2.0 V) 4.0 V–5.0 V (V_{in} = 6.0 V)	$I_{out(max)}$	 150 150	 300 300	 600 600	mA
Output Voltage Noise (f = 100 Hz to 100 kHz) I_{out} = 30 mA, C_{out} = 1 μF	V_n	 –	 100	 –	μVrms
Ripple Rejection (f = 120 Hz, 15 mA) (f = 1.0 kHz, 15 mA)	RR	 – –	 55 50	 – –	dB
Enable Input Threshold Voltage (T_A = −40 °C to 85 °C) (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(en)}$	 0.95 –	 – –	 – 0.3	V
Output Voltage Temperature Coefficient	T_C	–	±100	–	ppm/°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

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TYPICAL CHARACTERISTICS

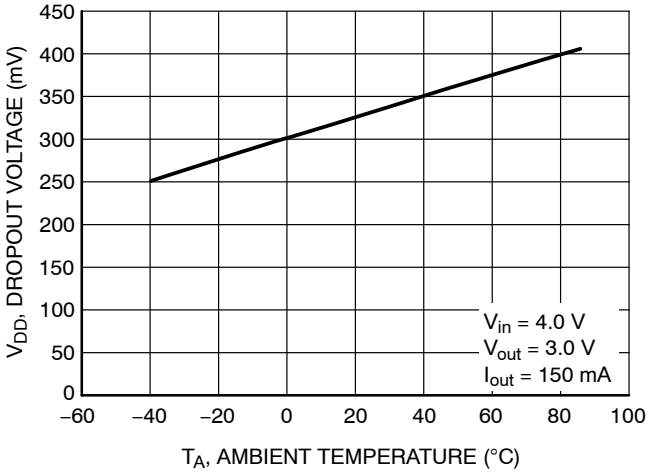


Figure 2. Dropout Voltage vs. Temperature

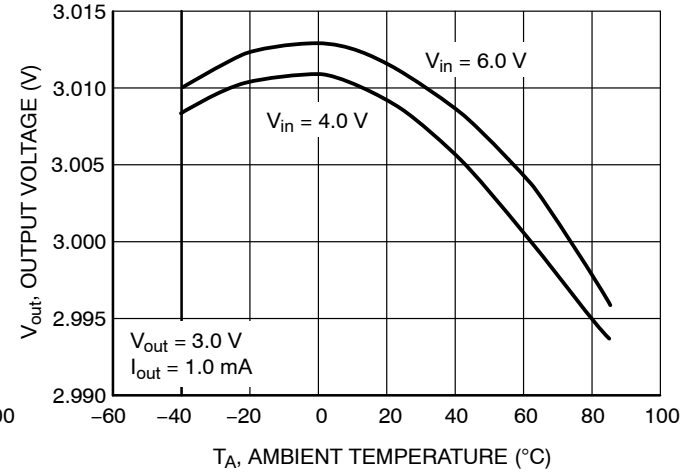


Figure 3. Output Voltage vs. Temperature

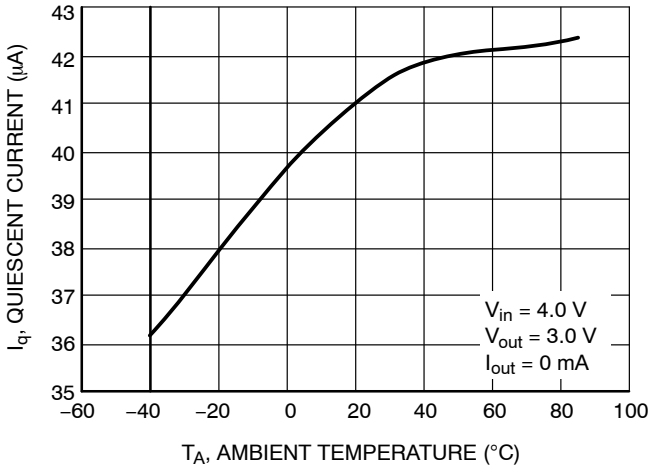


Figure 4. Quiescent Current vs. Temperature

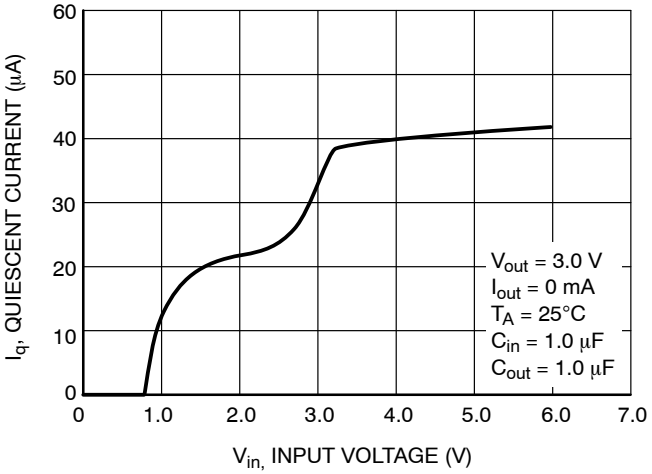


Figure 5. Quiescent Current vs. Input Voltage

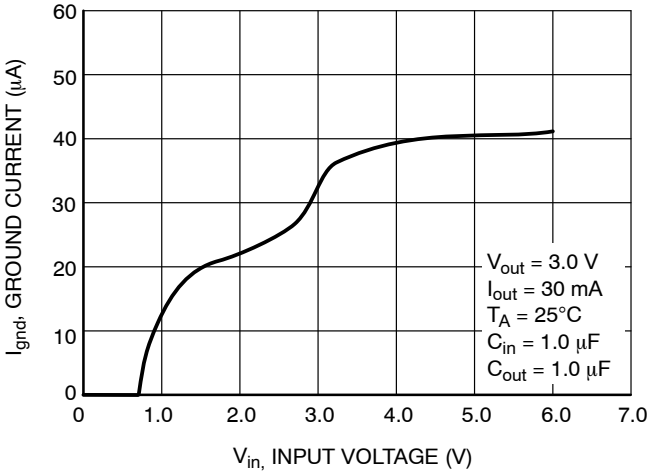


Figure 6. Ground Pin Current vs. Input Voltage

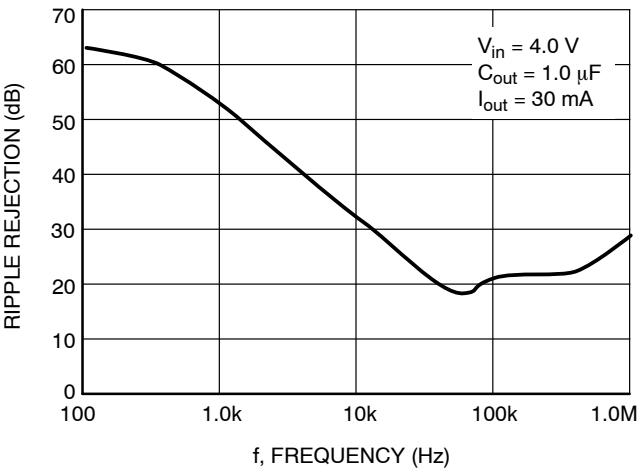


Figure 7. Ripple Rejection vs. Frequency

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TYPICAL CHARACTERISTICS

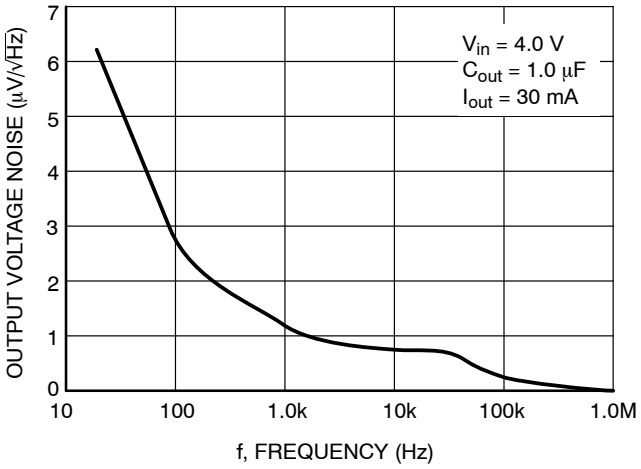


Figure 8. Output Noise Density

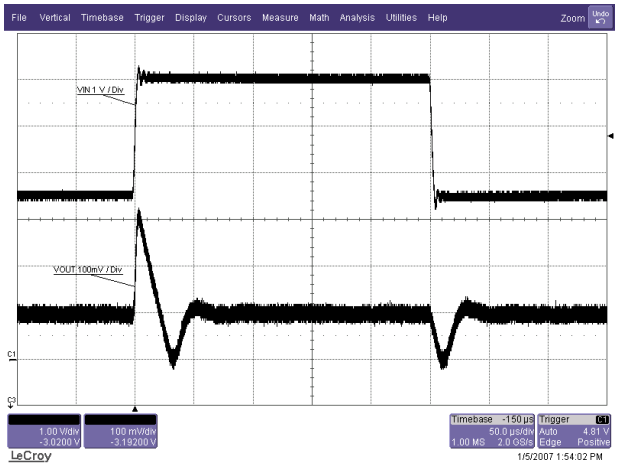


Figure 9. Line Transient Response

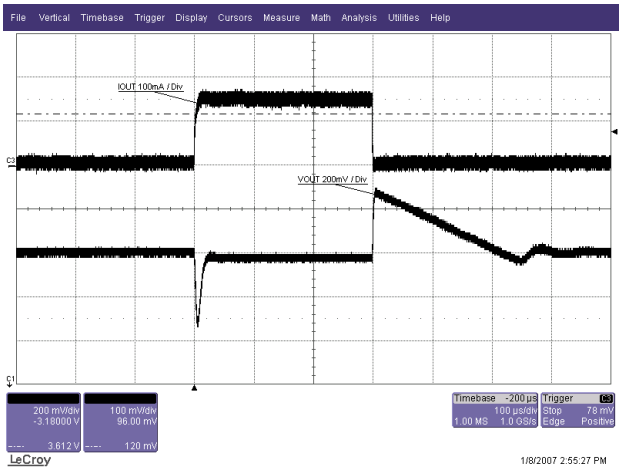


Figure 10. Load Transient Response

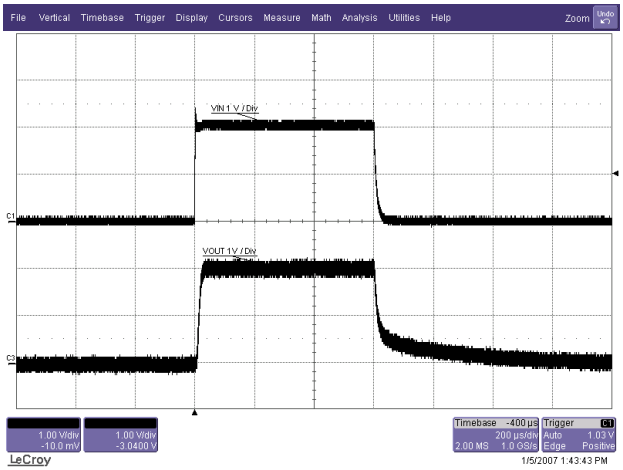


Figure 11. Turn-on Response

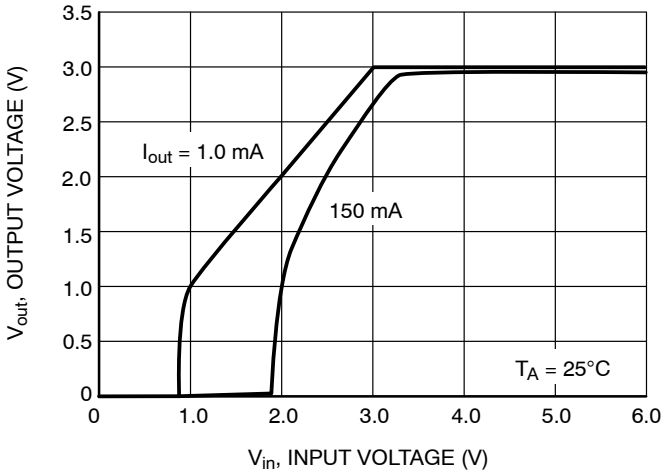


Figure 12. Output Voltage vs. Input Voltage

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DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3.0% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

Quiescent and Ground Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160 °C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125 °C. Depending on the ambient power dissipation and thus the maximum available output current.

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APPLICATIONS INFORMATION

A typical application circuit for the NCP699 series is shown in Figure 1, front page.

Input Decoupling (C_{in})

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP699 package. Higher values and lower ESR will improve the overall line transient response.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

Output Decoupling (C_{out})

The NCP699 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 5.0 Ω can thus safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum capacitors. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to V_{in}.

Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Thermal

As power across the NCP699 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP699 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum 125 °C, then the NCP699 can dissipate up to 400 mW @ 25 °C.

The power dissipated by the NCP699 can be calculated from the following equation:

$$P_{tot} = [V_{in} * I_{gnd}\ (@I_{out})] + [V_{in} - V_{out}] * I_{out}$$

or

$$V_{inMAX} = \frac{P_{tot} + V_{out} * I_{out}}{I_{gnd}(@I_{out}) + I_{out}}$$

If an 150 mA output current is needed then the ground current from the data sheet is 40 μA. For an NCP699 (3.0 V), the maximum input voltage will then be 5.65 V.

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ORDERING INFORMATION

Device	Nominal Output Voltage*	Marking	Package	Shipping†
NCP699SN18T1G	1.8	LJS	TSOP-5 (Pb-Free)	3000 Units/ 7″ Tape & Reel
NCP699SN29T1G	2.9	ACP		
NCP699SN30T1G	3.0	LJV		
NCP699SN33T1G	3.3	LJW		
NCP699SN34T1G	3.4	ACF		
NCP699SN50T1G	5.0	LJX		

DISCONTINUED (Note 5)

NCP699SN13T1G	1.3	LJY	TSOP-5 (Pb-Free)	3000 Units/ 7″ Tape & Reel
NCP699SN14T1G	1.4	AA4	TSOP-5 (Pb-Free)	3000 Units/ 7″ Tape & Reel
NCP699SN15T1G	1.5	LJP	TSOP-5 (Pb-Free)	3000 Units/ 7″ Tape & Reel
NCP699SN25T1G	2.5	LJT	TSOP-5 (Pb-Free)	3000 Units/ 7″ Tape & Reel
NCP699SN28T1G	2.8	LJU	TSOP-5 (Pb-Free)	3000 Units/ 7″ Tape & Reel
NCP699SN31T1G	3.1	AAE	TSOP-5 (Pb-Free)	3000 Units/ 7″ Tape & Reel
NCP699SN45T1G	4.5	ACQ	TSOP-5 (Pb-Free)	3000 Units/ 7″ Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* Additional voltages in 100 mV steps are available upon request by contacting your **onsemi** representative.

5. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

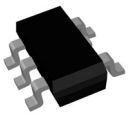
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REVISION HISTORY

Revision	Description of Changes	Date
9	Rebranded the Data Sheet to **onsemi** format. NCP699SN13T1G, NCP699SN14T1G, NCP699SN15T1G, NCP699SN25T1G, NCP699SN28T1G, NCP699SN31T1G, NCP699SN45T1G OPNs Marked as Discontinued.	2/4/2026

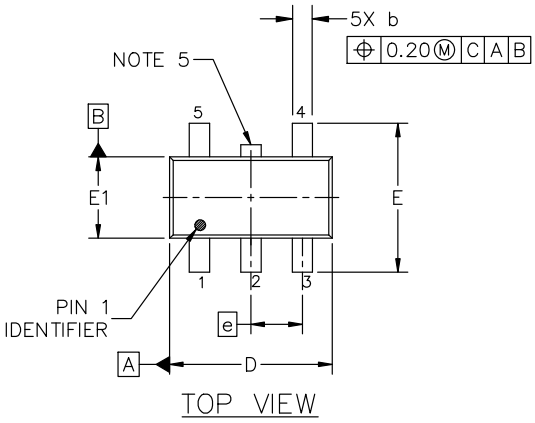
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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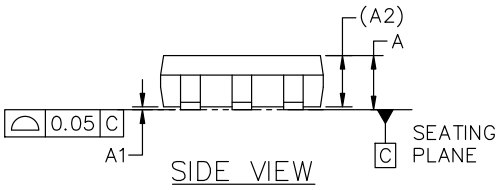


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

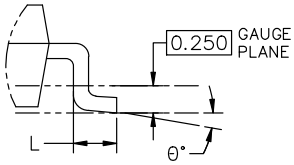
DATE 01 APR 2024



TOP VIEW



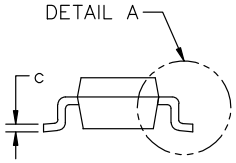
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

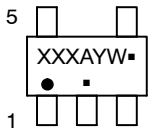
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

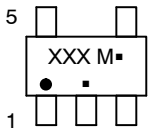
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

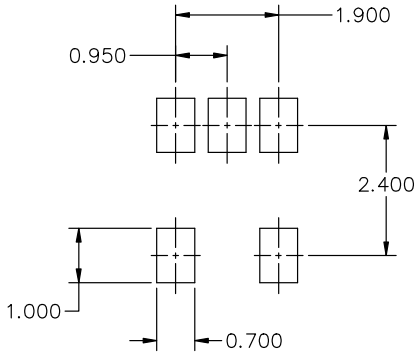
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98ARB18753C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

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